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Motor Drives

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Abstract

Three phase simultaneous current pulse control for a high frequency series resonant DC link converter was achieved by utilizing a previously developed pulse trimming method and current peak limiting with saturable core. Each resonant pulse is split to flow in three phases almost at a time so that very smooth sinusoidal output current waveform is attained. The duality of the series resonant dc link with the parallel resonant link is discussed. Simulation and the basic experiments are performed.

Introduction

Pulse Width Modulated (PWM) inverters with high frequency switchings are often utilized for driving various speed induction motors to avoid the torque ripple and the acoustic noise, keeping the efficiency high; while in contrary, the switching losses increase and the high efficiency can not be maintained even if high speed switching devices such as FETs and IGBTs are applied. High frequency resonant-link power conversion utilizing zero-volt or zero-current switching has been enormously developed recently. The method features the possibility of having not only a high power density, but also very low switching losses. In a previous paper in 1988, the authors presented a series resonant dc link type ac to ac power conversion scheme as shown in Fig. 1(a) [1]. The converter is a dual of the parallel resonant link type in Fig. 1(b) and the switching occurs at zero current instants. However, the method had such a problem as irregular current peak appearing when the output voltage changes suddenly, while the voltage peak problem happened for the parallel resonant type. The solution was an additional circuit with a capacitor and a transistor to limit the voltage [3]. Alternatively, the series resonant type had the solution with a simple saturable core to limit the current peaks [4].

The current control ability of the converter is enormously improved in this paper by using pulse-split concept in addition to the current peak limiting circuit. The current pulses iL are distributed to three phases almost at a time, dividing the original pulses at an optimal values such that a smooth current flow is available on the output. This flexible current control feature is essential to drive induction motors in order to reduce torque ripples as PWM inverters have.

Fig. 1. High frequency resonant dc link ac/ac converter.

Duality of Series Resonant DC Link

In the series resonant dc link converter in Fig. 1(a), a series inductance Ls and a capacitance Cs form the high frequency resonant circuit and both the three capacitors at the output and at the input are the filters to bypass the high frequency components to maintain the resonant frequency. Parallel inductance Lp superposes the dc current iL to the high frequency resonating current. In this circuit, for example, the resonating current starts by turning on thyristors as shown in black; as the average value of the current pulse is equal to the dc current iL, the adjustment can be done by the input converter although rapid adjustment is difficult because of the large inductance Lp.

Figure 1(b) shows the parallel resonant dc link converter. The resonance happens between the inductance Lp and the capacitance Cp, and the dc voltage E is superposed by the electrolytic capacitor C. This circuit generates high frequency voltage pulses across capacitor C and the pulses are distributed to three phase load.

Fig. 2(a) and (b) in solid line show the basic resonant circuits corresponding to Figs. 1(a) and (b), respectively. In Fig. 2(a), the voltage E is the output voltage of the input converter of Fig. 1(a), and thyristor Tj represents four thyristors conducting in series noted in black. When Tj is triggered the current starts to resonate and forms a galvanic current as shown in Fig. 2(c). After turning off, the inductance Lj charges up the capacitor Cj and the thyristor voltage Vj increases linearly. When Vj reaches preset threshold value Vj, the thyristor Th is again triggered to form the next pulse. Thus, the current pulse train is generated. The pulse train iL is fed to the output filter inductance Lf, keeping the voltage Vf almost constant and the voltage Vf is fed to the load. For three phase load, the circuit should have three capacitors fed by distributing thyristor-bridge as shown in Fig. 1(b).

Similarly for the parallel resonant type in Fig. 2(b), the resonant voltage Vf forms voltage pulse train by switching the transistor Tp. The voltage Vf is fed to flow almost constant current iL through filter inductance Lf to the load. For three phase operation the parallel resonant circuit needs three inductances and a transistor-bridge distributor as shown in Fig. 1(b).

If the dotted lines with dual elements are drawn in Fig. 2(b), the circuit becomes almost the same as series resonant circuit in Fig. 1(a). The only difference is the connecting point of capacitor Cj noted as "F". The original connecting point "F" on the ground "G" was changed to "F" on the source voltage E; the voltage across the capacitor becomes lower than the case of "F".
Dual-Flow with Current-Peak Limiting

Irregular Current Peaks

In Fig. 2 (a), if both the inductance \(L_d\) and the capacitor \(C_l\) are assumed sufficiently large and the dc bias current \(I_d\) and voltage \(V_L\) across the capacitor \(C_L\) are constant, the circuit equation becomes,

\[
E - V_L = L_d \frac{di}{dt} + \frac{1}{C_L} \int (i_t - I_d) \, dt
\]

and the resulting current \(i_t\) is obtained as follows,

\[
i_t = I_d \left(1 - \cos \omega_t t \right) + \sqrt{\frac{E}{L_d}} \sin \omega_t t
\]

where,

\[
\omega_t = \sqrt{\frac{E}{C_L}}
\]

\[
V_{sw0} = E - V_{CO} \cdot V_L \quad ; \quad V_{CO} \text{ : initial voltage across } C_O.
\]

Hence, the peak-value \((i_{peak})\) of \(i_t\) becomes,

\[
i_{peak} = I_d + \sqrt{\frac{E}{L_d}} \sin \sqrt{\frac{E}{L_d}} V_{sw0}
\]
Current peak Limiting with Saturable Core

Figure 4 illustrates the basic idea of current peak limiting for this series resonant circuit. In the simplified circuit in Fig. 4 (a), the resonant inductance \( L_0 \) is replaced by a saturable reactor (SR) with a biasing current \( I_m \) and the dc inductance \( L_d \) is represented by a constant current source \( I_l \).

The principle of the current pulse limiting is illustrated in Fig. 4 (b). In the characteristic of magnetizing current \( i_s \frac{V}{I_m} \) against flux linkage \( \lambda_m \) in Fig. 4 (a), the gradient of the slope in the saturated region corresponds to the resonant inductance \( L_0 \) \( (L_0 = \frac{1}{\tan \theta}) \) and the non-saturated region offers very high inductance. The current \( I_m \) biases the core of the saturable reactor (= saturable core) in the negative direction to the point "A". When thyristor \( T_h \) is triggered, current \( i_s \) starts flowing and the flux \( \lambda_m \) begins to move from the biased point "A" to saturated region into the unsaturated high inductance zone marked as "B" and the current becomes almost a plateau, suppressed by high inductance and returns to zero again at "A"; the corresponding current wave becomes as shown in the same figure.

For the actual circuit shown in Fig. 5, the magnetizing current \( I_m \) is replaced by \( N_1 I_d \) using tapped winding with winding ratio \( k = \frac{N_1}{N_2} \). The circuit becomes very simple and the magnetizing current \( I_m = N_1 I_d \) is automatically adjusted according to the load variations because \( I_l \) changes in proportion to the average load current. The preferred value for \( k \) is around 2.

Combining with Dual-Flow

In Fig. 6 the current peak limiting circuit is combined with pulse-splitting concept. In Fig. 6 (a), for instance, three inductances are added in series to the output capacitors to perform the pulse-splitting, and the resonating current \( i_s \) flows along the broken lines if positive currents are required for \( i_{sb} \) and \( i_{sb} \). The pulse-split is done by triggering the upper thyristors in the order of phases "a", "b", and "c", while the bottom thyristor in phase "c" should be triggered at the same time as the phase "a" is triggered and being kept in conduction to flow these three currents. The resulting currents are schematically shown in Fig. 6 (b). After \( i_{sb} \) carries the given required amount, \( i_{sb} \) is initiated and the required amount for \( i_{sb} \) is performed, and the circulating current \( i_s \) is initiated after \( i_{sb} \); the required amounts are given from the output voltage errors comparing with references. For this case, phase "c" is used for the circulating purpose, whereas the amount of \( i_{sc} \) is automatically satisfied if \( i_{sb} \) and \( i_{sb} \) are of adequate amounts.

![Circuit configuration with current peak limiting.](image)

Fig. 5. Circuit configuration with current peak limiting.

![Current flow.](image)

(a) Current flow.

![Current pulses.](image)

(b) Current pulses.

Fig. 6. Principles of pulse splitting.
System Control

Overall system diagram

Fig. 7 shows the overall system diagram. The sensor block samples the output voltages \( v_{ab} \), \( v_{bc} \), \( v_{ca} \) and the output control block compares them with sinusoidal reference voltages \( v_{ab}^* \), \( v_{bc}^* \), \( v_{ca}^* \), then decides which thyristors correspond to the first triggering, the second triggering, and the last triggering thyristors as explained in Fig. 6. The delaying angle between the first and the second thyristors is also decided in the control block by using the actual currents sensed by the same block. The control block outputs the firing signals to output converter gate-drive circuit which sends the firing signals to thyristors.

The input converter has the role of controlling both the dc biasing current \( I_d \) and the unity power factor in the input at the same time; \( I_d \) control is done by using \( I_d \) reference \( I_d^* \) which is set around twice of the peak output line current, while the unity power factor in the input is done by selecting the thyristors to flow the current pulses to form the sinusoidal current waveforms synchronizing with the signal from the input phases. The sinusoidal current waveform in the input is performed by using Pulse Density Modulation (PDM) technique by synchronizing the waveform with the input phase voltage.

Selection of triggering phase thyristors

In Fig. 8 the selecting procedure of firing thyristor is again illustrated in detail. The selection begins by sensing output line-line voltages \( V_{ab}, V_{bc}, V_{ca} \) and \( e_{ab}, e_{bc}, e_{ca} \). Comparing them with reference values \( v_{ab}^*, v_{bc}^*, v_{ca}^* \) and \( e_{ab}, e_{bc}, e_{ca} \) are compared with each other. The results of comparison are classified into following two cases depending on the polarity of the maximum error phases:

(i) Maximum error is positive:

The bottom thyristor of lower potential phase in maximum error phases and the upper thyristor of second potential phase are selected to be triggered first. For the second triggering thyristor the upper thyristor of the highest potential phase is selected. The opposite side of the bottom thyristor first triggered is triggered last as a circulating mode thyristor.

(ii) Maximum error is negative:

The upper thyristor of higher potential phase in maximum error phases and the bottom thyristor of second potential phase are selected to be triggered first. For the second triggering thyristor the bottom thyristor of the lowest potential phase is selected. The opposite side of the upper thyristor first triggered is triggered last as a circulating mode thyristor.

An example of the selection is schematically shown in Fig. 8 (a) and (b); the negative maximum error case is in figure (a) and the positive maximum error case is in Fig. 8 (b). The corresponding triggering order of the thyristors are shown in the right.

Above selection strictly depends upon the voltages appearing across the selected thyristors; positive polarity voltage is mandatory for the thyristors to be turned on. Fig. 8 contains both two cases in triggering orders of thyristors classified by line voltage relations.

For numerical examples of voltages showed in the parentheses, the current flows for the first and second triggering are noted in dotted line in the order of I and II. (Circulating modes III are not shown.) For other voltage combinations, dual-flow will be degraded to single flow trimming or to non-trimming primitive method.

![Fig. 7. Control diagram of overall system](image)

![Fig. 8. Examples of selection of triggering phase thyristors for output converter](image)
Results and Discussions

Fig. 9 (a) and (b) shows an example of simulated voltage and current waveforms for induction motor drive with the ratings of 60 Hz, 200v, 0.75kw at a operating condition of 60Hz, 160v, slip s = 3.3%. The waveforms in (a) and (b) are satisfactorily sinusoidal and the resulted torque waveform in figure (c) has almost no fluctuations.

Fig. 10 shows a short interval characteristics; currents i<sub>a</sub>, i<sub>b</sub>, i<sub>c</sub>, and flux linkage \( \lambda_m \) are shown in (a), (b), (c), (d) and (e) respectively. Figure (e) shows the output voltages \( v_{ab} \), \( v_{bc} \), and \( v_{ca} \). Each waveform has regular small ripple and shows smooth variations.

Fig. 11 explains the experimental mono-phase resonant circuit with simple triggering circuit. The triggering pulse is obtained from the opt-coupler when the current \( i_{th} \) becomes enough to light LED to activate the photo-transistor. In that figure, when the thyristor \( T_h \) is triggered, the current pulse \( i_{th} \) forms resonant waveform. During the off state of the thyristor, the dc inductance charges up the capacitor \( C_0 \) and the voltage \( v_{ab} \) across \( T_h \) also increases. The voltage \( v_{ab} \) to light LED is the threshold voltage \( V_{th} \), the adjustment of \( V_{th} \) is done by simply adjusting the series resistor \( R_{op} \).

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Fig. 9. Simulated output voltages, currents, and torque for three phase operation.

Fig. 10. Current pulses and voltages for Fig. 9.

Fig. 11. Experimental circuit and \( v_{ab} \) detection.
The experimentally obtained current pulses at winding factor $k = 1.2$ and $2.2$ are shown in Figs. 12 (a) and (b), respectively. For $k = 1.2$, the clamping level is very low and the pulse frequency $f_p$ is as low as $2.1$ kHz, whereas for $k = 2.2$, the clamping level increases and $f_p = 13.5$ kHz results. As the average current is equal to $I_0$, the duration interval of zero current becomes less than the case of low clamping level. The waveform involves small overshoot at the beginning of the flat-topped region marked "A", because of parasitic oscillations. The reason why the flat-topped region descends to the right seems to arise from partial saturation of the core.

To apply the triggering circuit to the actual three phase ac/ac circuit in Fig. 7, the resistors and the opto-couplers are only placed at the bottom thyristors of various converters in Fig. 13. After the triggering thyristors are selected as shown in black, all of the thyristors except bottom one are triggered (T1, T2, T3) are triggered.) Then the total across voltage which is equivalent to $V_{SW}$ at the monophase circuit in Fig. 11 appears at the bottom thyristor T4. When $V_{SW}$ reaches $V_{Th}$, the signal from opt-coupler is used to trigger thyristors to perform dual-flow trimming.

For the dual-flow trimming utilized, the condition for the trimming is not always possible to be satisfied. During the actual operation, only $30$ percent of the pulses are potential to be dual-flow although the result was better than the case without using dual-flow. For the cases not potential with dual-flow, single flow trimming which utilize the current mode 1 and 3 in Fig. 4(a) was utilized.

For this series resonant circuit the dc biasing inductance and the filter capacitors $C_f$ should have future consideration for reducing the sizes especially for motor drive in competing with PWM inverter. Higher frequency over $100$ kHz seems to be necessary in reducing the sizes and to compete with PWM inverters.

**Conclusion**

The series resonant dc link converter with dual-flow trimming and current peak limiting function was developed. The performance was satisfactory and the current limiting circuit became very simple and the clamping level is automatically adjusted by the load current.

By using the output voltage reference the series resonant dc link can be easily applicable for induction motor drives and the pulse-split with current limiting scheme seems to be extremely useful to the general purpose ac/ac converters in which the output voltage rate is specified and the current reference is not available. Although the feature is the dual of the parallel resonant type (4) with simultaneous current reference, the series resonant-type seems to posses pretty wide feasibility for the future industrial use such as PWM general purpose inverters have.

**References**


**Fig. 13.** $V_{SW}$ detection for three phase practical system.