Current-Clamped, Modified Series Resonant DC-Link Power Converter for a General Purpose Induction Motor Drive

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Abstract—A new ac/ac power converter topology, in which all the switches operate in a resonant fashion to reduce switching losses, is proposed. The topology enables conduction-period control of individual current pulses, whereby pulse-width modulation (PWM) could be achieved to a fair degree of accuracy with the associated controller. The scheme implements current peak (resonant) limiting by a simple diode clamp. Improved switch utilization (voltage \times current) and reduced part-count could be cited as the merits of the circuit over the previous soft-switched current-sourced ac/ac configurations. It is experimentally verified that the output PWM controller could be used to implement constant V/F operation, and the results are presented. In-depth design criteria for the topology that gives optimized voltage stresses are presented. A charge-based, line current feed-forward, mode-controller is introduced at the input and digitally verified. Feasibility of the simultaneous control over both input power-factor and smooth input-output line currents are studied and the digital verification is presented.

Index Terms—Current source, dc link, motor drive, pulse width modulation (PWM), resonant.

I. INTRODUCTION

SOFT-SWITCHING schemes are gaining popularity due to their characteristic feature of markedly reduced switching losses. However, soft-switching ac/ac topologies generally lack duty-ratio control, and the pulse density modulation (PDM) has been the eventual modulation scheme [1], [2]. For a comparable spectral content at the output (and to get rid of sub-harmonic beating) PDM requires much higher switching frequencies compared to pulse width modulation (PWM). The higher switching-frequency requirement could offset the merits of soft-switching converters due to the frequency-dependent loss components.

Increasing power demand from a drive can be achieved most effectively through an increase of output voltage of the feeding inverter system. Current source type converters compete favorably in such cases due to their inherent lower \( \frac{dv}{dt} \) at the output; the merits of lower \( \frac{dv}{dt} \) are that: 1) leakage current in the load (motor) due to stray capacitance is reduced and 2) reduced EMI and eddy current losses. To fully exploit the merits of a current-source power-converter in a high-power system, the soft-switching series resonant dc link power conversion scheme [1] is an attractive alternative.

Several improved versions of the topology can be found in the literature [5]–[7]. However, those topologies either lack full current pulse controllability, are susceptible to high current peaks and voltage stresses, or are of higher part-count or possess a combination of limitations thereof. At this point in time, it would be appropriate to give a brief run-down on each of the previous topologies and the new topology.

Topology [5] offers an attractive time sharing pulse-splitting scheme that helps to improve the pulse controllability. The limiting factor is that the conducting width of a current pulse for a phase cannot be controlled over each and every pulse. Topology [6] has made a breakthrough by adding the conduction period controllability to the topology; but the minimum pulse-width and the resonant current peaks seen by the bridge devices are compromised. Topology [7] facilitates conduction period controllability and resonant current peak clamping for reduced current stresses. The drawbacks are that the auxiliary-thyristor bridge sees higher resonant current peaks and voltage stresses (as high as five times the output voltage-peak), and that the part-count (device number) of the topology is high. The proposed topology (new topology in Fig. 1) performs resonant-current clamping and conduction-period control (PWM) only by means of an extra thyristor-diode set. It does not use any dedicated devices for start-up. PWM capability, once achieved, enables much lower switching-frequency operation than with the PDM operation, and yet obtains almost comparable spectral performance compared with a hard-switched, current-source converter [3]. Hard-switch operation reaches the thermal-limit at much lower switching frequencies. The experimental results of the hard- and soft-switch comparison [4] on GTO show that, as high as twenty-fold (20:1) frequency gain could be achieved with the soft-switch operation. Therefore, with the availability of PWM in this topology, the "wide switching frequency availability" could be exploited for much better spectral content.

A. Overview of the Proposed Power Converter and Control Possibilities

The proposed ac/ac power-converter topology is drawn in Fig. 1. It generates unity power factor smooth line currents at the input and variable frequency, harmonically optimized sinusoids at the output. Typical current-pulses seen by bridge thyristors are represented as pulse-current \( i_s \) in Fig. 1. These pulses are distributed among phases to synthesize reference sinusoids. The width of the current pulses \( i_s \) is adjustable,
B. Circuit Description

Input line impedance $L$ and small filter capacitors $C_f$ in Fig. 1 constitute the low-pass filter at the input, whereas, motor leakage inductance and $C_f$ form the filter at the output. $C_f$ is selected in such a way that vars drawn by it at the fundamental frequency is negligible [8]. Small inductance $L_{0a}$, $L_{0q}$ and the capacitor $C_0$ form the resonant circuits. In addition to being a current source of current $I_d$, the inductor $I_{d_0}$, $I_{Q0}$ plays the role of the energy balancing element of the dc link. The input-bridge supplies positive and negative voltage pulses at the input to maintain the average current in $I_d$ at the given reference $I_{d,ref}$ (positive voltage pulses increase $I_d$, and negative voltage pulses decrease $I_d$); moreover, the input bridge synthesizes unity power factor line currents. Diode “D” is the clamping device that clamps the resonating current $i_s$ flowing into the load at the level of $I_d$ (current in $I_d$). The auxiliary thyristor “$T_{aux}$” adjusts the pulse-width of $i_s$.

II. PRINCIPLE OF OPERATION

A. Equivalent Circuit

Filter capacitors $C_f$ are considered to be constant voltage sources over the period of a single current-pulse of $i_s$, because $i_s$ is of higher frequency compared to the input and output waveforms. Therefore, for analytical purposes, the monophase equivalent circuit can be drawn as shown in Fig. 2(a). Note that the four thyristors in black in Fig. 1 are a set of thyristors conducting in series to generate a current pulse $i_s$; the four thyristors are lumped in to a single thyristor $T_{equ}$, as shown in Fig. 2(a). $E$ and $V_o$ represent the input and output voltages, respectively. Principle of the circuit operation has been explained by means of five circuit states drawn in Fig. 2(b), where the thick black lines represent the current path for each case. Note that the circuit states are plotted in time domain, in the topmost trace of Fig. 3(a), together with their current waveforms.

B. Current Pulse Generation

1) State 1: Assume that a dc current of value $I_d$ exists in the inductor $L_d$. Fig. 2(b) represents the state-1, where all the thyristors are off and $D$ conducting and $I_d$ circulates charging $C_0$ up linearly. Traces 5 and 6 of Fig. 3(a) represents the voltage variations across $C_0$ and $T_{equ}$, respectively. As $C_0$ gets charged up, the forward voltage of $T_{equ}$ $V_{set}$ builds up until it reaches a defined threshold $V_{thm}$ at $t_0$, as shown in Fig. 3(a), trace 6.

2) State 2: State 2 is illustrated in Fig. 2(b) ($T_{equ}$, $D$ conducting). At $t = t_0$, when $V_{set} = V_{thm}$, $T_{equ}$ is gated on. Change in $I_d$ ($di_d/dt \approx 0$) is neglected, whereupon, the voltage equation around the loop [see Fig. 2(a)] for the loop yields

$$E - V_o = (L_{0a} + L_{0q}) \frac{di_s}{dt} + \frac{1}{C_0} \int (i_s - I_d)dt \quad (1)$$

and the current $i_s(t)$ becomes

$$i_s = L_d(1 - \cos \omega_0 t) + \frac{V_{set}(t_0)}{Z_0} \sin \omega_0 t \quad (2)$$

where

$$Z_0 = \sqrt{\frac{L_{0a} + L_{0q}}{C_0}}$$

$$\omega_0 = \sqrt{\frac{1}{(L_{0a} + L_{0q})C_0}}$$

$i_s$ is of resonant nature and starts growing at $t_0$, as shown in Fig. 3(a), trace 1. The node 2 in Fig. 2(a) gives the current relation

$$I_d = i_s + I_{d0} \quad (3)$$

$I_d$ is constant, therefore, to make up for the increasing $i_s$, $I_{d0}$ starts falling and goes to zero at $t_r$, turning the $D$ off where $i_s$ gets clamped at $I_d$ to satisfy (3), as shown in Fig. 3(a) trace 1.

3) State 3: Fig. 2(b) [$T_{equ}$-on] represents the State 3 ($T_{equ}$-on). The clamped $i_s$ continues to flow through the load as a flat-topped current pulse $(i_s = I_d)$, the width of which is controllable. State 3 is considered to be the powering mode of the converter.
4) **State 4:** The State 4 is drawn in Fig. 2(b); $T_{aux}$ is turned-on to reverse the polarity of $C_0$. The resonant circuit for the case is formed by $C_0$ and $L_{01}$. Depending on the polarity of $V_o$, State 4 takes on two sub-states. Currents for $V_o < 0$ are drawn in Fig. 3(a). When $T_{aux}$ turns on at $t_3$, $i_d$ starts to flow, but the diode $D$ continues to be off because of the reverse voltage being applied [see Fig. 2(b)]. $T_{aux}$ turns-off at $t_2$, having reached the current zero [see Fig. 3(a) trace 4]. $i_s$ for $V_o > 0$ is shown in Fig. 3(b). Until the time $t_1$, every bit of the current waveforms is as same as for the case $V_o < 0$. Now $T_{aux}$ is turned-on at $t_1$, where $D$ and $T_{aux}$ start conducting. $i_s$ linearly goes down by $\Delta i_s$, which makes $\dot{i}_{dl} = +\Delta i_s$ [see (3), $I_d$ constant]. $i_0$ grows and reaches $-\Delta i_s$ at $t_4$, where $i_{aux} = i_{dl} + i_0 = 0$ and $T_{aux}$ turns off.

5) **State 5:** Soon after $T_{aux}$ has turned-off at $t_2$ (or $t_4^*$, depending on the previous state), State-5 [Fig. 2(b)] begins. The reversed $C_0$ forward bias $D$ at $t_2$. The energy trapped in $C_0$ [see Fig. 3(a) trace 5 for capacitor voltage] and $L_{02}$ re-excite the tank of $C_0$ and $L_{01} + L_{02}$. The current $i_{dl}$ starts to grow toward $I_d$, and $i_s$ starts reducing to satisfy the current equation at node-2 ($I_d = i_{dl} + i_s$). $i_s$ reaches zero at $t_3$, whereby $T_{equ}$ turns-off marking the end of a cycle and the State 5.

### III. Power Circuit Design/Pulse Stability

**A. Pulse Stability**

Pulse stability analysis requires the knowledge of the peak of $i_{dl}$ and $i_{aux}$, and the maximum possible voltage stresses of the devices. In the State 1, $I_d$ charges $C_0$ linearly up until $t_{0-}$, just before the turn-on of $T_{equ}$ at $t_0$. The voltage across
The equation for $V_{thm}$ at $t_{o}$ is $V_{thm}$, therefore, the voltage of $C_{0}$ at $t_{o}$ can be expressed as

$$V_{0}(t_{o}) = V_{thm} + V_{0} - E.$$  \hfill (4)

Fig. 3(a), trace 5, shows that the State 2 further charges $C_{0}$ in a resonant manner until $t_{r}$, where $\dot{i}_{x}$ reaches $I_{d}$. The additional charge put in to $C_{0}$ during the State 2 is $\Delta Q$; it is represented by the shaded area in trace 1 and 2 of Fig. 3(a). The voltage of $C_{0}$ at $t = t_{r}$ turns out to be

$$V_{0}(t_{r}) = V_{thm} + V_{0} - E + \frac{\Delta Q}{C_{0}}.$$  \hfill (5)

$V_{0}(t_{r})$ becomes a transcendental function; to make the mathematics simpler, it is assumed that $\dot{i}_{x}$ increases linearly from $t_{o}$ to $t_{r}$ at the rate $(\dot{i}_{x} / dt)_{o}$, and the shaded area $\Delta Q$ in Fig. 3(a) is treated triangular. The Appendix deals with the derivation of $\Delta Q$.

1) Selection of $Z_{0}$: $Z_{0}$ is the characteristic impedance of the tank formed by $S_{0}$ and $L_{01} + L_{02}$. Consider the State 5, which begins by turning $D$ on at $t_{2}$; when $V_{o} < 0$, it gives the worst case for $D$ to excite the tank at $t = t_{2}$, therefore, it brings in the weakest $\dot{i}_{dd}$ growth of the circuit and the minimal potential peak of $i_{dd}$ (i.e., $i_{peak}$). During the State 5, for $\dot{i}_{x}$ to reach zero and turn $T_{eq}$ off, $\dot{i}_{dd}$ should at least grow up to be $I_{d}$ ($= i_{dd} + \dot{i}_{x}$). The point “W” in Fig. 3(a) trace 3 shows the potential peak (which is reachable if and only if $T_{eq}$ allows reverse current). It yields the following inequality:

$$\left(i_{dd}\right)_{peak} \geq I_{d}.$$  \hfill (6)

Substituting for $(i_{dd})_{peak}$ in (6), arranging terms, and defining the function $Y$ would yield

$$Y \geq \left(\frac{I_{d}^{2}}{2V_{thm}}\right)Z_{0} - (I_{d})Z_{0} - 2|V_{o}| + V_{thm} \geq 0.$$  \hfill (7)

Fig. 4(a) and (b) graph the function $Y$ for specifically identified boundaries of $V_{thm}$, marked on the top of each plot. Circuit operation maintains $V_{thm} > 0$, therefore, $(I_{d}^{2} / 2V_{thm}) > 0$ and $Y$ has a minimum at $Z_{0} = V_{thm} / I_{d}$. The range of $Z_{0}$ satisfying (7) can be written as

$$Z_{0} > \frac{V_{thm}}{I_{d}} \left(1 + \sqrt{\frac{4|V_{o}|}{V_{thm}} - 1}\right).$$  \hfill (8)

$$Z_{0} < \frac{V_{thm}}{I_{d}} \left(1 - \sqrt{\frac{4|V_{o}|}{V_{thm}} - 1}\right).$$  \hfill (9)

The range of $Z_{0}$ for each case is marked in thick line on the $Z_{0}$ axis. The condition $V_{thm} > 4|V_{o}|$ [Fig. 4(a)] yields no real solution for $Y = 0$; therefore, regardless of the value of $Z_{0}$, the system is stable, for (7) is satisfied for any $Z_{0}$. But, $V_{thm} > 4|V_{o}|$ is not practically viable because it yields elevated voltage stresses across $T_{eq}$. The condition $2|V_{o}| < V_{thm} < 4|V_{o}|$ [Fig. 4(b)] makes the two roots of $Y$: $Z_{1}$ and $Z_{2}$ positive, and yields two discrete solution ranges for $Z_{0}$: $2|V_{o}| < V_{thm} < 4|V_{o}|$ gives an important boundary for $V_{thm}$, because it satisfies the condition $V_{thm} \simeq 2|V_{o}|$, which gives the minimal voltage stress point of the converter (see Section III-B). The range marked sol. 2 given by (9)

is preferable, because it yields a smaller $Z_{0}$ and, therefore, smaller $L_{01} + L_{02}$ can be used.

a) How to find the smallest $Z_{0}$: $V_{thm}$ is a defined parameter. $I_{d}$ and $|V_{o}|$ are varying, but the peaks of $|V_{o}|$ and $I_{d}$ are known. From (9), it follows that the largest possible $I_{d}$ and $|V_{o}|$ yield the lowest $Z_{0} (= Z_{2})$; $Z_{0}$ should lie to the left of $Z_{3}$ for the stability.

2) Selection of $Z_{01}$: The tank of current $i_{aux}$ is formed by $L_{01}$ and $C_{01}$ of characteristic impedance $Z_{01}$. $i_{aux}$ creates a resonant peak, but the rms value is quite low due to the lower duty ratio of $i_{aux}$. However, it is important to minimize the peak of $i_{aux}$ to reduce the volume of core and copper. The peak excursion of $i_{aux}$ that the designer contend to deal with is taken to be $I_{wish}$. Note that $i_{o}$ flows as the excitation of the tank occurs at $t_{2}$. The worst case of current $i_{aux}$ results when $V_{o} > 0$, because $D$ and $T_{aux}$ conduct together for a while, and the additive current $i_{dd}$ shows up in $i_{aux}$ ($= i_{o} + i_{dd}$). The peak of $i_{aux}$ is $(i_{aux})_{peak}$, which should be limited to $I_{wish}$, which yields $(i_{aux})_{peak} \leq I_{wish}$; it can be written as

$$i_{o} + I_{d} \leq I_{wish}.$$  \hfill (10)

Substituting values and arranging terms, (10) is simplified to

$$Z_{01} \geq \frac{|V_{o}| + V_{thm} + \frac{R}{2V_{thm}}}{I_{wish} - I_{d}}.$$  \hfill (11)

Substituting for $I_{wish}$ and $V_{thm}$, and assuming that in the denominator $I_{d}$ is comparably smaller, i.e., $I_{th} = I_{d} \approx I_{d}$, the worst case $Z_{01}$ is calculated; maximum $|V_{o}|$ and $I_{d}$ in the numerator gives the worst case $Z_{01}$.

3) Selection of $C_{0}$: Fig. 5 graphs the blown-up tail-end of $\dot{i}_{x}$ and the voltage across $T_{eqv}$, $V_{thm}$. The circuit commutated turn-off time of the thyristor, $T_{eqv}$, is marked at $t_{s}$. As soon as the storage time $t_{s}$ has elapsed, a reverse voltage of $V_{thm}$ will appear across $T_{eqv}$. After the time $t_{s}$, $T_{eqv}$ is blocking and the circuit is practically in State 1; $C_{0}$ gets charged by $I_{o}$ at the rate given by $I_{d} / C_{0}$ [see Fig. 2(b) □]. The ramps “AB” and “AD” in Fig. 5 signify different charging profiles that could result due to the use of different $C_{0}$ values, namely $C_{11}$ and $C_{02}$ ($C_{02} > C_{11}$). With $C_{01}$, the smaller of the two, voltage across the device takes on the curve “AB,” whereby the cross-over of the device voltage to the positive region occurs as fast as at point B. As seen, point B yields $t_{x} < t_{q}$, and the

![Graph showing solution range of $Z_{0}$ for $V_{thm}$](image-url)
device has not yet recovered, therefore, it cannot hold up the positive voltage by premature cross-over; therefore, forward recovery current would flow, and should the peak of which exceed the latching current, the device will prematurely turn-on. The premature turn-on could possibly cause instability because of the inadequate time to exist across at the turn-on. Therefore, the time should always be greater than for the stability and it can be expressed as follows:

\[ t_x \geq t_q \tag{12} \]

Considering the fact that \( I_d \) is constant, time \( t_x \) can be written as \( t_x = C_0 V_{thm}/I_d \); substituting for \( t_x \) in (12) and arranging terms

\[ C_0 \geq \frac{t_q \cdot I_d}{V_{thm}}. \tag{13} \]

Equation (13) shows that a bigger \( I_d \) contributes much to the problem; therefore, \( C_0 \) selection uses the largest \( I_d \).

**B. Is There an Optimum \( V_{swt} \)?**

\( V_{swt} \) is the voltage across \( T_{equ} \), which turns-on for each pulse should the voltage across it exceed a defined threshold \( V_{thm} \). Fig. 6(a) represents two consecutive current pulses of \( i_s \), \("(n-1)"\) and \("n."\) The pulse "\(n-1"\) ends at \( t_3 \), turning the old \( T_{equ} \) off. New phases and \( T_{equ} \) are selected at \( t_{3+} \) to form the next pulse "\( n."\). The voltage across the new \( T_{equ} \), and the resultant voltage change around the loop [see Fig. 2(a) for the loop] are drawn in Fig. 6(b) and (c), respectively. Note that the input and output voltages of the converter (\( E \) and \( V_o \)) vary as the switches connect between different input and output phases; therefore, at time \( t_{3+} \), \( V_{swt} \) could go beyond the defined-\( V_{thm} \) due to the resultant voltage of the phase change, \( \Delta V \). The worst case \( V_{swt} \) (voltage across \( T_{equ} \)) is important, because it dictates the switch voltage-rating. Fig. 6(b) shows that for \((n-1)\)th pulse \( T_{equ} \) has a voltage of \( V_{thm} \) at \( t = t_{3-1} \) a moment before its turn-on at \( t_0 \). As modes go on, \( T_{aux} \) turns-on at \( t_1 \) (see Fig. 3 for details), reverses the voltage of \( C_0 \), and turns off at \( t_2 \). Now the voltage of \( C_0 \) at \( t_3 \) can be written as

\[ V_{CO}(t_2)_{n-1} = -E_{n-1} - V_{on-1} - V_{thm} - \frac{\Delta Q}{C_0}. \tag{14} \]

\( n-1 \) in the subscript depicts that the quantity belongs to \((n-1)\)th current pulse. In between \( t_2 \) to \( t_3 \), \( C_0 \) is charged additionally by \( \Delta Q \) (see Fig. 13, Appendix for \( \Delta Q \)), and the voltage of \( C_0 \) at \( t_3 \) can be written as

\[ V_{CO}(t_3)_{n-1} = -E_{n-1} - V_{on-1} - V_{thm}. \tag{15} \]

The switch voltage across the new \( T_{equ} \) at \( t_{3+} \) can be written as

\[ V_{swt}(t_{3+})_n = -E_n - V_{on} + V_{CO}(t_3)_{n-1} \tag{16} \]

where, the subscript “\( n \)” represents the fact that the quantity belongs to \( n \)th pulse. Substituting values for voltage of \( C_0 \) in (16):

\[ V_{swt}(t_{3+})_n = (E_n-V_{on}-(E_n-1+V_{on-1}+V_{thm})), \tag{17} \]

The peak of the output and input voltage is assumed to be \( V_{jk} \). Then the largest possible forward \( V_{swt}(t_{3+})_n \), which appears across the new \( T_{equ} \) at \( t_{3+} \), turns out to be

\[ V_{swt}(t_{3+})_n = 4V_{jk} - V_{thm}. \tag{18} \]

Fig. 7 graphs the relation (18). Arrows indicate how the selected \( V_{thm} \) for \((n-1)\)th pulse, i.e., \( V_{thm,n-1} \), would bring about maximum \( V_{swt}(t_{3+})_n \) for the \( n \)th pulse. If \( T_{equ} \) is fired at \( V_{thm} \) given by the point-1, the next pulse could see a forward voltage given by the point-2 that translates to the voltage at point-3 on \( X \) axis; now if \( T_{equ} \) is fired at \( V_{thm} \) given by point-3, the next pulse would see a voltage given by point-4. Two important points drawn out of above observation are:

1. If started from a point to the right of “\( X \)” (i.e., point-1, Fig. 7), the worst case forward voltage for the next pulse turns-out to be to the left of “\( X \)” (i.e., point-3), hence time is available for \( C_0 \) to get charged up and bring the threshold at point-3 up to the threshold at point-1. The time availability is important, because it gives recovery time, \( t_q \), for the old \( T_{equ} \) to turn-off, and time for \( V_{swt} \) to reach \( V_{thm} \) to fire the new \( T_{equ} \).

2. If \( V_{thm} \) at “\( X \)” (\( V_{thm} = 2\sqrt{V_0} \)) is used, the next pulse, in the worst case, would see the same optimized voltage given by “\( X \)” In practice, to allow for switch recovery, optimum \( V_{thm} \) lies slightly away from “\( X \)” to the right of it.

**IV. CONTROL STRATEGY**

The proposed circuit has a single commutation circuit formed by \( L_01 \), \( L_02 \), and \( C_0 \) for all bridge thyristors. Therefore, the pulse-width available at the input and output bridges are the same. Control criterion presented hereon deals with
A. Input Converter Control

Input converter serves two purposes: it regulates the current in \( I_d \) to form a current-source and synthesizes sinusoidal line currents at a given power factor. To match the input and output power drawn by the circuit, input line-currents are drawn in a controlled manner, and the system is said to implement “power feed forward.” Power feed forward minimizes \( I_d \) fluctuations, whereby the involvement of line current in the \( I_d \) regulation is minimized, and better line currents are obtained. Instantaneous input and output power matching is not possible at the bridge terminals. To clarify the fact readers are urged to refer to the Fig. 2(b) [3], the powering state of the converter. Current \( I_d \) is passing through the input and output bridge terminals, and the power at the respective terminals calculates to be \( E \cdot I_d \) and \( V_o \cdot I_d \). Since the input and output voltages are of different frequency and amplitude, it is unlikely that the above two quantities be equal. The mismatch in instantaneous power renders \( I_d \) a linear change, at the rate given by \( E - V_o/I_d \), within a current pulse; but the average power can be matched and the average of \( I_d \) can be maintained at the reference level. \( I_{d,\text{ref}} \). Fig. 8(a) represents the block diagram of the input controller. “L” in Fig. 8(b) represents the line-inductance of impedance \( X_L \). Phasor diagram for the input filter is drawn in Fig. 8(c); phasors are marked in bold with a bar on top. Subscript in the voltages represents the points, which the voltages belong to (ex. \( V_{a*} \) at point \( A^* \)).

The power calculator derives the active and reactive Power [9] as follows:

\[
P_{\text{out}} = v_d i_d + v_q i_q
\]
\[
Q_{\text{out}} = v_d i_q - v_q i_d
\]

where \( d \) and \( q \) represent the DQ components of the motor (load) voltages and currents; \( P_{\text{out}} \) is the instantaneous active power, and \( Q_{\text{out}} \) is instantaneous reactive power. \( P_{\text{out}} \) is referred to the utility terminal to find the basic reference line currents [i.e., \( i_{a*,in} \) for phase A, Fig. 8(a)] of input frequency. Then, the reference is further modified using the gain factor, \( K^* \), to compensate for \( I_d \) variations, and the final set of reference-currents (i.e., \( i_{a*,\text{ref}} \) for line A) is derived. Next the current reference is fed forward and the reference voltages (i.e., \( V_{a*,\text{ref}} \) for phase A) at the terminals \( A^* \), \( B^* \), and \( C^* \) are generated.

1) Input Switch Selection—Mode Controller: Amount of charge drawn by the converter terminals \( A^* \), \( B^* \), and \( C^* \) over the shaded current pulse in Fig. 8(d) is marked by \( \Delta Q_a \), \( \Delta Q_b \), and \( \Delta Q_c \), respectively, in Fig. 8(b); the average currents drawn by the terminals \( A^* \), \( B^* \), and \( C^* \) during the period “T” translated to be \( \Delta Q_a/T \), \( \Delta Q_b/T \), and \( \Delta Q_C/T \), respectively. Fig. 8(d) represents the reference voltage \( V_{a*,\text{ref}} \) and its actual voltage trajectory of \( V_{a*} \) over the period \( T \). Point “P” in Fig 8(d) represents where the actual voltage lies just before the shaded current pulse occurs; the voltage error at “P” is marked as \( \Delta V_1 \). The intention of the controller is to make the local voltage-average of each line equal to the respective reference voltages. Point “Q” represents where the trajectory of \( V_{a*} \) should end for local average of it (over the period \( T \) to become equal to the reference \( V_{a*,\text{ref}} \); as the voltage trajectory moves along “PQ” and reaches the point \( Q \), it is said that a voltage error of \( \Delta V_1 \) [see Fig. 8(d)] is fully compensated. Therefore, in the process the charge drawn by \( C_f \) connected to phase \( A^* \) can be written as \( C_f \cdot \Delta V_{a*} \); line current \( i_a \) is sinusoidal and assumed constant over the
period $T$, therefore, the charge supplied by the line over the period $T$ would become $i_d T$. Now, the charge flow at point $A^b$ in Fig. 8(b) yields

$$i_d T = C_f \cdot \Delta V_{a'} + \Delta Q_a$$  \hfill (20)  
$$i_d T = C_f \cdot \Delta V_{b'} + \Delta Q_b$$  \hfill (21)  
$$i_d T = C_f \cdot \Delta V_{c'} + \Delta Q_c.$$  \hfill (22)

Since there is no neutral conductor, the following relation holds true:

$$\Delta Q_a + \Delta Q_b + \Delta Q_c = 0.$$  \hfill (23)

Equation (23) depicts that the three charge quantities always yield a charge set of mixed (both + and − polarity). The direction of charge flow is such that, for instance, if $\Delta Q_a$ is positive then charge is flowing in to the converter in the same direction shown in Fig. 8(b); therefore, the upper thyristor on the arm $A^*$, $T_{A^+}$, must be conducting, whereas, If $\Delta Q_a$ is negative charge flow is in the opposite direction to that shown in Fig. 8(b), and the bottom thyristor $T_{A^-}$ should be conducting. Table I summarizes the selection criterion for the input bridge thyristors. “+” and “−” in the table represent the polarity of the charge quantities $\Delta Q_a$, $\Delta Q_b$, and $\Delta Q_c$. It follows from the above explanation that “+” and “−” necessarily represent top and bottom thyristors, respectively. Based on the polarity of $\Delta Q_a$, $\Delta Q_b$, and $\Delta Q_c$ six unique patterns can be distinguished, which are treated as current vectors in row one through six in Table I. However, the converter proposed in the paper is a current source type that in general permits the selection of two switches from the input bridge at a time. Given the above constraint, each of the six vectors could be sub-divided in two vectors. The division is carried out depending on the magnitude of the charge quantities; for clarification of the fact note that the vector 1 has sub-divisions depending on the inequality $\Delta Q_a \leq \Delta Q_b$. The selected thyristors for each sub-row are tabulated in the last column of the Table I. The thyristors relevant to maximum and minimum charge quantities are selected for firing; for instance, first row of vector-1 shows the relation $\Delta Q_b > \Delta Q_a > \Delta Q_c$. Note that $\Delta Q_c < 0$ and $\Delta Q_b > 0$. Accordingly, thyristors in black in Fig. 8(b), marked $T_{B^+}$ and $T_{B^-}$, is the selection.

### B. Output Converter Control

Output converter implements a PWM controller with a minor $I_q$ regulation loop and a major voltage feed back loop. A zero current vector compensation scheme is also adopted.

1) **PWM method**: Fig. 9(a) shows two phasor sets, 30° shifted to each other, namely the set $\bar{I}_a$, $\bar{I}_b$, $\bar{I}_c$, and $\bar{I}_x$, $\bar{I}_y$, $\bar{I}_z$. The latter is the modulating phasor set; note that Fig. 9(c) shows the PWM pulses for the phasor $\bar{I}_x$. $\bar{I}_a^*$, $\bar{I}_b^*$, and $\bar{I}_c^*$ are assumed to be the time domain representation of the phasors $\bar{I}_a$, $\bar{I}_b$, $\bar{I}_c$, and $\bar{I}_x$, $\bar{I}_y$, $\bar{I}_z$. One of the three sinusoids, $\bar{I}_a^*$, $\bar{I}_b^*$, and $\bar{I}_c^*$ would necessarily yield the lowest instantanous voltage of the three over a period of 120°. Noting the above fact, $\bar{I}_a^*$, $\bar{I}_b^*$, and $\bar{I}_c^*$ are re-drawn in the time domain as difference-sinusoids (i.e., $\dot{I}_a^* - \dot{I}_b^*$ etc.) in Fig. 9(b). For instance, in Fig. 9(b), between points $\Theta$ to $\Omega$, $\dot{I}_a^*$ becomes the minimum of the three; therefore, two current profiles $\dot{I}_a^* - \dot{I}_b^*$ and $\dot{I}_a^* - \dot{I}_c^*$ (termed difference-sinusoids) are drawn making $\dot{I}_a^*$ the base. In between $\Theta$ to $\Upsilon$, triangular carrier crosses $\dot{I}_a^* - \dot{I}_b^*$ at “M” and $\dot{I}_a^* - \dot{I}_c^*$ at “N.” The length thus formed,
TABLE I

<table>
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<tr>
<th>Method of Input Switch Selection</th>
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<td>vector</td>
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</table>

\( MN \), is equivalent to \( i_{zf} = i_{zf}^* \); therefore, \( MN \) is used to generate the pulse \( \hat{1} \) of the current \( i_x \) as shown in Fig. 9(c). The zero current vectors are shown in Fig. 9(c). These vectors represent the region where there are no \( i_{zf}, i_y, \) and \( i_z \) (see Fig. 1) flowing, and therefore the region where no power is supplied to the load.

2) Zero Vector Compensation: The converter cannot stay in the State-1 indefinitely, for voltage in \( C_0 \) could rise to prohibitively bigger values; for simplicity of implementation, the time that the converter spends in State-1 is taken to be the time it takes voltage across \( T_{eq} \) to reach the defined threshold \( V_{thm} \). Therefore, exact zero-vector duration cannot be satisfied by the State-1 alone. To lengthen the time it spends in zero vector, a circulation mode is activated by turning on both thyristors on one arm (i.e., \( T^+_A, T^-_A \), Fig. 1) of the output bridge.

3) Control Method: This is targeted at voltage/frequency control; the block diagram of control for phase \( X \) can be found in Fig. 10. A PWM pulse pattern for sinusoidal current and a sinusoidal voltage reference, stored in a ROM, are used in this method. In the scheme PWM current pattern is used to turn-on the switches, and then the resulted output voltages \( V_x, V_y, \) and \( V_z \) at the terminals \( X, Y, \) and \( Z \) are used to generate a synchronized three-phase voltage reference using the ROM data. The generated voltage reference is compared with the actual voltages to generate the voltage errors (i.e., \( \Delta V_x \) for phase \( X \)). As seen, error voltage \( \Delta V_x \) and the factor given by \( I_q \) regulation loop, \( K^* \), is used to find \( K_{out} \), which modifies the duty factor of the ROM data for current of phase \( X \).

C. Digital Implementation of the AC/AC System

The controller is implemented using “ACSL” software [10] on “hprise” workstation. Fixed calculation step size of 0.02 \( \mu S \) is used with the fourth-order “Runge–Kutta” algorithm for integration. Voltage behind the transient reactance is used to model the motor (4 kW). The digital simulation results can be found in the Fig. 11. It depicts that fairly good line currents of unity power factor and smooth motor currents are feasible with smaller fluctuations in \( L_d \).

D. Experimental Implementation

Although a conventional \( j \)controller would be enough to perform the controller requirement, the DSP TMS320C25-based development-system, available at the laboratory, is used in the implementation. Characteristic data for the prototype can be found in Table II. Fig. 12 shows the experimental waveforms; as seen the method yields smooth waveforms. A 30-\( \Omega \) resistor load is kept in parallel with the induction motor. The response of the system for a command-voltage change of 0–90 V, at \( f = 30 \) Hz is captured in Fig. 12(d); as seen the controller successfully responds to the change in commanded voltage.

V. PWM LIMITS

A. The Highest Possible Pulse Frequency

Maximum pulse-frequency of the converter depends on two factors: the minimum conducting width of a current
pulse, i.e., the total minimum time the converter spends in modes 3 and 4 (see Fig. 3), and the minimum turn-off time requirement for \( T_{equ} \) to recover, i.e., the time \( t_q \) in Fig. 5. It is assumed that in Fig. 3(a), the length \((r - t_0)\) and \((t_3 - t_2)\) are negligible compared to \(t_1\), which is the width of the \( i_{aux} \). Accordingly, the minimum conducting period occurs when \( t_1 \) reaches \( t_r \). By substituting values from Table II:

\[
\text{Max. Pulse Frequency} = \frac{1}{t_2 - t_1 + t_q} \\
= \frac{1}{\pi \sqrt{L_0 C_0 + t_q}} \\
= 38.6 \text{ kHz.} 
\]

(24)

### B. Current Bus Usage/Limit of Modulation Index

In Fig. 14, A and B are the magnitudes of the carrier and the reference-current, respectively. Fig. 14(b) represents the portion of an exaggerated reference current and the carrier. The carrier used in the prototype is 1.5 kHz, which yields a period of 667 \( \mu \text{s} \). Therefore, the time-\( \lambda \) spend by the carrier in traversing a length of \((A-B)\) is given by

\[
\lambda = \left(1 - \frac{B}{A}\right) \cdot \frac{667}{2}. 
\]

(25)

The zero-vector implementation is achieved by the arm shorting as explained earlier; therefore, the shortest period that can be implemented by such vectors is dictated by the minimum pulse width of a current pulse and the thyristor turn-off time \( t_q \). Note also that the full zero vector duration is given

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**Fig. 10.** V/F control by PWM current pulses.

**Fig. 11.** Simultaneous control of line current, motor current, and biasing current (digital simulation results).
Substituting (25) in (26), and arranging terms

\[ 2\lambda \geq \pi \sqrt{L_{q1}C_0} + t_q. \]  

Substituting \( \lambda \) from (25) in (26), and arranging terms

\[ \frac{B}{A} \leq 1 - \left[ \frac{\pi \sqrt{L_{q1}C_0} + t_q}{607} \right] \cdot \frac{1}{607}. \]  

Substituting values from Table II, the modulation index \( B/A \) turns out to be

\[ \frac{B}{A} \leq 0.99. \]  

The minimum value of \( B/A \) depends on the minimum conduction-period of a pulse. With the time taken by the carrier to traverse a distance \( B \) (see Fig. 14 for min. \( B \)), it can be derived

\[ \frac{607 \cdot B}{A} \geq \pi \sqrt{L_{q1}C_0}. \]  

Substituting values from Table II, \( B/A \geq 0.02 \). Allowing a safety margin, the range of \( B/A \)

\[ 0.9 \geq \frac{B}{A} \geq 0.03; \quad \text{carrier} = 1.5 \text{ kHz}. \]  

VI. CONCLUSION

The topology is easy to operate and of smaller part count; therefore, it constitutes an economically viable system. The PWM control algorithm presented is found to be very effective and gives quite satisfactory output current and voltage spectral performance. Moreover, with a current source converter the \( V/F \) operation has been successfully implemented.

The line-current feed-forward, charge-based, mode controller is robust and does not excite \( L_C \), \( C_f \) oscillations.

The fact that there exists a particular voltage \( V_{thm} \) across the equivalent thyristors \( T_{eq} \), that gives an optimal voltage stress per switch is identified. The design criterion and voltage optimization method introduced could be easily adopted in the design of resonant converters of the family [1], [5]–[7].

Fig. 12. Experimental results (\( f = 30 \text{ Hz} \)). (a) Motor voltage and current, (b) motor voltage and PWM current pulses, (c) current waveforms of the topology, and (d) dynamic performance for reference voltage change.
Fig. 13. Derivation of $\Delta Q$.

(a) Current reference.

(b) Illustrations for PWM limits.

APPENDIX

A. Derivation of $\Delta Q$

Taking derivatives with respect to time on both sides of (2), the rate of change of $i_s$ at $t = 0$:

$$\tan(\theta) = \left(\frac{d\theta}{dt}\right)_{t=0} = \frac{V_{thm}}{L_0 + L_0 \omega_0} = \frac{V_{thm}}{C_0 \cdot Z_0^2}.$$  (31)

From Fig. 13, area of the triangle $GHI$ is equal to $\Delta Q$: it could be derived as follows:

$$GH = \frac{IH \tan(\theta)}{1} = \frac{I_d \cdot C_0 \cdot Z_0^2}{V_{thm}}.$$  (32)

$$\Delta Q = \frac{I_d^2 \cdot C_0 \cdot Z_0^2}{2 \cdot V_{thm}}.$$  (33)

B. Expressions for Currents

$$i_d = \frac{2V_o + V_{thm} + \frac{I_d^2}{2} (L_0 + L_0 \omega_0)}{2V_{thm} C_0} \sin(\omega_0 t);$$

$$V_o < 0,$$

(35)

REFERENCES


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