A, B	Peak value of the flux in cores 1 and 2.
$\hat{V}_1, \hat{V}_2$	Peak value of input and output voltages.
C	Tuning capacitance.
ω	Angular frequency.
δ	Phase angle between the two core fluxes.
i_1, i_2	Current in input and output windings.
P_{12}	Parametric power transferred from input to output.
i	Load current.
R	Load resistance.

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Simulation of a Current Source Inverter Drive

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Abstract—**A novel simulation of a current source inverter is developed which retains the effects of commutation but minimizes the number of analog computer components. Simulation traces are compared with tested results on an actual system.**

Introduction

BLESSED with relatively straightforward circuitry, ac motor drives incorporating current source inverters are being considered for use as a possible alternative to more conventional voltage source inverter drives. Since the current source inverter drive is inherently capable of regeneration, it is particularly appealing for use as four-quadrant single motor drives.

Earlier work has shown that, when a current source inverter is used in conjunction with an induction motor, satisfactory operation cannot be achieved without feedback stabilization [1], [2]. The critical importance of feedback control in the successful operation of this drive makes analytical design techniques especially valuable since time spent on cut-and-try approaches on laboratory breadboards is eliminated. One design approach is to simulate the system on an analog or hybrid computer and set all control gains, time constants, and limits by visually observing the effect each change has on system behavior. This approach is especially appealing, since all relevant quantities are continuously displayed at a rate (time scale) adjusted so that man-machine interaction with the computer is at an optimum.

In past applications inverters have operated on a voltage source principle in which the switching of the inverter could be modeled with reasonable accuracy as an ideal switch with zero internal impedance [3]. Analog computer simulation of such an inverter is readily accomplished with an array of relays. Advent of the current source inverter has presented new problems in inverter modeling since the commutation of a current source inverter does not resemble the effect of an ideal switch. The commutation time is affected both by the capacitance of the commutating capacitors contained within the inverter and also the external load inductance. Because the ac line currents are switched quickly, large voltage spikes appear on the output phases which are directly related to the commutation time. The magnitude of these spikes affects the

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rating of the inverter components so that it is important to accurately simulate this effect. Also, the commutation effect produces an inherent time delay between the instant a change in the output frequency (or phase) is desired and when it actually occurs. This time delay has an influence on control gains which can be tolerated in the feedback control system.

At present, a simulation of a current source inverter has not appeared in the literature. Since an inverter of this type contains six thyristors, six diodes, and six capacitors, a detailed simulation of all components would place a heavy burden on a computer facility and would probably render as impractical system studies involving ac motor drives. This paper describes a unique approach to the simulation of a current source inverter. By attention to the symmetry inherent in the circuit, it is shown how the number of computer components can be reduced to a minimum. The effects of commutation, of critical importance in feedback control, are accurately modeled. The simulation is verified by comparison with an actual system.

Basic Operation

The basic three-phase bridge configuration of a current source inverter drive is illustrated in Fig. 1, which omits the auxiliary circuitry that is required to force-commutate the thyristors. The inverter is fed with a controlled current i_d which, ideally, is constant, has negligible ripple, and is sequentially switched from phase to phase of the motor load. Only two thyristors conduct at any given time, each carrying the impressed direct current for 120° of the fundamental output period, except for commutation overlap. The resulting motor-line currents have a waveform similar to the ac line current produced by a conventional six-pulse voltage-fed rectifier as shown in Fig. 2.

During steady-state operation, an induction motor can be represented as an equivalent counter EMF in series with a small impedance. It can be noted that even though the currents are square wave in nature, the motor terminal voltage is essentially sinusoidal with voltage transients (spikes) superimposed at the instants of commutation. These transients appear across the motor leakage reactance and are generated by the commutating circuit. To produce instantaneous current transfer, as indicated by the ideal waveforms of Fig. 2, infinite impulse voltages would be necessary. In practice, the finite available commutating voltage requires a nonzero time interval to force the current change through the leakage inductance.

In general, three different types of circuit arrangements can be used to commutate the inverter thyristors. 1) Autosequential commutation: Commutation of a main thyristor occurs automatically after firing the next main thyristor in the sequence of the commutating group. No auxiliary thyristors are used [4]. 2) Individual auxiliary commutation: Commutation of a main thyristor is accomplished by firing an auxiliary thyristor. Each main thyristor has an associated auxiliary thyristor [5]. 3) Third-harmonic auxiliary commutation: Commutation of a main thyristor is accomplished by firing an auxiliary thyristor. Each group of three main thyristors has a single auxiliary thyristor. Only one commutating capacitor is used operating at three times the output frequency [6]. Of the three circuits, the autosequential commutated inverter

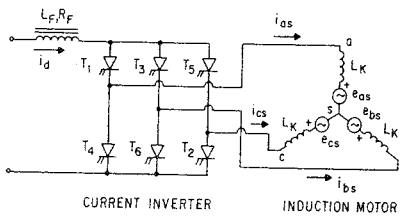


Fig. 1. Simplified current source inverter drive.

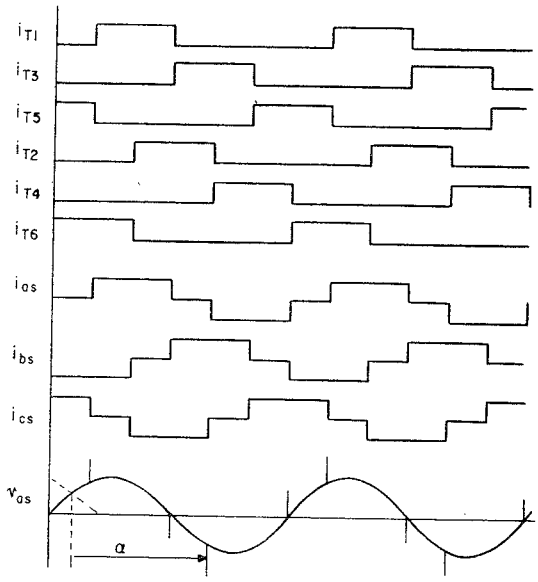


Fig. 2. Idealized current and voltage waveforms.

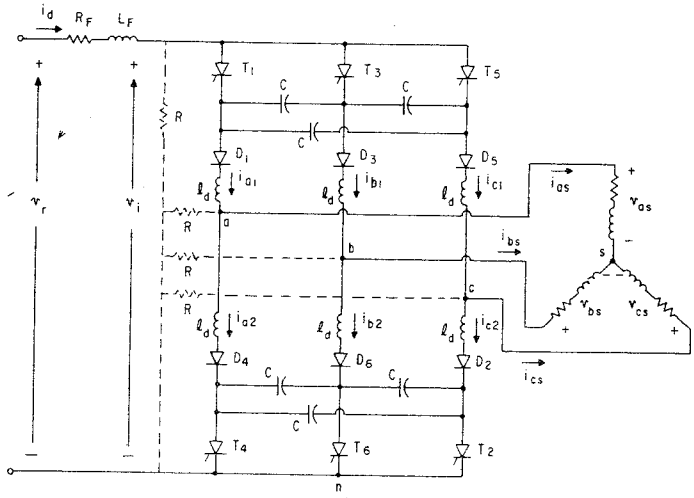


Fig. 3. ASCI inverter arranged for computer modeling.

(ASCI) is by far the most widely used. This paper deals specifically with the simulation of the popular ASCI inverter. However, the approach outlined in this paper can be readily extended to accomodate other types of commutation schemes.

Basic Theory and Equations

The basic ASCI inverter configuration is shown in Fig. 3. It can be noted that additional components l_d and R have been included for purposes of simulation. In most cases the inductance l_d exists physically so as to limit di/dt. If not physically present, it can be made negligibly small in the simulation. The resistances are assumed sufficiently large so as not to affect

the solution. These added components are required in order to develop a sufficient number of equations to define the circuit behavior. It should be mentioned that this approach was originally developed by C. H. Thomas in the modeling of a rectifier bridge and first applied to the study of a magnet power supply [7]. Although a passive load has been shown for simplicity, and type of balanced load can be modeled, for example, an ac induction motor.

If it is assumed that commutation does not occur in the top and bottom halves of the bridge simultaneously, then the inverter topology will assume only one of 12 configurations: six structures existing between commutation intervals and six during the commutation interval. Figs. 4 and 5 show the circuit configuration for two intervals, in particular, just before and during commutation from $T5$ to $T1$. Just before commutation the current is flowing in legs $T5$ and $T6$. The circuit equations for this circuit configuration are

$$i_{c1} = \frac{1}{l_d}\int (v_i - v_{cn})\,dt \tag{1}$$

$$i_{b2} = \frac{1}{l_d}\int v_{bn}\,dt. \tag{2}$$

All other bridge currents are zero.

When thyristor $T1$ is fired, the top bridge current is transferred almost instantaneously from $T5$ to $T1$, since the array of capacitors in the top half of the bridge is so charged as to reverse bias thyristor $T5$. By Thevenin's Theorem, the delta-connected capacitors having capacitance C and initial condition $v_C(0)$, can be replaced by an equivalent capacitor of capacitance $3C/2$ charged to an initial condition $v_C(0)$. The circuit equation valid for commutation from $T5$ to $T1$ can then be written

$$i_{a1} = \frac{1}{l_d}\int (v_i - v_{an})\,dt \tag{3}$$

$$i_{c1} = \frac{1}{l_d}\int (v_i - v_C - v_{cn})\,dt \tag{4}$$

$$i_{b2} = \frac{1}{l_d}\int v_{bn}\,dt \tag{5}$$

where

$$v_C = \frac{2}{3C}\int i_{c1}\,dt. \tag{6}$$

All other currents are zero during these intervals. It is important to note that (4) is the same as (1), except that the commutation voltage v_C has been added. In essence, it can be noted that an added voltage has been "switched" into the equation defining i_{c1}.

Similar sets of equations can be written for the other ten circuit connections. For example, when $T6$ commutates to $T2$, before commutation,

$$i_{a1} = \frac{1}{l_d}\int (v_i - v_{an})\,dt \tag{7}$$

$$i_{b2} = \frac{1}{l_d}\int v_{bn}\,dt. \tag{8}$$

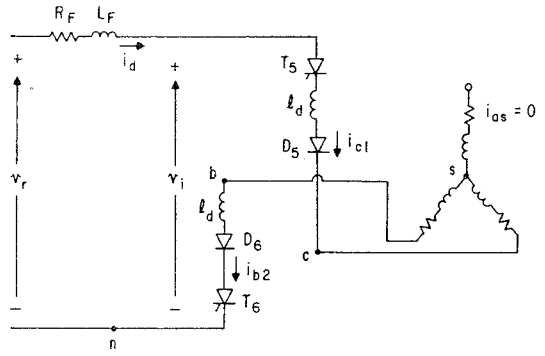


Fig. 4. Circuit configuration just before commutation from $T5$ to $T1$.

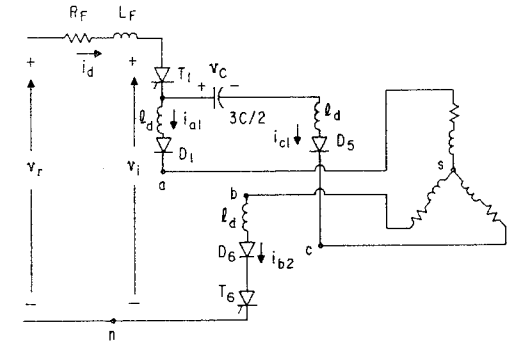


Fig. 5. Circuit configuration during commutation from $T5$ to $T1$.

During commutation,

$$i_{a1} = \frac{1}{l_d}\int (v_i - v_{an})\,dt \tag{9}$$

$$i_{b2} = \frac{1}{l_d}\int (v_{bn} - v_C)\,dt \tag{10}$$

$$i_{c2} = \frac{1}{l_d}\int v_{cn}\,dt \tag{11}$$

where

$$v_C = \frac{2}{3C}\int i_{b2}\,dt. \tag{12}$$

Again, the equations before and during commutation are similar except that the voltage v_C has been introduced in the expression for i_{b2}.

In general, the voltage v_C in (4) and (10) are different entities since they correspond to voltages in the top and bottom halves of the bridge, respectively. In general, however, the final value of v_C reached after the completion of a commutation in the top half differs negligibly from the initial capacitor voltage for the next commutation in the bottom half. Hence, as an approximation, it is assumed that all six commutations can be modeled by means of a single (equivalent) capacitor voltage v_C. In effect, this assumption is valid only when the load is balanced, and commutations do not occur in the top and bottom half of the bridge simultaneously. However, this is a design constraint which is usually met in practice.

It is convenient to let $T_1, T_2, \cdots, T_6$ correspond to vari-

ables which take the value 1.0 when gating signals are applied to thyristors $T1, T2, \cdots, T6$, and zero otherwise. With the above assumption, the six bridge currents and equivalent capacitor voltages can now be written

$$i_{a1} = \frac{1}{l_d}\int (v_i - T_3 v_C - v_{an})\,dt \geqslant 0 \tag{13}$$

$$i_{b1} = \frac{1}{l_d}\int (v_i - T_5 v_C - v_{bn})\,dt \geqslant 0 \tag{14}$$

$$i_{c1} = \frac{1}{l_d}\int (v_i - T_1 v_C - v_{cn})\,dt \geqslant 0 \tag{15}$$

$$i_{a2} = \frac{1}{l_d}\int (v_{an} + T_6 v_C)\,dt \geqslant 0 \tag{16}$$

$$i_{b2} = \frac{1}{l_d}\int (v_{bn} + T_2 v_C)\,dt \geqslant 0 \tag{17}$$

$$i_{c2} = \frac{1}{l_d}\int (v_{cn} + T_4 v_C)\,dt \geqslant 0 \tag{18}$$

$$v_C = \frac{2}{3C}\int (T_3 i_{a1} + T_5 i_{b1} + T_1 i_{c1} - T_6 i_{a2} - T_4 i_{b2} - T_2 i_{c2})\,dt. \tag{19}$$

The symbol "$\geqslant 0$" is appended to each bridge current equation to indicate that the bridge currents are zero whenever the actual integral attempts to go negative. It is clear that the variables T_1 to T_6 imply the use of switches in the computer simulation.

In addition to the bridge currents, expressions must be written which define the dc link current and inverter output voltages. They are

$$i_d = \frac{1}{L_F}\int (v_r - v_i - R_F i_d)\,dt \tag{20}$$

$$v_{an} = R(i_{a1} - i_{a2} - i_{as}) \tag{21}$$

$$v_{bn} = R(i_{b1} - i_{b2} - i_{bs}) \tag{22}$$

$$v_{cn} = R(i_{c1} - i_{c2} - i_{cs}) \tag{23}$$

$$v_{sn} = (1/3)(v_{an} + v_{bn} + v_{cn}) \tag{24}$$

$$v_{as} = v_{an} - v_{sn} \tag{25}$$

$$v_{bs} = v_{bn} - v_{sn} \tag{26}$$

$$v_{cs} = v_{cn} - v_{sn}. \tag{27}$$

In order for (24) to be valid, it is necessary that

$$v_{as} + v_{bs} + v_{cs} = 0. \tag{28}$$

Equation (28) is valid whenever the load is balanced. It can be shown that (28) is true for symmetrical induction machines and synchronous machines as well as for passive loads [8].

Analog Simulation

The analog computer-simulation diagrams which evolve from the above equations are given in Figs. 6-9. A summary of the computer symbols used to construct the diagrams is

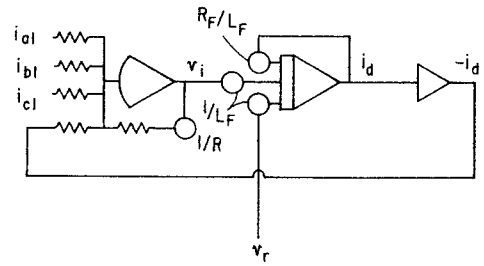


Fig. 6. Simulation of dc link.

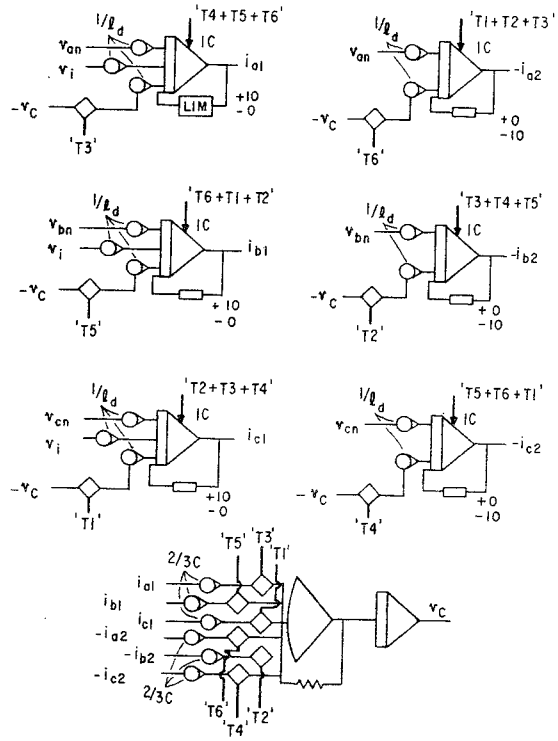


Fig. 7. Simulation of bridge currents and commutation voltage.

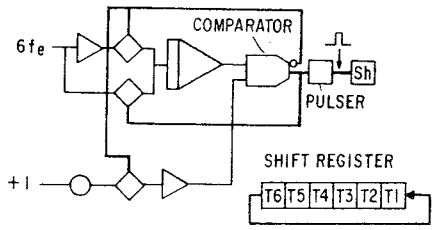


Fig. 8. Simulation of thyristor firing signals.

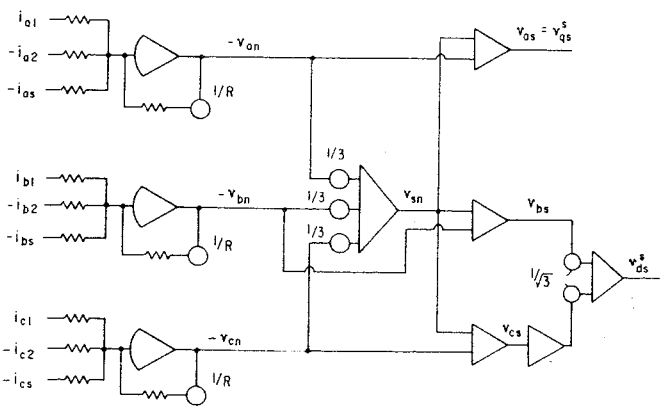


Fig. 9. Simulation of inverter bridge and load voltages.

given in the Appendix. Fig. 6 shows the computer implementation of the dc link current i_d. The source voltage v_r is assumed to be available as an output from a simulation of another device, for example, a six-pulse rectifier or dc/dc chopper.

In Fig. 7 the simulation of the inverter bridge currents and commutation voltage v_C is given. The logic variables "$T1$," "$T2$," etc., corresponding to the gating pulses of the six thyristors, are assumed to be "1" when the respective thyristor is gated, and zero otherwise. The required gating pulses can be instrumented by various techniques. One technique which converts a variable-amplitude analog signal to a variable-frequency set of logic pulses is shown in Fig. 8. Note that additional "lockout" logic has been provided by resetting each thyristor current integrator to zero to insure that the thyristors will not conduct over the reverse half of its conduction cycle.

The inverter bridge and load voltages are shown in Fig. 9. The equations defining the load are not shown. In the event that the required load is an induction motor, the voltages v_{qs}^s and v_{ds}^s are the inputs to the simulation of the induction machine (not shown [8]).

Simulation Results

In order to verify the computer simulation, representative traces were compared to measured results from an actual system. The induction machine used for purposes of comparison was a 230-V 4-pole 25-hp induction machine having the following parameters: $r_s = 0.0788\ \Omega$, $r_r' = 0.0408\ \Omega$, $x_{ls} = 0.2122\ \Omega$, $x_{lr}' = 0.4632\ \Omega$, $x_m = 5.54\ \Omega$, and $J = 1.0\ \text{kg} \cdot \text{m}^2$. The base frequency used to compute the above reactances was 60 Hz. The inverter commutation capacitance and dc link inductance was 80 μF and 8.96 mH, respectively. A six-pulse rectifier bridge was used to obtain the dc link input voltage v_r.

Fig. 10 shows a scope trace taken from the actual system. For the case shown, the inverter frequency was set at one-half rated frequency (30 Hz), and the dc link current was adjusted until the fundamental component of motor-line current was at rated value ($i_d = 82$ A). The slip of the motor was 0.04. The large spikes in the motor phase voltage resulting from inverter commutation are clearly evident. The ripple current superimposed on the ideal quasi-square wave stator current results from the finite value of dc link inductance used in the actual hardware. The frequency of the ripple current contains both 180- and 360-Hz ripple currents arising from the inverter and rectifier, respectively.

Fig. 11 gives the corresponding simulation results for the same operating condition. Examination of the computed phase current and voltage with the measured results indicates excellent agreement. Similar correlation was obtained with the other variables shown in Fig. 11, except for v_C which is an equivalent rather than an actual voltage variable.

The simulation of the current source inverter which has been developed has proven very effective in evaluating control algorithms for such drives. One typical system is the current-amplitude and slip-frequency control system shown in Fig. 12 [9]. Fig. 13 is a typical starting transient for this system using the analog computer simulation of this paper. Note

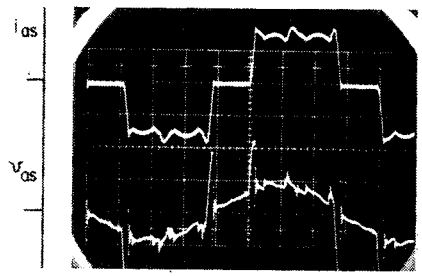


Fig. 10. Measured results form an actual drive system. Top trace: motor line current i_{as}, scale 50 A/div. Bottom trace: motor phase voltage v_{as}, scale 100 V/div.

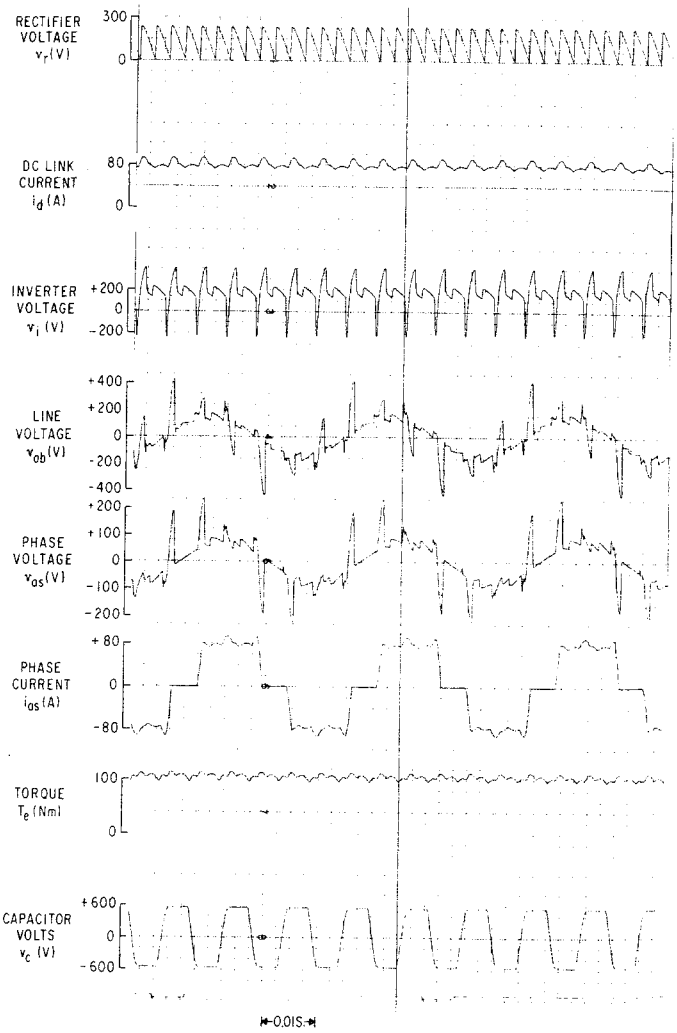


Fig. 11. Computed results from an analog computer simulation.

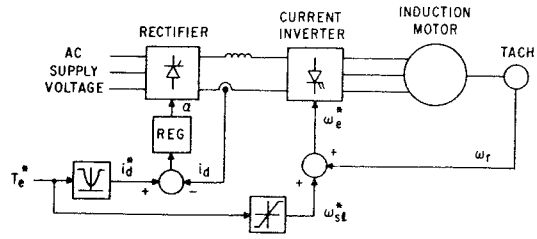


Fig. 12. Torque controller for current source inverter ac drive employing current amplitude and slip frequency regulation.

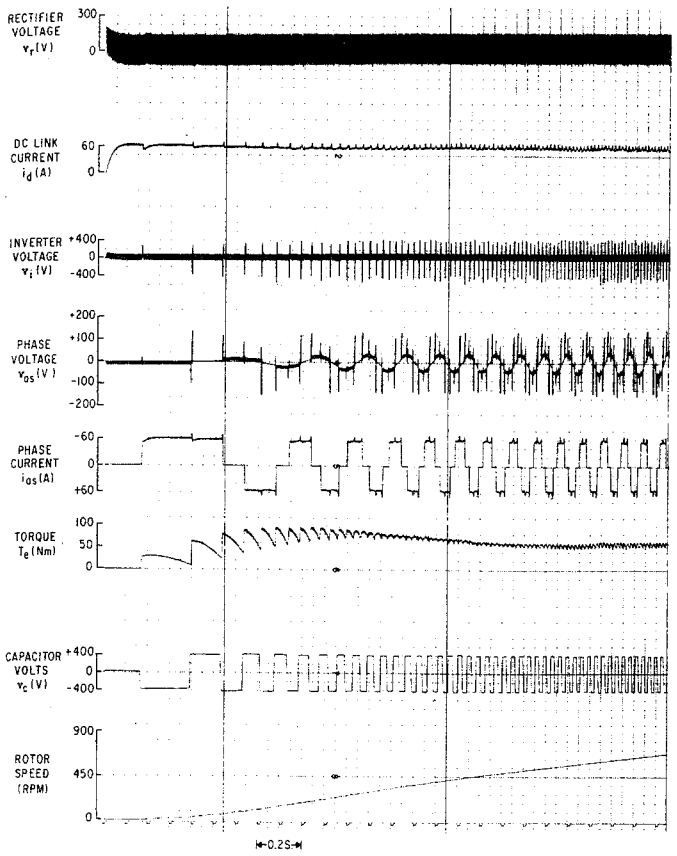


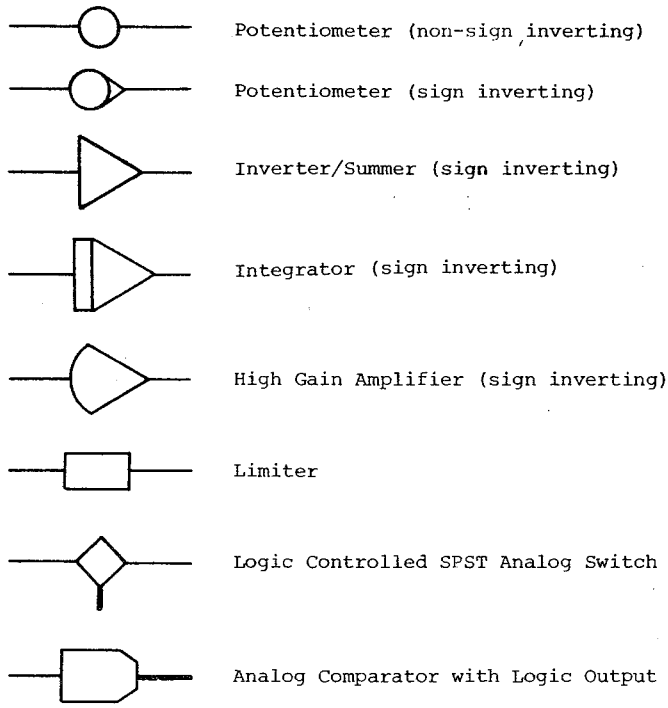
Fig. 13. Acceleration of drive from a stalled condition with inertial loading using control system of Fig. 12.

again the voltage spikes which ride on top of the motor phase and line voltages. With minor modifications a wide variety of control schemes can be studied and compared one against the other. Such studies have contributed to the development of new control algorithms having superior dynamic response [10], [11].

Conclusion

This paper has presented a simplified approach to the computer simulation of a current source inverter. It is shown that the commutating capacitors can be reduced from six to a single equivalent capacitor, resulting in a substantial reduction in computer components. Although this paper deals specifically with analog computer simulation, the approach is equally valid for digital computation using simulation algorithms. A key assumption in this approach is that commutation does not occur simultaneously in both the top and bottom halves of the bridge (commutation overlap). Fortunately, in practice, operation in this mode is to be avoided, so this assumption does not constitute a severe restriction. The simulation is valid for both steady-state and transient behavior and, therefore, should prove most useful to those engaged in the design of such systems.

Appendix
Analog Computer Symbols



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