Analysis of a Novel Forced-Commutation Starting Scheme for a Load-Commutated Synchronous Motor Drive

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Abstract—A load-commutated inverter synchronous motor drive system employing a simple auxiliary commutation circuit for machine startup is analyzed, and results of a hybrid computer simulation are presented. The commutation circuit employs a single commutation capacitor connected to the neutral of the machine and two auxiliary thyristors, which are used only during machine starting. A practical operating scheme is developed for the forced commutated inverter, which insures commutation over all load currents by actively allowing the commutation capacitor to charge to a voltage proportional to load current. Results of key computer runs are given including inverter waveforms, transient waveforms during transition from forced to load commutation, as well as the effect of forced commutation and load commutation on pulsating torque. The forced-commutation circuit is used only for synchronous machine startup. However, due to its simplicity it also is an attractive alternative to be considered for other types of current-fed inverter ac drives.

INTRODUCTION

ONE OF THE factors which has prevented the widespread use of ac drive systems has been the relative expense of the forced-commutated inverter compared to their ac-dc or dc-dc converter counterparts. When employing a synchronous motor, the field winding can be overexcited such that a leading power factor is presented to the inverter. In this case natural or load commutation of the inverter thyristors can be obtained. Load commutation considerably simplifies the inverter and is a highly desirable mode of operation. Unfortunately, such a drive cannot operate at low speeds where the machine counter electromotive force (EMF) is insufficient to commutate the inverter thyristors. Even in applications where the machine must operate over a limited speed range, some method must be employed to start the machine. One technique which has been used to commutate the inverter at low speed is to interrupt the dc link current by proper control of the phase-controlled rectifier feeding the inverter [1]. Since the phase-controlled rectifier must drive the dc link current to zero six times per cycle, this method can only be used at relatively low motor speeds. When operating from a dc source, such as in a traction application, a force-commutated chopper circuit must be used to utilize this commutation scheme.

In this paper an alternate method of starting a synchronous machine is presented employing a simple forced-commutation circuit. The circuit utilizes a single commutation capacitor and only two auxiliary thyristors for the entire inverter. Since the forced commutation part of the inverter need operate only over low speeds where the inverter is unable to load commutate, the rating of the circuit components need only be a fraction of the full machine rating. Fig. 1 shows a circuit diagram of the commutation scheme. It can be noted that the commutation capacitor is connected to the neutral of the machine. Since the fundamental component of the commutation capacitor current is three times the inverter fundamental frequency, an inverter employing this scheme may be termed a third harmonic auxiliary commutated inverter. Such a commutation scheme has been proposed in the past for use in HVdc transmission systems to obtain forced commutation of the inverter (rather than the usual line commutation) and thus reduce the amount of reactive power consumed from the ac system. The arrangement is attributed to Kaganor and Saba in [2], where further references dating from 1940 are given. Recently the technique has been adapted for use in applying forced commutation to a thyristor cycloconverter [3].

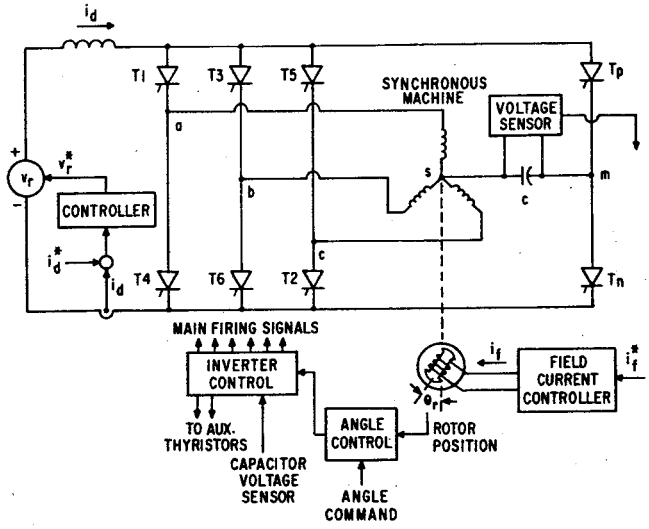

Fig. 1. Load-commutated synchronous motor drive with third harmonic auxiliary commutation.

This paper analyzes the third harmonic commutated inverter specifically for use in starting synchronous machines. However, the approach also offers the possibility of a simple economical forced-commutated current-fed inverter for induction-motor drives. The behavior of the commutation circuit, including effects on motor performance, are analyzed with the aid of a hybrid computer. Operating problems of the drive system in the load-commutated mode including transients occurring

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during the transition from forced to load commutation are addressed. System control strategies including proper thyristor gating control are developed.

SYSTEM DESCRIPTION

Fig. 1 shows a simplified version of the drive system to be studied. This figure also served to define the nomenclature which will be used throughout this paper. In this system a controllable dc link current i_d is fed to a three-phase inverter which in turn drives a wound-field synchronous machine. The link current is controlled by adjusting the voltage source v_r in response to an error signal generated by the difference of actual link current i_d and the commanded link current i_d*. In practice the voltage source can be any type of ac/dc rectifier or dc/dc chopper, but is not considered in detail here. The inverter main thyristors $T1$-$T6$ are gated in the usual fashion sequentially as numbered. The thyristors are fired directly by the output of the angle control block, which consists of a set of six pulses for each electrical revolution of the machine. The pulses occur at a known location relative to the shaft position by employing a shaft position sensor which measures the shaft angle and then phase shifting this signal by a controllable amount as determined by the angle command. The thyristors are thus fired at preselected rotor locations, and therefore the angle between the field magneto motive force (MMF) and the stator MMF is controlled.

The machine field current i_f is also assumed controllable in the same fashion as the dc link current in response to a command signal i_f*. Since the stator current, rotor angle, and field current are controllable, the power factor can be controlled if desired, and hence load commutation can be accomplished. However, at standstill or low speed, the machine has negligible counter EMF, and the inverter cannot load-commutate. Therefore, an auxiliary method of commutating the thyristors is needed until the machine gains sufficient speed to load-commutate. The commutation circuit shown in Fig. 1 is used to accomplish the necessary inverter commutation. The commutation capacitor voltage sensor is used to actively control the peak capacitor voltage, and its operation will be explained below. Two different types of thyristor gating can be implemented and warrant separate consideration.

PRINCIPLES OF COMMUTATION–SIMPLE SEQUENTIAL GATING

In order to provide an adequate starting point for the discussion to follow, the commutation principle will be discussed briefly. In analyses of this type the machine can be represented by a counter EMF of peak value E_M in series with a commutating inductance L_k. Consider the commutation from main thyristor $T2$-$T4$. The equivalent circuit for this commutation is shown in Fig. 2 with the initial capacitor voltage as indicated. The waveforms for this interval are sketched in Fig. 3. Examination of Fig. 3 reveals that commutation takes place in three stages.

Stage 1

Commutation is initiated by firing auxiliary thyristor Tn, which effectively places capacitor C in parallel with e_3 and L_k

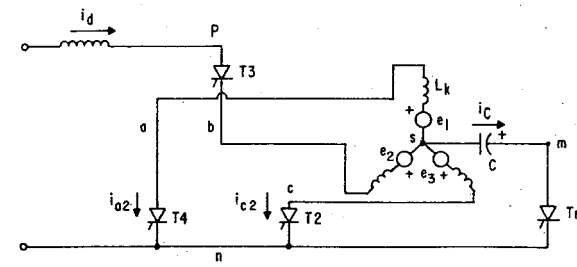

Fig. 2. Equivalent circuit for commutation from $T2$ to $T4$.

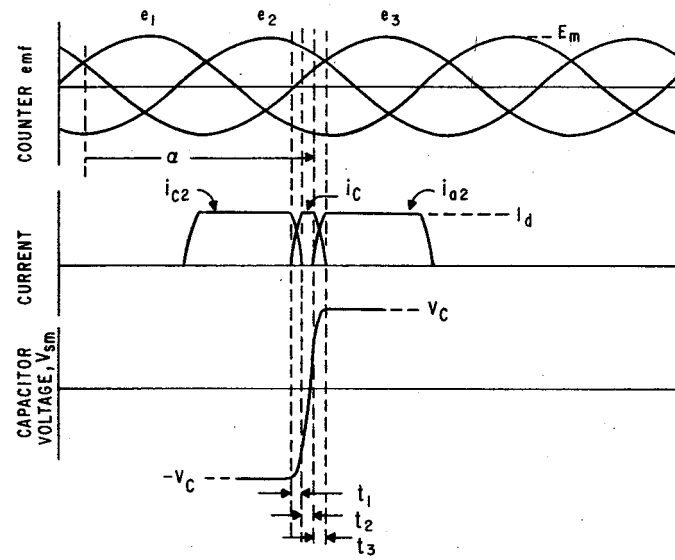

Fig. 3. Waveforms for commutation from $T2$ to $T4$.

(motor phase c, line to neutral). For proper operation, the initial capacitor voltage v_{ms} is higher than e_3, and consequently the current in phase C immediately starts to decrease, while the current in the commutating capacitor begins to build up. The sum of these currents is the constant direct current I_d. There is gradual commutation of current from phase c to the commutating capacitor. During this current transfer, the capacitor voltage v_{sm} becomes more positive. Stage 1 lasts until the entire load current has been commutated to Tn and the capacitor, at which point $T2$ goes off. This first stage lasts for a time t_1 as indicated on Fig. 3.

Stage 2

Since the capacitor is now carrying all of the load current, the capacitor voltage v_{sm} rises linearly until it equals the counter EMF generated in phase a (i.e., until $v_{sm} = -e_1$). The second stage lasts for a time t_2 as seen in Fig. 3. Note that during stage 2, the current in phases a and c is zero. Thus the actual motor currents will be less than the usual 120° duration.

Stage 3

When the capacitor voltage v_{sm} overcomes the counter EMF of phase a $(-e_1)$ current begins to transfer from capacitor C to thyristor $T4$. It is assumed that $T4$ is fired as soon as forward voltage is applied to it or, alternatively, that Tn and $T4$ are fired simultaneously and the gate pulse to $T4$ remains

throughout stages 1 and 2 and is present when the voltage on $T4$ becomes positive. Since current i_{a2} is increasing, the capacitor current is decreasing, and the rate of rise of capacitor voltage decreases until commutation is complete ($i_{a2} = I_d$). The capacitor voltage is now of the proper polarity to commutate $T3$ off when Tp is fired. From symmetry it is concluded that the initial capacitor voltage was $-V_c$ as shown in Fig. 3. As shown in Appendix B, the peak capacitor voltage V_c is given by

$$V_c = I_d \sqrt{\frac{L_k}{C}} - E_M \sin(\alpha + \pi/6) \tag{1}$$

where E_M is the peak counter EMF generated by the machine. Note that this voltage must be sufficiently high to commutate $T3$ off for the next commutation. This situation will only be true if e_3, the counter EMF of phase c, is lower than $-e_1$, the negative counter EMF of phase a, during the commutation. As proven in Appendix B, this condition essentially limits the range of angles α over which the commutation circuit is effective to

$$90° < \alpha < 270°.$$

The particular case of zero counter EMF illustrates the potential problem with the commutation circuit. Following Appendix B with the counter EMF zero, the capacitor charges to a peak voltage given by

$$V_c = I_d \sqrt{L_k/C}. \tag{2}$$

During the next commutation the current in the offgoing thyristor is given by

$$i_{c2} = I_d - \frac{V_c}{\sqrt{L_k/C}} \sin(t/\sqrt{L_k C}), \tag{3}$$

while the capacitor voltage is given by

$$v_{ms} = V_c \cos(t/\sqrt{L_k C}). \tag{4}$$

The time when current reaches zero in the offgoing thyristor is found by setting (3) equal to zero. This results in

$$t/\sqrt{L_k C} = \sin^{-1}(I_d\sqrt{L_k/C}/V_c). \tag{5}$$

Substituting V_c from (2) gives

$$t/\sqrt{L_k C} = \sin^{-1} 1 = \pi/2. \tag{6}$$

Incorporating this expression in (4) yields

$$v_{ms} = 0, \tag{7}$$

that is, the capacitor has discharged completely to zero in a quarter cycle oscillation, while driving the current in the offgoing thyristor to zero.

Since the capacitor now carries the dc link current, it immediately reverses, reapplying forward voltage to the thyristor which results in zero turn-off time. It is clear that for practical circuits, which will contain some losses, the thyristor will not turn off. From the above simplified discussion it is clear that at zero speed, the capacitor will not charge high enough at the end of a commutation to insure the next commutation. To overcome this problem, the technique of delayed gating has been employed as described below.

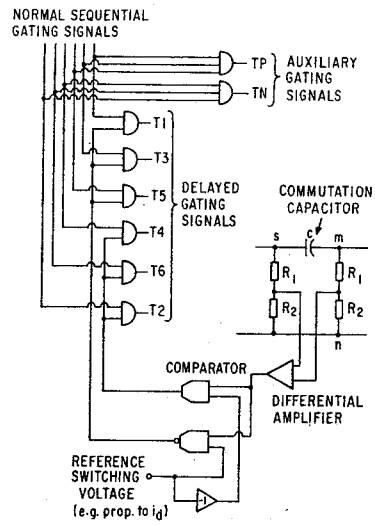

Fig. 4. Technique for delayed gating of main thyristors.

PRINCIPLES OF COMMUTATION–DELAYED GATING

It is useful to now refer to Fig. 4, which illustrates the delayed gating principle. In general, the sequential gating signals for the main thyristors are delayed until the capacitor charges to a predetermined voltage level as sensed by a suitable capacitor voltage sensor (differential amplifier and comparators). The capacitor is thus assured of charging to a predetermined voltage level and commutation is guaranteed.

In order to illustrate the delayed commutation principle, consider a commutation of current from thyristor $T2$-$T4$ (phase c to phase a), and assume the capacitor voltage v_{ms} is positive. To turn $T1$ off, auxiliary thyristor Tn is fired, and C is placed across phase c in such a direction as to drive i_{c2} to zero. When i_{c2} is driven to zero, $T2$ turns off, and the entire link current is in C, which therefore reverses its voltage linearly. When the voltage on capacitor C is of sufficient value to forward bias $T4$, the firing of $T4$ is delayed by the inhibit signals being applied to the AND gates. $T4$ is allowed to be fired only after C has charged to a sufficiently high voltage to insure the next commutation. This voltage level is determined by comparing the signal voltage indicative of capacitor voltage v_{sm} with a desired threshold level (reference switching voltage). The output of the comparator inhibits the gating of the main thyristors until the capacitor has charged to the reference level. The voltage dividers, consisting of $R1$ and $R2$, allow the capacitor voltage to be sensed using signal level circuitry (i.e., the differential amplifier).

It can be noted that the reference switching voltage may be constant value or be controlled to follow a signal indicative of some other circuit parameter. For example, the threshold level can be proportional to link current, thus assuring a higher commutating voltage as the link current increases. In this man-

ner the circuit commutating ability can be made to track that required by the load.

If the main thyristor gating is delayed until the capacitor voltage charges to a reference value V_{ref}, then the final capacitor voltage will be given by

$$V_c = \sqrt{[V_{ref} + E_M \sin(\alpha + \pi/6)]^2 + I_d^2 L_k / C} - E_M \sin(\alpha + \pi/6). \quad (8)$$

Precharging of Commutation Capacitor

When it is desired to load commutate, firing of the auxiliary thyristors is simply inhibited. To initially charge the capacitor for startup, an auxiliary thyristor and an opposite main thyristor (e.g., *Tn* and *T*1) may be fired causing the capacitor to ring up through the link inductor L_d and phase *a* toward twice the link voltage. Then, as operation begins the capacitor will pump up as determined by the reference switching voltage. Alternatively, the capacitor may be initially charged through a resistor from an auxiliary power supply.

SYSTEM SIMULATION

In order to properly evaluate system behavior, a hybrid computer simulation of the third harmonic commutated inverter was implemented, including a detailed model of both inverter and machine. The synchronous machine was simulated in the usual manner as an equivalent two-phase machine with the reference frame for voltage and current vectors fixed in the rotor [4]. The thyristors were simulated as perfect switches with series *di/dt* reactors. The simulation of the commutating circuit is of particular interest and is included in Appendix A. The remainder of the inverter was simulated in similar fashion. The dc link as shown in Fig. 1 was also simulated as well as the rotor position sensor and necessary voltage and current transformation (three-phase to two-phase transformation and vice-versa).

The synchronous motor chosen for this study corresponds to a 20 kVA, eight-pole homopolar-inductor type of machine. The maximum rotor speed is 7500 r/min corresponding to a line frequency of 500 Hz. Rated terminal line voltage is 90 V at this frequency. These parameters correspond to those of an onboard inductor-motor flywheel energy-storage device for an electric vehicle application [5]. The parameters of the machine and the rest of the system parameters are as follows

Synchronous machine (homopolar-inductor motor) parameters:

r_s	$= 0.0139\ \Omega$,	base 1 = *n* voltage = 71.8 V (peak),
x_{ls}	$= 0.07228\Omega$,	base frequency = 500 Hz,
x_{md}	$= 0.215\ \Omega$,	base kVA = 20,
x_{mq}	$= 0.1197\ \Omega$,	poles = 8,
$x_{lfr'}$	$= 0.7458\ \Omega$,	inertia = J = 0.0109 kg·m^2,
$r_{fr'}$	$= 0.00309\Omega$.	

Inverter and dc link filter parameters:

$C = 160\ \mu$F,
$l = 10\ \mu$H,
$L = 0.358$ mH,
$RL = 0.0085\ \Omega$,
} Figs. 6–8.

SIMULATION RESULTS

Third Harmonic Commutation

Fig. 5 shows the inverter operating at a fundamental frequency of 250 Hz. This condition corresponds to high-frequency operation of the inverter, which would probably not be encountered in the event that load commutation is used for high-speed operation, but serves to illustrate the commutation waveforms. Note that the motor voltage and current waveforms are similar, but not identical to those obtained for a conventional current-source inverter [6]. In particular, the currents in the main thyristors *T*1, *T*2, ···, T6 are slightly less than 120°. Notches in the phase voltage now occur in pairs corresponding to the turn-on and turn-off of the auxiliary thyristor currents.

Since the commutation circuit voltage must exceed the counter EMF of the machine, the commutation time depends greatly on the motor winding EMF which appears in series with the commutation capacitor at the commutation instant. Note that the "rate of rise" of the thyristor current *Tp* is significantly greater than the subsequent "rate of decrease." In the limiting case, the thyristor currents i_{Tp} and i_{Tn} are each on for half the time, and the main thyristor currents become 60° rather than 120° blocks of current. Also, the capacitor voltage becomes triangular, and the reverse recovery voltage on the thyristor is very small indicating that thyristors *Tp* and *Tn* are on the verge of shorting the dc link. This situation represents the highest operating frequency attainable for the given load and circuit parameters. For the present system, the limiting frequency was 400 Hz at a dc link current of 150 A.

The waveforms shown in Fig. 5 were taken for an ideal dc link current source (infinite link inductor). The waveforms for a finite dc link inductor (0.358 mH) are nearly identical to those of Fig. 5 except that small ripples appear in the dc link current during the commutation periods as shown in Fig. 6.

Effect of Third Harmonic Commutation on Electromagnetic Torque

In general, the pulses of current that flow through the thyristors *Tp* and *Tn* contribute a zero sequence component that is a nontorque producing component of current. As a result it can be shown that the torque is essentially reduced by one-half during the commutation interval. Fig. 7 illustrates this effect for the 50 Hz case. Fig. 8 shows the torque waveform for four higher line frequencies. The "notches" that occur in the torque waveform are clearly evident. Although the duration of the notches is effectively the same for all operating frequencies, as the frequency increases, the notches become a greater and greater portion of a cycle. At 100 Hz the notching has resulted in the average torque being depleted by approximately one-eighth, at 200 Hz by one-fourth, and at 400 Hz by one-half.

Load Commutation

Fig. 9 displays the same operating condition as Fig. 5, except in this case the commutation circuit was disabled and the six-pulse thyristor bridge was forced to operate under load commutation (back EMF commutation). Note that the com-

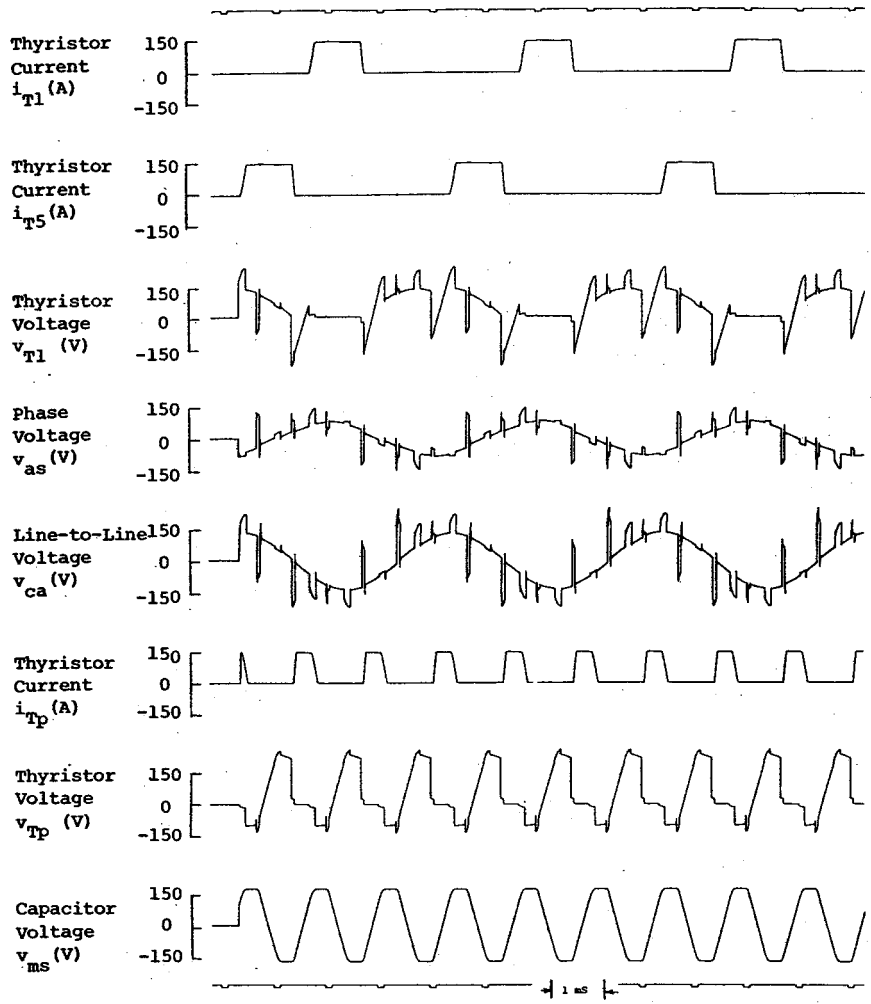

Fig. 5. Steady-state operation under third harmonic auxiliary commutation at 250 Hz with constant dc link current.

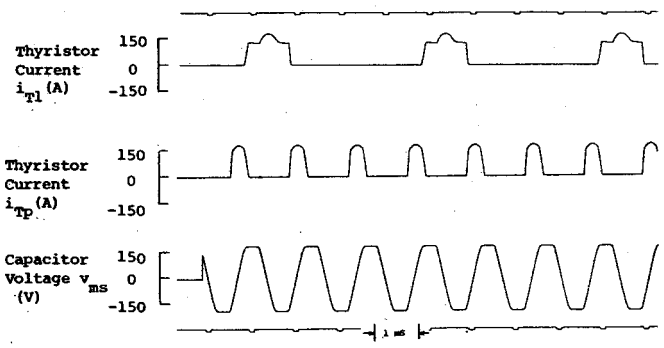

Fig. 6. Effect of finite link inductor on operation under third harmonic commutation at 250 Hz.

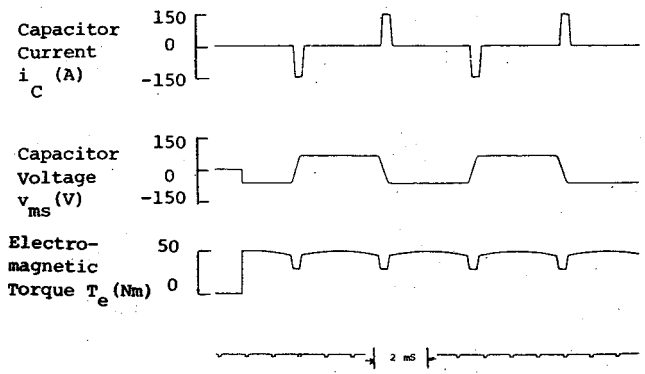

Fig. 7. Effect of commutation on electromagnetic torque at 50 Hz.

mutation notches are much larger (longer) than for the corresponding forced commutation case. The large spikes which appear on the motor windings are no longer present.

Effect of Delayed Gating

In Fig. 10 the proper main thyristor has been gated at the same instant as the auxiliary thyristor (no commutation delay). The dc link current is slowly reduced to zero to observe the effect of load on commutation. Since the commutation capacitor voltage is a function of the link current (8), it decreases as i_d is decreased. Note that $\alpha \cong 160°$ for this case, and thus delayed gating is not needed since $90° < \alpha < 270°$ as explained earlier. However, the method is unable to commutate upon starting or for other values of α without delayed gating.

In Fig. 11 the firing of the main thyristors has been delayed. In particular, the oncoming main thyristor has been delayed until the capacitor voltage exceeds a preset threshold

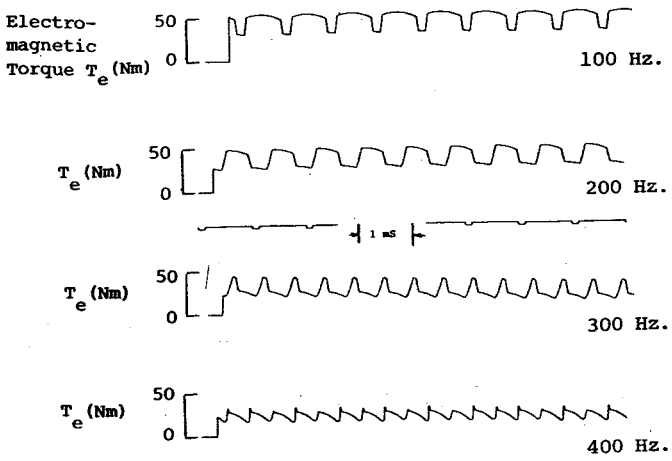

Fig. 8. Effect of commutation on electromagnetic torque for progressively higher frequencies.

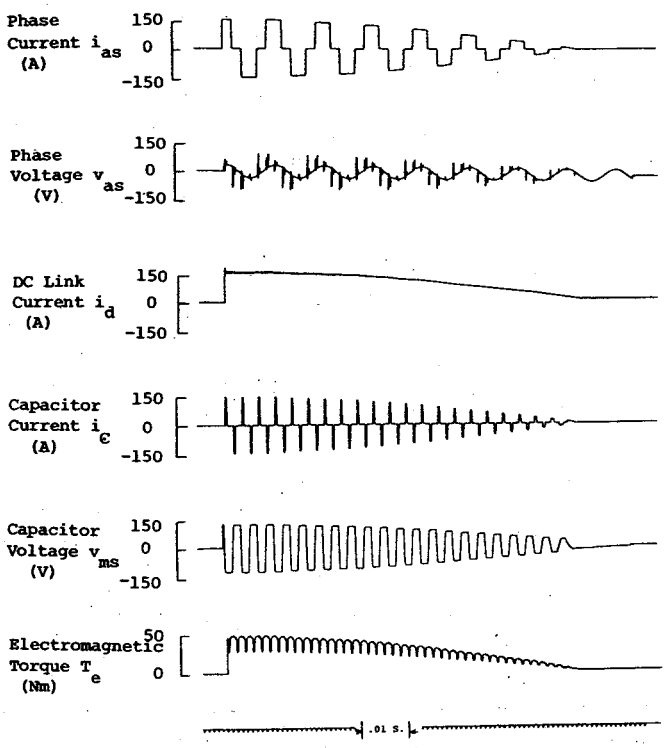

Fig. 10. Performance of commutation circuit as dc link current is decreased. No delay in commutation time.

of 150 V. Note that commutation continues successfully until the link current is reduced to a sufficiently small value that the capacitor voltage does not exceed the prescribed threshold before the opposite auxiliary thyristor is fired. At this point a commutation failure occurs as the auxiliary thyristors shunt the dc link. It is apparent that the commutation time increases for decreasing i_d resulting in widening "notches" in the electromagnetic torque.

Fig. 12 shows the effect of making the threshold voltage for commutation delay a function of dc link current. Note that the capacitor voltage again decreases as link current is decreased. The result is similar to Fig. 10. However, in this case, the commutation time is under control and can be adjusted at will, and the inverter can be operated at all values of α as well

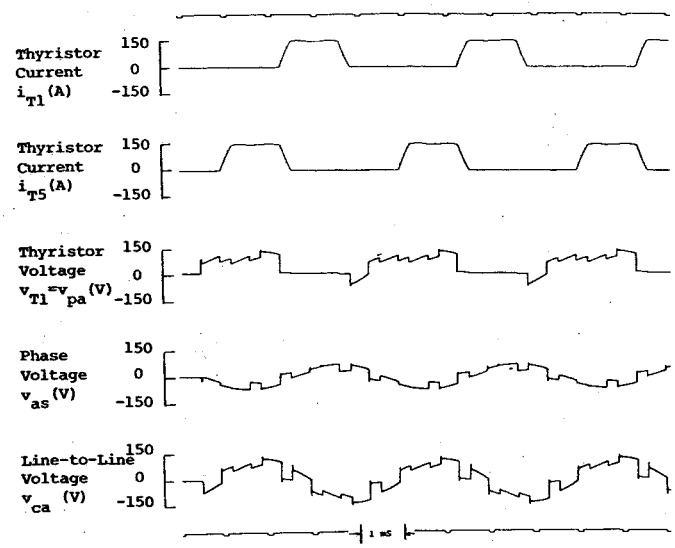

Fig. 9. Steady-state operation under load commutation at 250 Hz, $\alpha = 0°$.

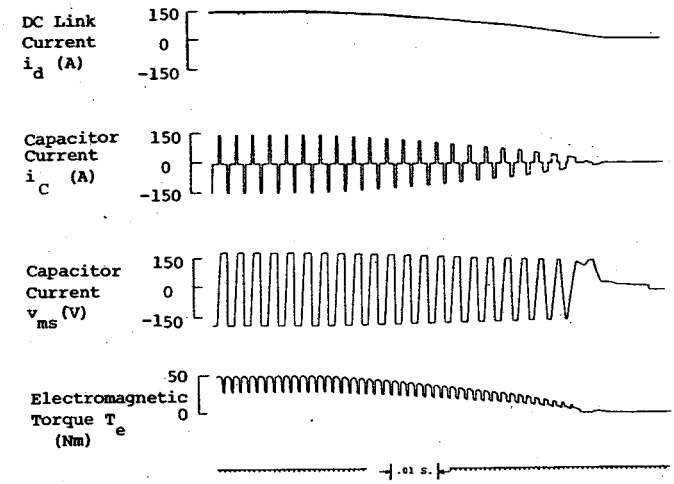

Fig. 11. Performance of commutation circuit as dc link current is decreased. Delay in commutation time maintaining constant commutation voltage.

as at motor standstill. If desired, a lower limit can be provided in the commutation time for very light load conditions.

Transient Behavior During Transition from Forced to Load Commutation

Fig. 13 displays a typical transition from forced to load commutation. In particular, the MMF angle is set at 60° and the motor is adjusted for leading power factor. For this run, the dc link current as well as the speed were held constant. It can be observed that the torque increases markedly after the transition to load commutation.

Effect of Link Current and Line Frequency on Load Commutation

Two of the system variables which have a dominant effect on load commutation are the motor line frequency and dc link current. In Fig. 14 the dc link current has been increased gradually so as to observe the effect on commutation. It can

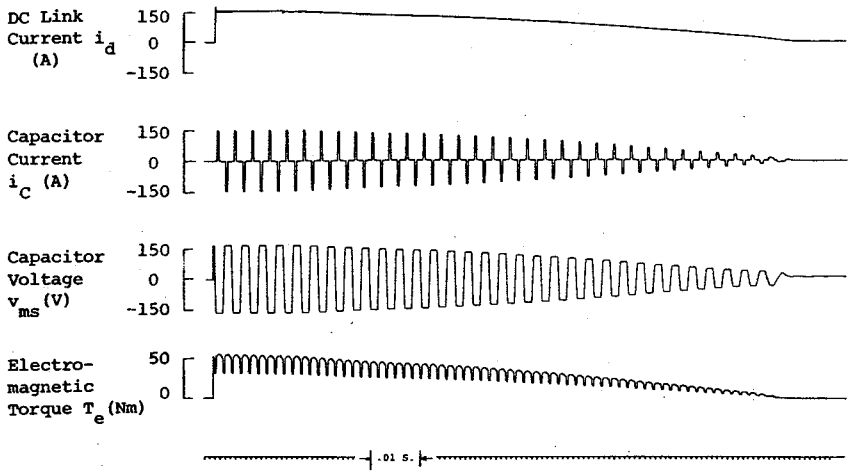

Fig. 12. Performance of commutation circuit as dc link current is decreased. Threshold level proportional to dc link current.

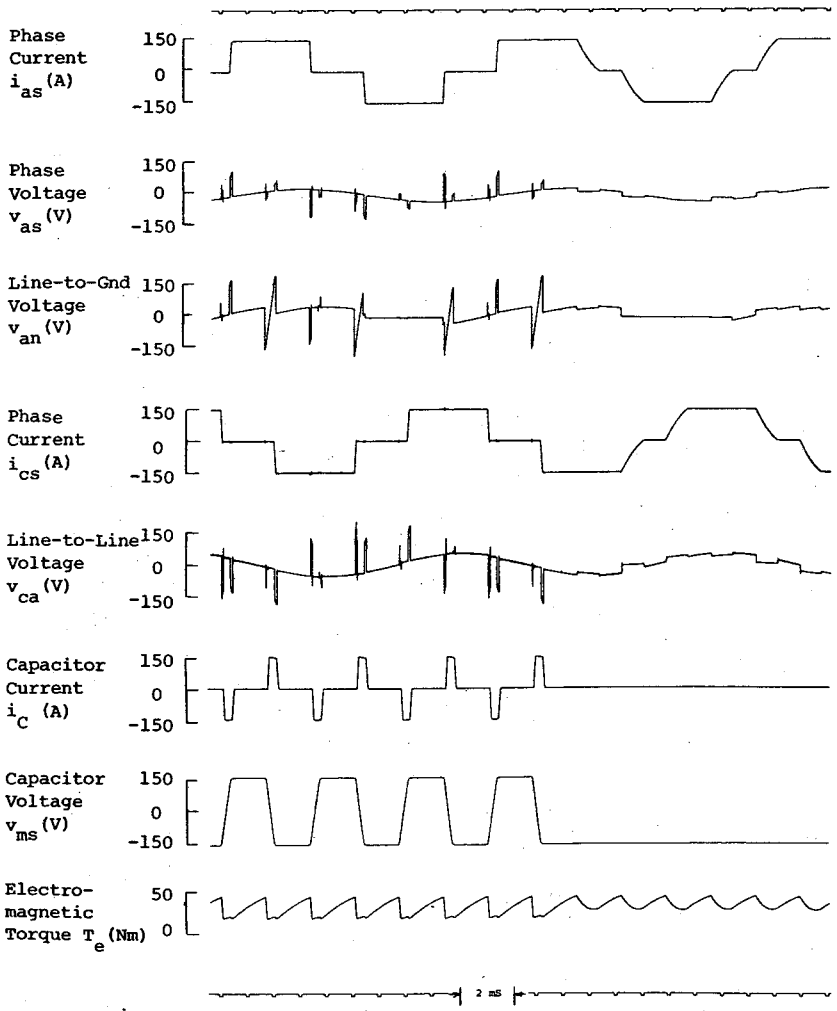

Fig. 13. Transient behavior of system during transition from forced to load commutation, $\alpha = 60°$, 100 Hz.

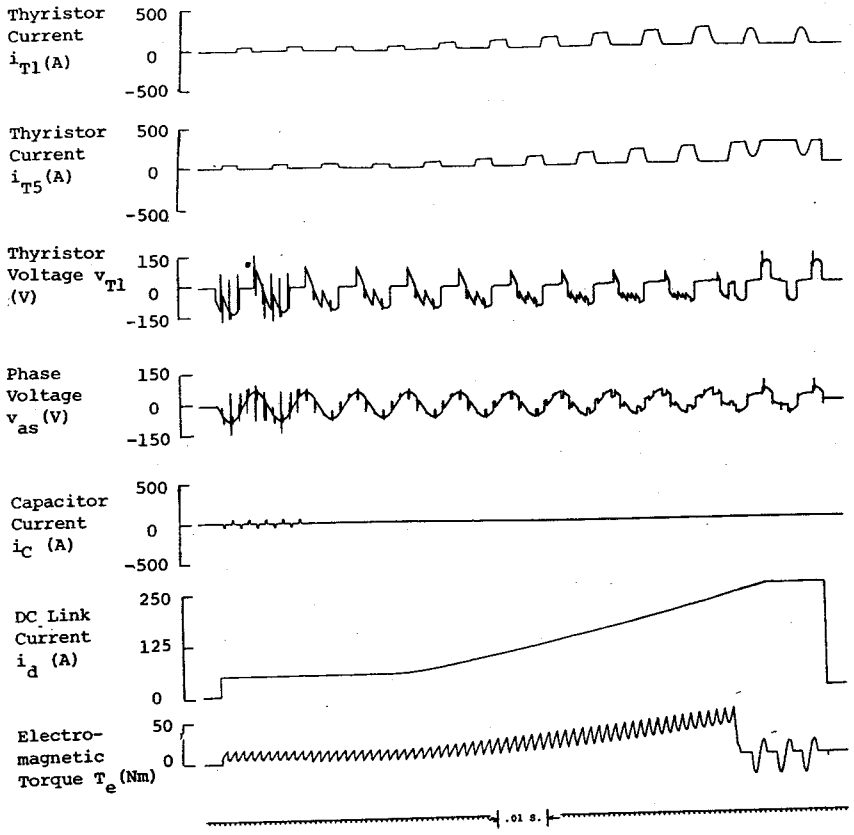

Fig. 14. Effect of increasing dc link current on load commutation at 50 Hz.

be noted that the turn-off time decreases in proportion to the link current so that ultimately thyristor $T5$ is unable to commutate to $T1$ and shoot-through occurs.

In Fig. 15 the dc link current has been held constant, but the motor speed reduced slowly. In general, successful transition from force to load commutation could not be achieved below 0.1 pu speed (50 Hz). However, once having achieved load commutation much lower speeds were possible. In Fig. 15 a transition to load commutation is made at 50 Hz. and the line frequency then slowly decreased. It can be noted that commutation failure does not occur until the machine reaches a frequency of 0.03 per unit (15 Hz).

CONCLUSIONS

A load-commutated inverter drive employing a simple forced commutation circuit for machine startup has been analyzed and shown to be an excellent candidate for a practical ac drive system. Since the commutation circuit consists of a single capacitor and only two auxiliary thyristors, the basic simplicity of the load-commutated inverter power circuit is maintained. By delaying the gating of the incoming main thyristor, the forced commutation can be maintained over all inverter delay angles. Using this technique, the commutating capacitor peak voltage can be actively controlled to optimize circuit operation. Transition from forced to load commutation and vice versa is accomplished without any difficulty. While the analysis presented here has centered specifically around a synchronous machine drive, the commutation scheme can also be used for other current-fed ac drives (i.e., synchronous-reluctance, permanent magnet, or induction motor drives). Third harmonic commutation shows promise as a simple reliable commutation technique for low-cost ac motor drives.

APPENDIX A
SIMULATION OF COMMUTATION CIRCUIT

The simulation diagram for the commutation circuit will be developed with reference to Fig. 16. The phase currents and dc link voltage are available from other parts of the simulation and are generated in conventional fashion. It can be noted that a large resistance is placed from neutral to ground to develop the neutral voltage, while the di/dt inductors are used to generate the auxiliary thyristor currents. Referring to Fig. 16, the neutral to ground voltage is

$$v_{sn} = R_{sn}(i_{as} + i_{bs} + i_{cs} + i_{Tp} - i_{Tn}).$$

Assuming that the respective thyristor is conducting,

$$i_{Tp} = \frac{1}{l}\int (v_{pn} - v_{ms} - v_{sn})\,dt \geq 0 \tag{9}$$

and

$$i_{Tn} = \frac{1}{l}\int (v_{ms} + v_{sn})\,dt \geq 0. \tag{10}$$

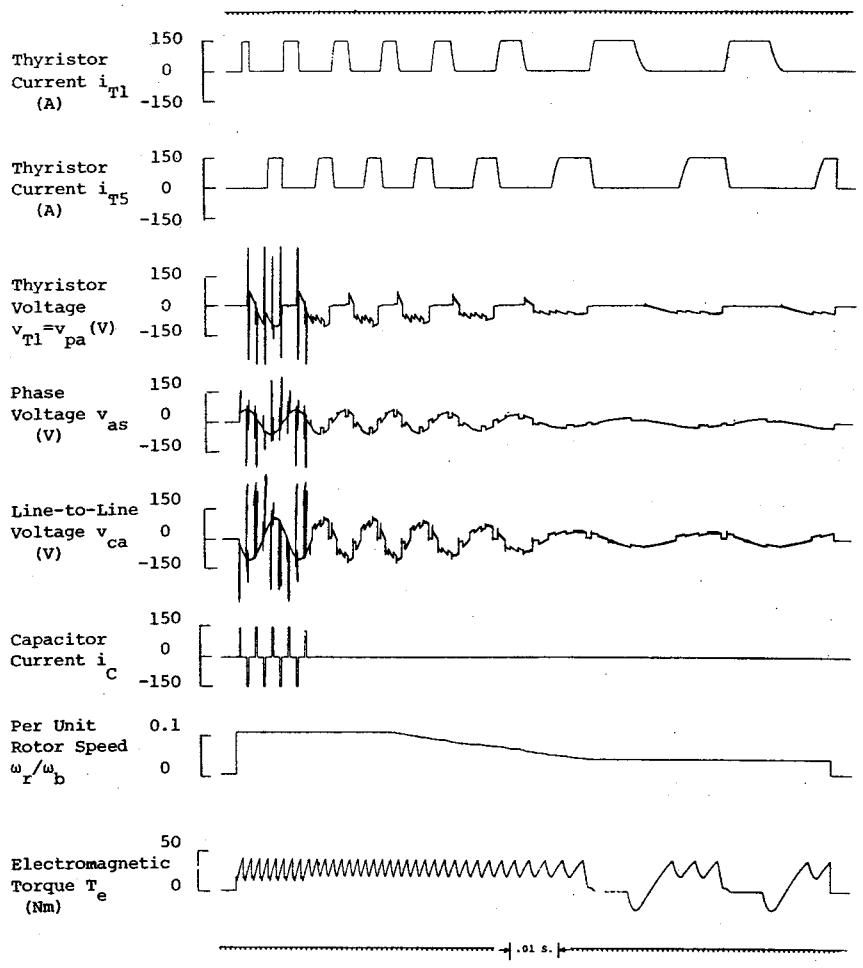

Fig. 15. Effect of decreasing rotor speed on load commutation with fixed dc link current.

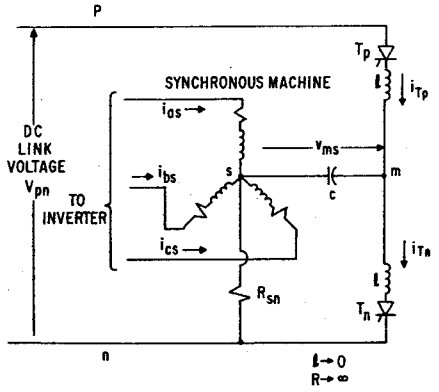

Fig. 16. Equivalent circuit for commutation circuit simulation.

The voltage across the commutation capacitor is computed as

$$v_{ms} = \frac{1}{C}\int (i_{Tp} - i_{Tn})\,dt. \tag{11}$$

These equations are simulated in Fig. 17. The integrators for i_{Tp} and i_{Tn} are gated in the simulation from the identical arrangement logic circuits illustrated in Fig. 3. Additional gating logic is not needed since the auxiliary thyristor currents naturally go to zero and remain at zero as the commutating capacitor charges. The limiters around the integrators ensure unidirectional auxiliary thyristor current.

APPENDIX B
ANALYSIS OF COMMUTATION

In this analysis it is assumed that the counter EMF changes a negligible amount during the commutation interval. Thus the counter EMF can be assumed constant for a given α.

Stage 1

Thyristor $T2$ is conducting, and $T4$ does not conduct during this interval. Referring to Fig. 2

$$L_k\frac{di_{c2}}{dt} - \frac{1}{C}\int i_c\,dt - e_3 = 0. \tag{12}$$

Solution of this equation under the constraint

$$i_c + i_{c2} = I_d$$

and the initial conditions

$$i_{c2}(0) = I_d;\ v_{ms}(0) = V_c$$

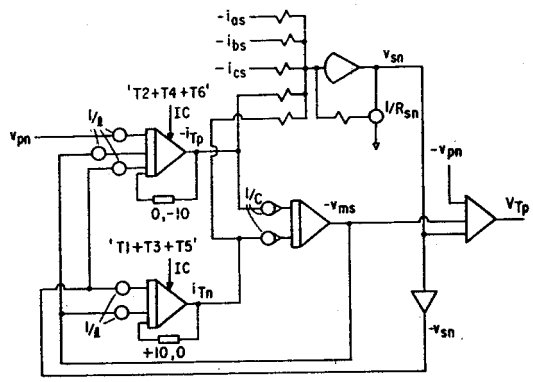

Fig. 17. Simulation diagram for third harmonic auxiliary commutation circuit.

results in

$$i_{c2} = I_d - \frac{V_c - e_3}{\sqrt{L_k/C}} \sin\ (t/\sqrt{L_kC}) \tag{13}$$

where $e_3 = -E_M \sin\ (\alpha - \pi/6)$. The duration of Stage 1 is found by solving 13 for $i_{c2} = 0$:

$$t_1 = \sqrt{L_kC}\ \sin^{-1}\left[\frac{I_d\sqrt{L_k/C}}{V_c + E_M \sin\ (\alpha - \pi/6)}\right]. \tag{14}$$

The capacitor voltage at the end of Stage 1 is found from

$$v_{sm}(t_1) = -V_c + \frac{1}{C}\int_0^{t_1}\left(\frac{V_c - e_3}{\sqrt{L_k/C}}\right)\cdot \sin\frac{t}{\sqrt{L_kC}}\,dt \tag{15}$$

where t_1 is given by (14).

Stage 2

Stage 2 starts when the entire link current is in the commutation capacitor C and lasts until the capacitor voltage equals the counter EMF e_1 (no delayed gating) or until $T4$ is fired (delayed gating), whichever is longer. During Stage 2 the capacitor voltage changes linearly

$$\frac{dv_{sm}}{dt} = \frac{I_d}{C}. \tag{16}$$

Note that the reapplied dv/dt to T2 is

$$\frac{dv}{dt} = \frac{I_d}{C} + \frac{de_3}{dt} = \frac{I_d}{C} - 2\pi f E_M \cos\ (\alpha - \pi/6) \tag{17}$$

where f is the frequency of the counter EMF.

Stage 3

During Stage 3, $T2$ is off, and $T4$ is conducting. Referring to Fig. 2,

$$L_k\frac{di_{a2}}{dt} - e_1 - \frac{1}{C}\int_0^t i_C\,dt = 0. \tag{18}$$

Under the constraint $i_{a2} + i_C = I_d$ and the initial conditions $i_{a2}(0) = 0$, $v_{ms}(0) = e_1$ (no delayed gating), the solution is

$$i_C = I_d \cos\ (t/\sqrt{L_kC}) \tag{19}$$

$$i_{a2} = I_d[1 - \cos\ (t/\sqrt{L_kC})]. \tag{20}$$

Stage 3 lasts until $i_C = 0$. The duration of Stage 3 is, from (19),

$$t_3 = \frac{\pi}{2}\sqrt{L_kC}. \tag{21}$$

The capacitor voltage is

$$v_{sm} = -E_M \sin\ (\alpha + \pi/6) + \frac{1}{C}\int_0^t I_d \cos\ (t/\sqrt{L_kC})\,dt$$

$$= -E_M \sin\ (\alpha + \pi/6) + \frac{I_d}{C}\sqrt{L_kC}\sin\ (t/\sqrt{L_kC}). \tag{22}$$

Substituting (21) into (22) gives the peak capacitor voltage V_c as

$$V_c = -E_M \sin\ (\alpha + \pi/6) + I_d\sqrt{\frac{L_k}{C}}\ \text{(no delayed gating)}. \tag{23}$$

For delayed gating a similar analysis applies, but with the initial condition

$$v_{sm}(0) = V_{\text{ref}} > -e_1. \tag{24}$$

In (24) V_{ref} is the capacitor threshold voltage at which $T4$ is fired. The peak capacitor voltage becomes

$$V_c = \sqrt{[V_{\text{ref}} + E_M \sin\ (\alpha + \pi/6)]^2 + I_d^2(L_k/C)}$$
$$-E_M \sin\ (\alpha + \pi/6)\quad \text{(delayed gating)}. \tag{25}$$

The ranges of α for which delayed gating is not required can be found by observing that for commutation to be successful the minimum value of i_{c2} as given in (13) must be less than or equal to zero. This is equivalent to the constraint

$$I_d - \frac{V_c - e_3}{\sqrt{L_k/C}} < 0. \tag{26}$$

Substituting $-E_M \sin\ (\alpha - \pi/6)$ for e_3 and (22) for V_c in this inequality, results in

$$\sin\ (\alpha - \pi/6) > \sin\ (\delta + \pi/6), \tag{27}$$

which has the solution

$$90° < \alpha < 270°. \tag{28}$$

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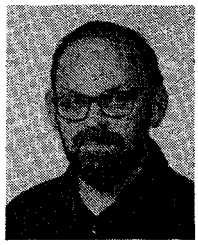

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