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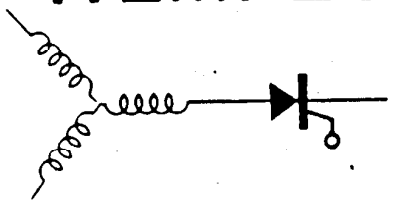

Wisconsin Electric Machines and Power Electronics Consortium

RESEARCH REPORT
82-1

Hybrid Computer Simulation of an ASCI Current Source Inverter

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April 1982

HYBRID COMPUTER SIMULATION OF AN ASCI CURRENT SOURCE INVERTER

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Abstract

A hybrid computer representation of a current source inverter is described. The inverter is modeled in considerable detail so that the simulation is suitable to portray double overlap, discontinuous current operation and other abnormal modes of inverter behavior. Both system equations and simulation diagarams are included. Several computer runs are shown to illustrate the simulation of typical inverter operation.

Introduction

Recently, the use of adjustable speed AC motor drives in conjunction with inverters which approximate current rather than voltage sources have been increasingly employed in industry. The most widely utilized current source inverter configuration is the auto sequentially commutated inverter or ASCI inverter described originally by Ward[1]. To date, work has concentrated mainly on the prediction of circuit behavior of this configuration and the development of control strategies for use in controlling AC machines[2-4].

At present, abnormal modes of system behavior arising from the use of current source inverters have, in the large, gone uninvestigated since they are difficult to analyze. Many of the conventional techniques for analyzing steady state phenomena presently heavily utilize the symmetry inherent in the three phase inverter waveshape[5]. However, when the inverter is unbalanced due to an unbalance in load or firing condition such symmetry is no longer available and the solution becomes hopelessly complex. In this case the analyst must rely upon implicit integration of the system equations using simulation to obtain the desired solution. This paper realizes such a simulation tool which will facilitate the study of a wide variety of transient as well as abnormal steady-state motor drive phenomena.

Although simulation models for current source inverters have appeared in the literature, the switching is often idealized in order to reduce the complexity of the simulation. In particular, the author has reported two such simulations in the past. In the first simulation, the commutation phenomena was neglected completely and the inverter treated as an ideal switch having a transport lag representing the commutation time[6]. The commutation interval was approximated by replacing the commutation capacitors with a ficticious resistor which resulted in the same equivalent current transfer time. The second simulation accurately modeled the commutation phenomena by the use of an equivalent

capacitor which accomplished the commutations produced by all six of the ASCI commutation capacitors[7]. However, two important limitations inherent in this approach is that the load remains balanced and that the commutation intervals never exceed 60°. That is, double overlap never occurs. These limitations are precisely those which are to be overcome in this paper. Digital computer simulation algorithms have also appeared in the literature[8]. However, turn around time continues to be a difficulty with such approach and often prevents a digital simulation from being a true engineering design tool.

Inverter Description and Equivalent Circuit

The auto-sequential type of controlled current inverter which is to be modeled is shown in Fig. 1. Although any load is possible, the inverter will be analyzed, for purposes of convenience, connected to a passive R-L load. The inverter consists of two groups of three thyristors. Delta connected commutating capacitors C1-C6, all of the same value, serve to provide the necessary reverse voltage needed to turn off each thyristor. Since voltages which can exceed the DC supply are built up on the commutating capacitors, diodes D1-D6 isolate the commutating capacitors from the load preventing their discharge after commutation. Each thyristor and diode carries the full load current for approximately 120° of the fundamental output period so that during commutation, current overlap between adjacent motor phases occurs as current transfer takes place. The commutating capacitors carry load current only during commutation intervals. Neglecting overlap periods, one phase of the load is always disconnected from the source.

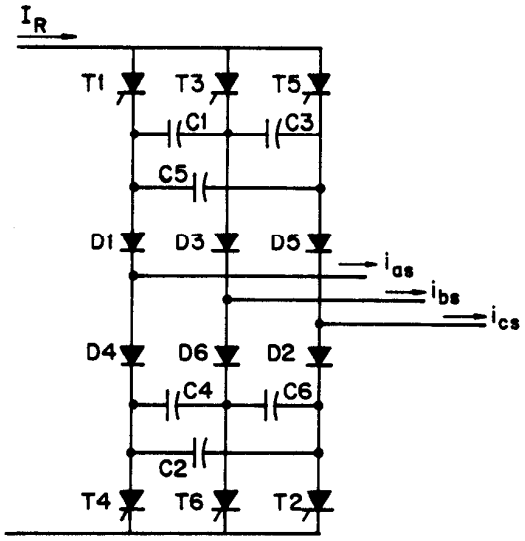


Fig. 1 Current Source Inverter with Auto-Sequential Commutation

A typical sketch showing load waveforms is given in Fig. 2. It can be noted that when overlap exceeds 60° current will be commutated in both the top and bottom half bridges producing a temporary "short circuit" path in shunt with the load. Also, because of the inductive nature of the load and the rapid commutation of current between phases, spikes of voltage are produced across each phase the amplitude of which must be carefully evaluated in a practical application. For accurate prediction of both of these effects, a detailed representation of the inverter is clearly required.

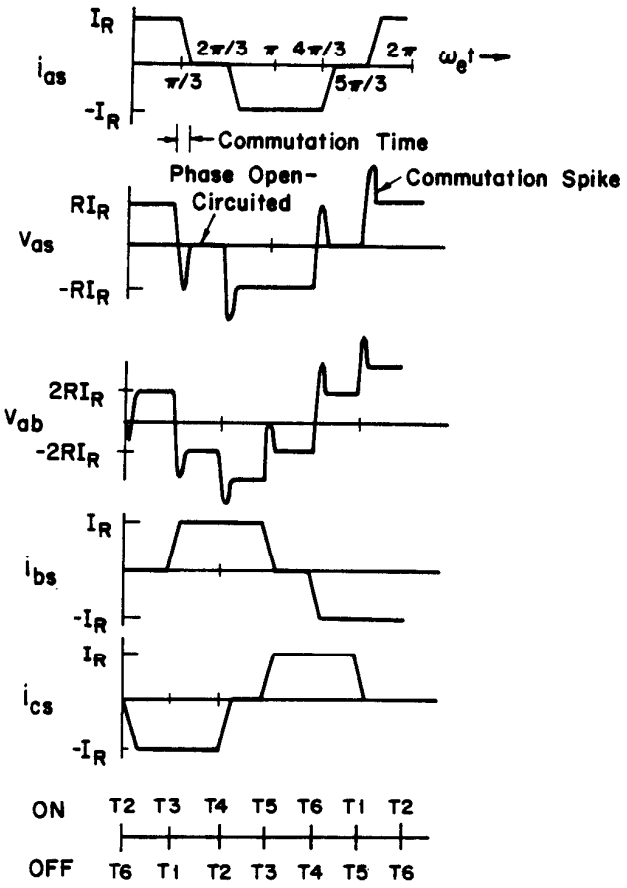


Fig. 2 Expected Waveforms for R-L Load

In order to write a sufficient number of independent equations to describe the system, the inverter can be modeled by the equivalent circuit shown in Fig. 3. The elements R_{km}, $R_{\ell m}$, R_{am}, R_{bm}, and R_{cm} in Fig. 3 are artificial resistors having a large numerical value (approximately 20 per unit) and are needed to define the load or motor terminal voltages with respect to the neutral reference. Although ficticious, it has been demonstrated in previous simulations that these resistors have a negligible effect on system behavior[7].

It can be noted that the pair of delta connected capacitors have been replaced by two wye connected capacitor banks. Since the inverter always operates in a piecewise linear fashion, it can be shown that the same response will be always realized if the capacitor associated with the wye connected bank is three times that of the delta connected system. It should be mentioned that the conversion from delta to wye connected capacitors was made in order to eliminate an unstable algebraic loop which arises whenever three passive elements are connected in a closed loop.

The circuit has also been modified by inserting small inductors in series with each diode so as to permit a means of developing the current through each diode element during conduction. (A small resistor could also have been used). Since the inductance is assumed neglibibly small, this element also has negligible effect on the solution. In practice, this quantity could be scaled to represent stray lead inductance.

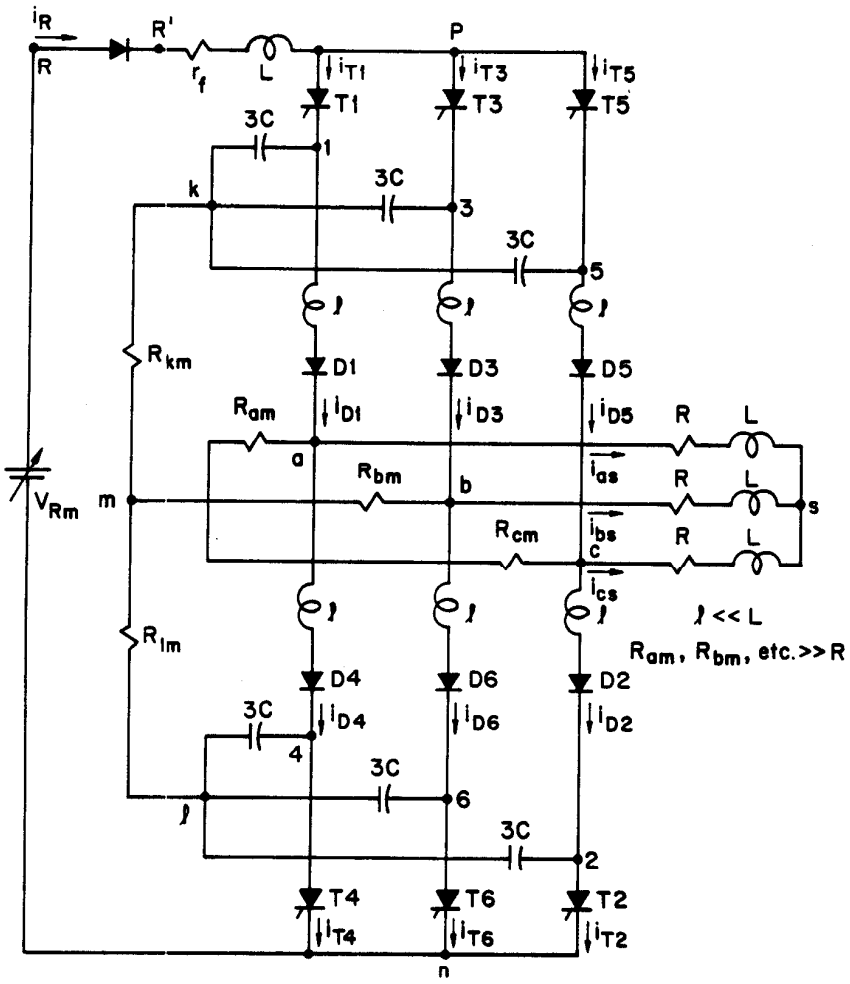


Fig. 3 Network Modified for Simulation Purposes

It can be noted that a DC filter inductor has been incorporated in the simulation. Hence, a constant current source has not been assumed. The inverter is permitted to function as an approximate constant current source with ripple components appearing in the DC side current due to the switching of the inverter. In the simulation, the input DC voltage V_R has been modeled as an idealized, adjustable amplitude DC voltage. In practical applications this voltage is typically the output of a thyristor bridge. The addition of such an AC-DC bridge produces additional ripple current in the DC current. In some cases, the DC current can even become discontinuous which results in additional modes of operation in so far as the inverter is concerned. Although the possibility of discontinuous DC current was included in the simulation, the operation of the AC-DC bridge was idealized. This component can be accurately modeled, if necessary, using previously developed techniques[9].

System Equations

The equations which describe behavior of the system are, in general, derived by inspection of the equivalent circuit, Fig. 3. The equations which describe behavior of the DC choke are

$$V_{R'n}(t) = V_{pn} \text{ if } I_R(t^-) < \varepsilon \tag{1}$$

$$V_{R'n}(t) = V_{Rn} \text{ if } V_{Rn} > V_{pn} \tag{2}$$

$$I_R = \frac{\omega_b}{X_f} \int (V_{R'n} - V_{pn} - r_f I_R)\, dt \tag{3}$$

where

$X_f = \omega_b L_f$, and $\varepsilon \to 0$.

The model of the thyristors are obtained by reference to Fig. 2. Let P1,...,P6 be ideal 120° gate pulses, and T1,...,T6 be logic pulses corresponding to on-off state of the thyristors. T1 = 1 if thyristor #1 is conducting, T1 = 0 if thyristor #1 is off, etc. Then

$$T1 = 1 \text{ if } P1 = 1 \text{ and } T5 = 1 \text{ and } V_{51} > 0 \tag{4}$$

$$T3 = 1 \text{ if } P3 = 1 \text{ and } T1 = 1 \text{ and } V_{13} > 0 \tag{5}$$

$$T5 = 1 \text{ if } P5 = 1 \text{ and } T3 = 1 \text{ and } V_{35} > 0 \tag{6}$$

$$T2 = 1 \text{ if } P2 = 1 \text{ and } T6 = 1 \text{ and } V_{62} < 0 \tag{7}$$

$$T4 = 1 \text{ if } P4 = 1 \text{ and } T2 = 1 \text{ and } V_{24} < 0 \tag{8}$$

$$T6 = 1 \text{ if } P6 = 1 \text{ and } T4 = 1 \text{ and } V_{46} < 0 \tag{9}$$

$$i_{T1} = i_R \text{ if } T1 = 1;\ i_{T1} = 0 \text{ if } T1 = 0 \tag{10}$$

$$i_{T3} = i_R \text{ if } T3 = 1;\ i_{T3} = 0 \text{ if } T3 = 0 \tag{11}$$

$$i_{T5} = i_R \text{ if } T5 = 1;\ i_{T5} = 0 \text{ if } T5 = 0 \tag{12}$$

$$i_{T2} = i_R \text{ if } T2 = 1;\ i_{T2} = 0 \text{ if } T2 = 0 \tag{13}$$

$$i_{T4} = i_R \text{ if } T4 = 1;\ i_{T4} = 0 \text{ if } T4 = 0 \tag{14}$$

$$i_{T6} = i_R \text{ if } T6 = 1;\ i_{T6} = 0 \text{ if } T6 = 0 \tag{15}$$

$$V_{pm} = V_{1m} \text{ if } T1 = 1 \tag{16}$$

$$V_{pm} = V_{3m} \text{ if } T3 = 1 \tag{17}$$

$$V_{pm} = V_{5m} \text{ if } T5 = 1 \tag{18}$$

$$V_{nm} = V_{2m} \text{ if } T2 = 1 \tag{19}$$

$$V_{nm} = V_{4m} \text{ if } T4 = 1 \tag{20}$$

$$V_{nm} = V_{6m} \text{ if } T6 = 1 \tag{21}$$

Note that to realize Eqs. 16-18, logic signals T1, T3 and T5 must be mutually exclusive. Similarily to realize Eqs. 19-21, logic variables T2, T4 and T6 must be mutually exclusive.

The voltages across the six capacitors are found by integrating the voltages across the six equivalent wye connected capacitors. That is,

$$V_{1k} = 3\omega_b X_c \int (i_{T1} - i_{D1})\, dt \tag{22}$$

$$V_{3k} = 3\omega_b X_c \int (i_{T3} - i_{D3})\, dt \tag{23}$$

$$V_{5k} = 3\omega_b X_c \int (i_{T5} - i_{D5})\, dt \tag{24}$$

$$V_{2\ell} = 3\omega_b X_c \int (i_{D2} - i_{T2})\, dt \tag{25}$$

$$V_{4\ell} = 3\omega_b X_c \int (i_{D4} - i_{T4})\, dt \tag{26}$$

$$V_{6\ell} = 3\omega_b X_c \int (i_{D6} - i_{T6})\, dt \tag{27}$$

where $X_c = 1/(\omega_b C)$.

The diode currents are defined by

$$i_{D1}(t) = 0 \text{ if } i_{D1}(t^-) < \varepsilon \text{ and } V_{1m} < V_{cm}$$
$$i_{D1} = \frac{\omega_b}{X_\ell} \int (V_{1m} - V_{am})\, dt \text{ otherwise} \tag{28}$$

$$i_{D3}(t) = 0 \text{ if } i_{D3}(t^-) < \varepsilon \text{ and } V_{3m} < V_{bm}$$
$$i_{D3} = \frac{\omega_b}{X_\ell} \int (V_{3m} - V_{bm})\, dt \text{ otherwise} \tag{29}$$

$$i_{D5}(t) = 0 \text{ if } i_{D5}(t^-) < \varepsilon \text{ and } V_{5m} < V_{cm}$$
$$i_{D5} = \frac{\omega_b}{X_\ell} \int (V_{5m} - V_{cm})\, dt \text{ otherwise} \tag{30}$$

$$i_{D2}(t) = 0 \text{ if } i_{D2}(t^-) < \varepsilon \text{ and } V_{2m} > V_{cm}$$
$$i_{D2} = \frac{\omega_b}{X_\ell} \int (V_{cm} - V_{2m})\, dt \text{ otherwise} \tag{31}$$

$$i_{D4}(t) = 0 \text{ if } i_{D4}(t^-) < \varepsilon \text{ and } V_{4m} > V_{am}$$
$$i_{D4} = \frac{\omega_b}{X_\ell} \int (V_{am} - V_{4m})\, dt \text{ otherwise} \tag{32}$$

$$i_{D6}(t) = 0 \text{ if } i_{D6}(t^-) < \varepsilon \text{ and } V_{6m} > V_{bm}$$
$$i_{D6} = \frac{\omega_b}{X_\ell} \int (V_{bm} - V_{6m})\, dt \text{ otherwise} \tag{33}$$

In Eqs. 28-33, ε is an arbitrarily small quantity and $X_\ell = \omega_b \ell$.

The voltages to neutral are needed to complete the solution for the voltages across the inverter bridge.

$$V_{km} = R_{km}(i_{T1} + i_{T3} + i_{T5} - i_{D1} - i_{D3} - i_{D5}) \quad (34)$$

$$V_{\ell m} = R_{\ell m}(i_{D2} + i_{D4} + i_{D6} - i_{T2} - i_{T4} - i_{T6}) \quad (35)$$

$$V_{1m} = V_{1k} + V_{km} \quad (36)$$

$$V_{3m} = V_{3k} + V_{km} \quad (37)$$

$$V_{5m} = V_{5k} + V_{km} \quad (38)$$

$$V_{2m} = V_{2\ell} + V_{\ell m} \quad (39)$$

$$V_{4m} = V_{4\ell} + V_{\ell m} \quad (40)$$

$$V_{6m} = V_{6\ell} + V_{\ell m} \quad (41)$$

$$V_{am} = R_{am}\,(i_{D1} - i_{D4} - i_{as}) \quad (42)$$

$$V_{bm} = R_{bm}\,(i_{D3} - i_{D6} - i_{bs}) \quad (43)$$

$$V_{cm} = R_{cm}\,(i_{D5} - i_{D2} - i_{cs}) \quad (44)$$

Finally expressions are required to define the load quantities. In a practical application the load would generally consist of an induction motor and can be modelled by conventional techniques[10]. It is assumed for simplicity that the load is a simple R-L load. The equations which are needed to define such a load are

$$V_{sm} = \frac{1}{3}\,(V_{am} + V_{bm} + V_{cm}) \quad (45)$$

$$V_{as} = V_{am} - V_{sm} \quad (46)$$

$$V_{bs} = V_{bm} - V_{sm} \quad (47)$$

$$V_{cs} = V_{cm} - V_{sm} \quad (48)$$

$$i_{as} = \frac{\omega_b}{X} \int (V_{as} - Ri_{as})\,dt \quad (49)$$

$$i_{bs} = \frac{\omega_b}{X} \int (V_{bs} - Ri_{bs})\,dt \quad (50)$$

$$i_{cs} = \frac{\omega_b}{X} \int (V_{cs} - Ri_{cs})\,dt \quad (51)$$

where $X = \omega_b L$.

Description of the Simulation

The simulation diagrams resulting from the equations of the previous section are given in Figs. 4-8. Fig. 4 shows the simulation of the filter choke together with the model of the six thyristors. Figure 5 shows the logic required to trigger each thyristor. Although it would be inappropriate to describe each element in detail, a number of blocks are not entirely standard. The square box in the feedback of high gain amplifiers in Fig. 4 represent limiters which were included to clip excess voltage spikes which sometimes occur during startup. The diamonds shown in Fig. 4 correspond to logic controlled D/A switches. The switch is closed when the logic input is one and is opened when the logic is zero.

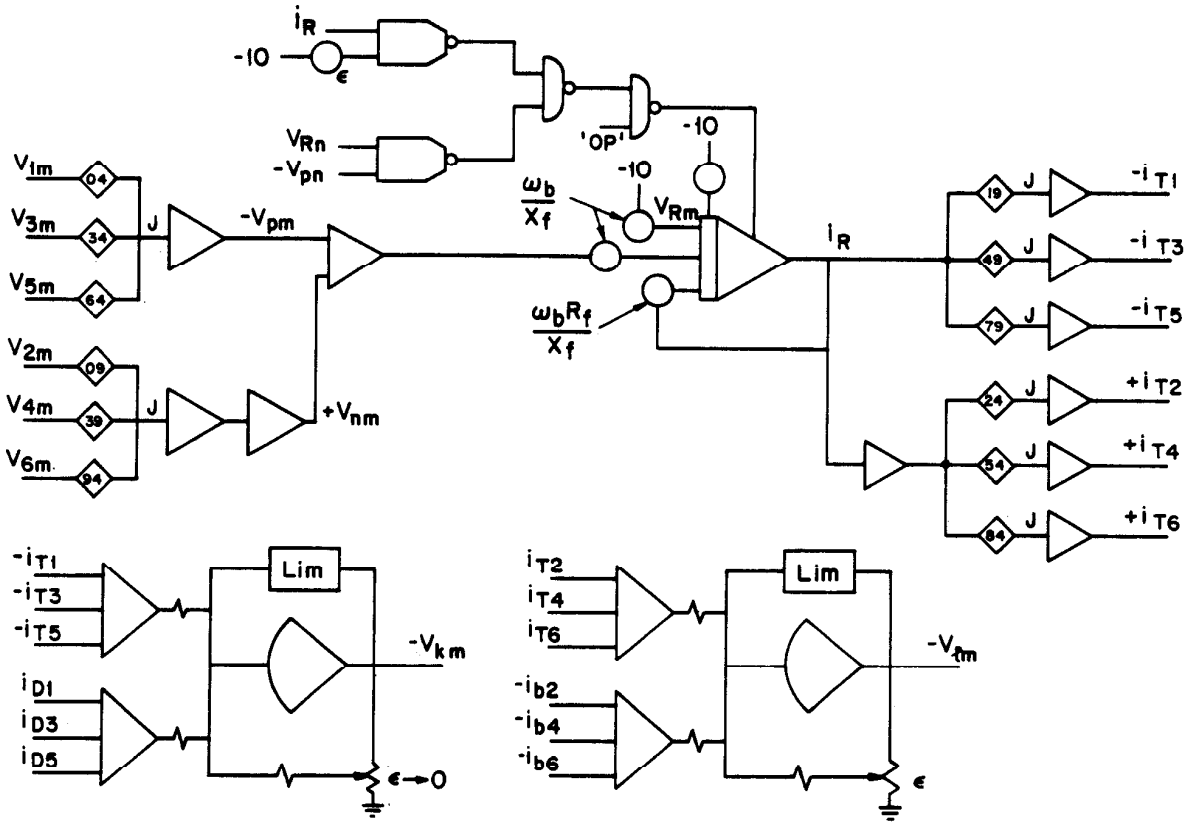


Fig. 4 Thyristor and DC Link Currents

The upper portion of Fig. 5 is an implementation of a variable frequency pulse generator which forms the input to a six bit ring counter. The timing of the pulse generator is adjusted by the input to the integrator. The six bit ring counter is fed to a logic complement which forms idealized trigger pulses of 120° duration. These pulses are fed to a flip-flop arrangement which implements Eqs. 4-9. Note that only one of the three quantities T1, T3 and T5 can be high at any one time. This constraint is needed to realize Eqs. 16-21. A similar statement applies to the logic for the bottom group.

In Fig. 6 is shown the simulation for the diode currents. The size of the equivalent lead inductance was chosen to be 1/100 that of the load inductance ℓ with good success. Note that mode control is used to hold each integrator which represents diode current in initial condition whenever the diode is in the blocking mode.

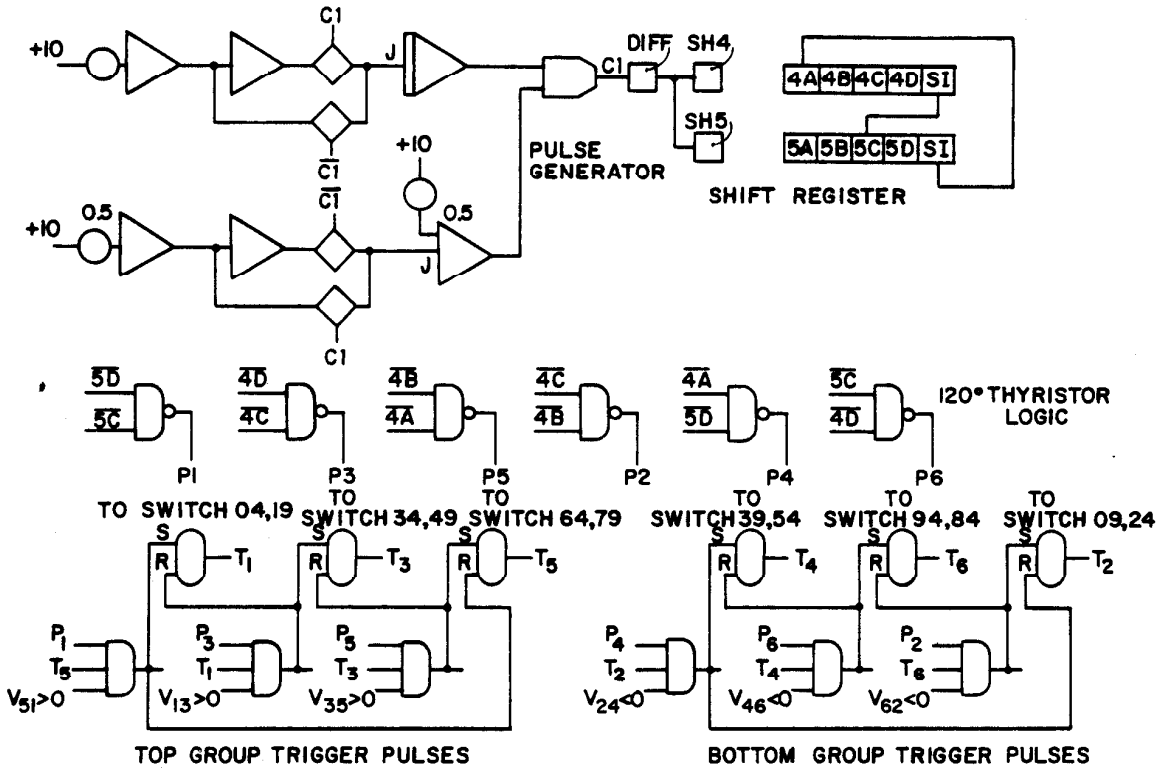


Fig. 5 Thyristor Logic

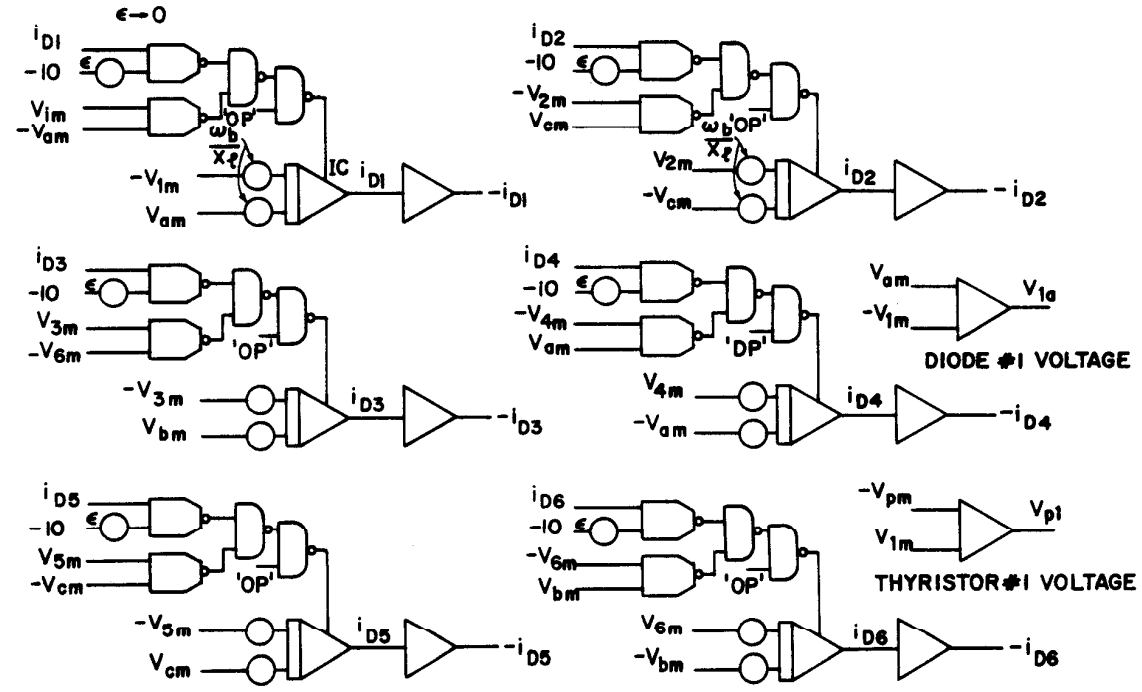


Fig. 6 Diode Currents

The six commutating capacitor voltages are illustrated in Fig. 7. Note that since the equivalent capacitors are wye connected, the line to line voltages must be developed algebraically. These equations are quite obvious and they were not written out explicitly in the previous section.

The voltages to neutral together with the representation of the load is shown in Fig. 8. For simplicity, a simple passive R-L load has been assumed. The representation of this load is given between the two dashed lines in Fig. 8. If necessary, the simulation for any type of three phase load can be substituted including active loads such as an induction or synchronous motor[10]

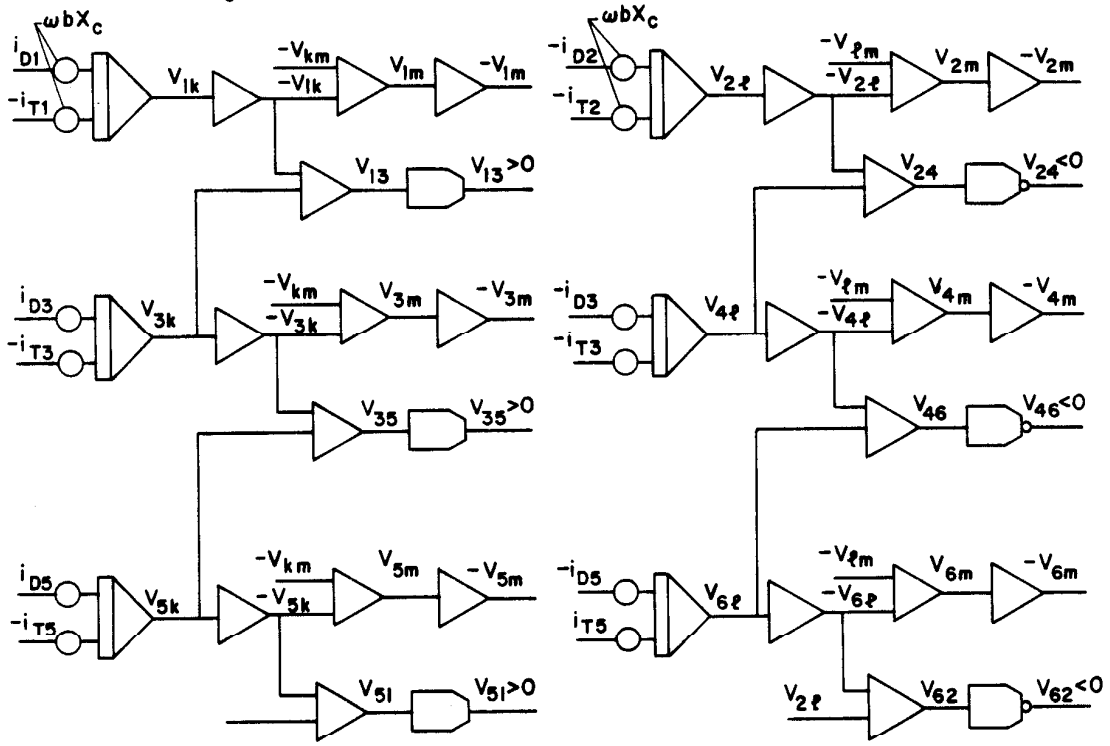


Fig. 7 Capacitor Voltages

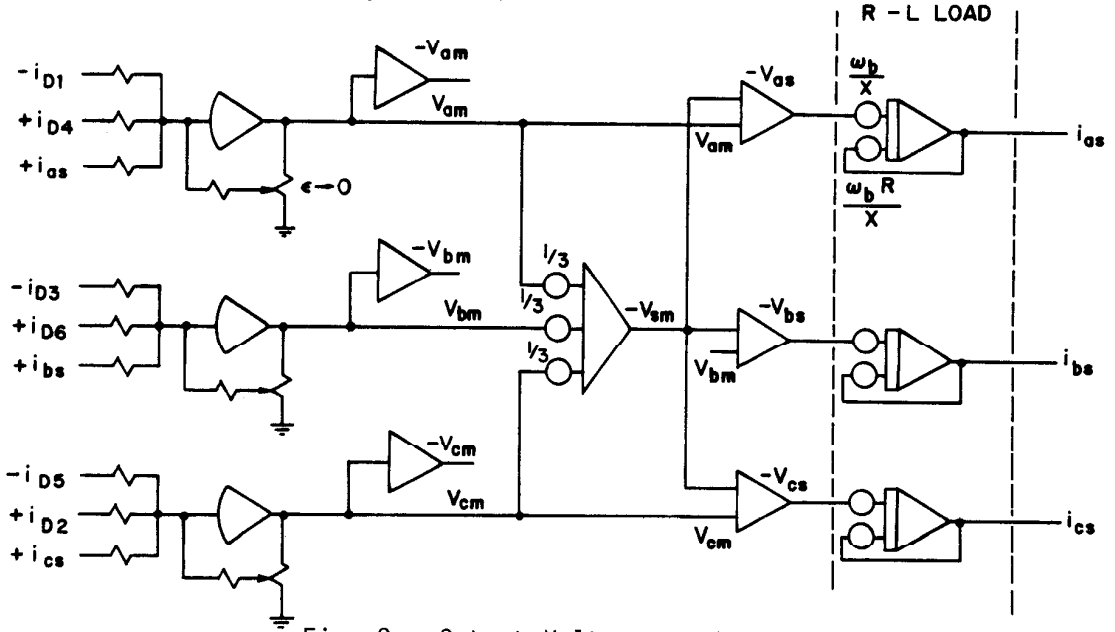


Fig. 8 Output Voltages and Load Currents

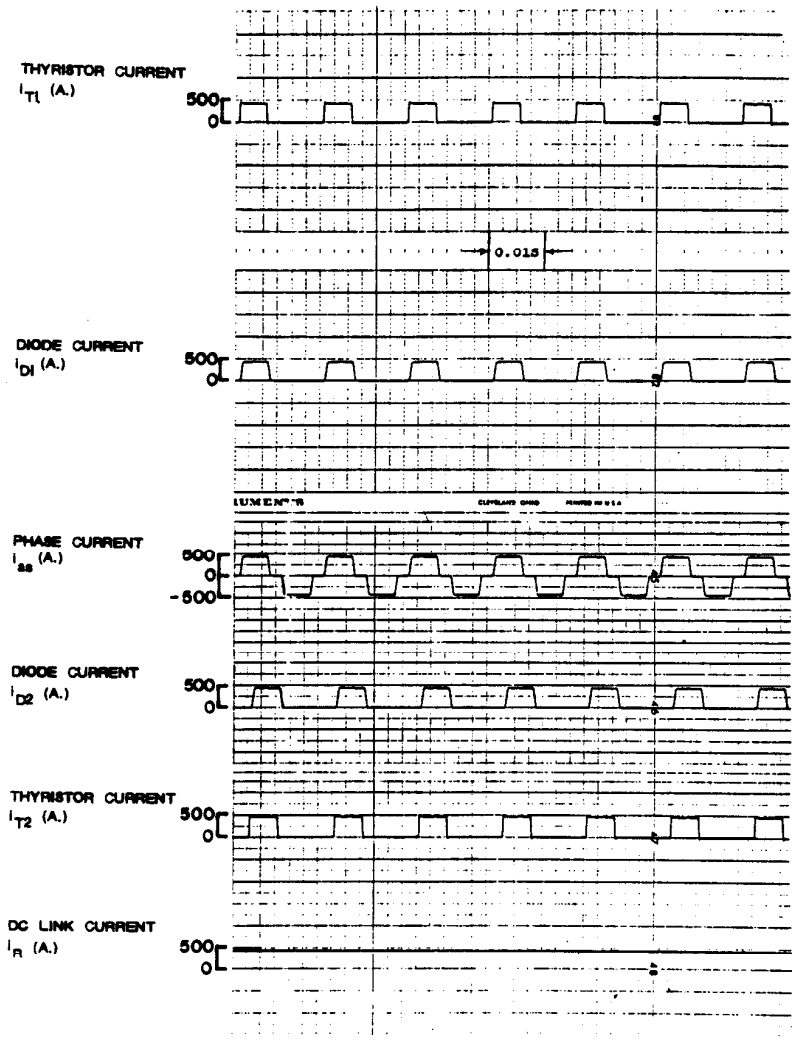
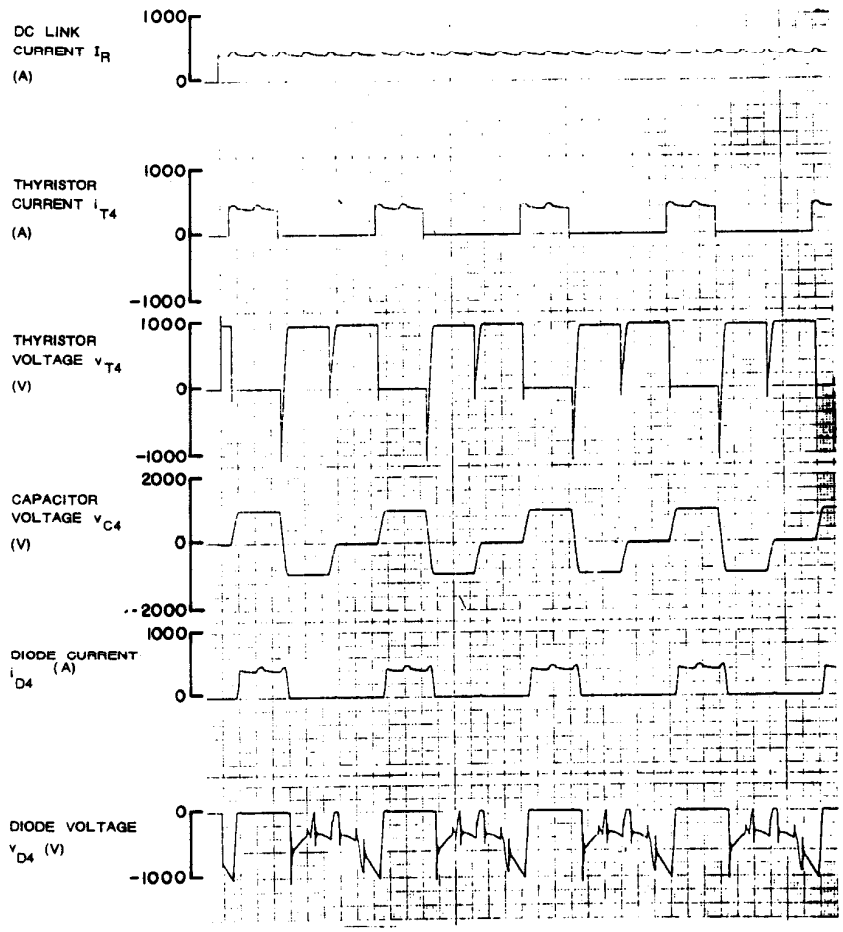


Fig. 9b Response of Current Source Inverter with Passive R-L Load at 66 Hz Showing System Currents.

In Figs. 10 and 11 the passive load has been replaced by an active induction motor load. Figure 10 shows system variables for no load operation at 45 Hz. The characteristic notches in the motor line and phase voltages can be noted. Of particular interest is the capacitor voltage, the thyristor voltage and the diode voltage which yields important information on sizing these components. In general, these simulation results have been found to show good correlation with previously published data .

In Fig. 11 the frequency has been increased to 80 Hz. which represents the 120° overlap condition for the motor parameters chosen. Examination of the commutating capacitor voltage indicates a nearly triangular waveshape which indicates that commutations are continously occuring. Note also the large ripple component of current that exists as the 120° overlap condition is approached.



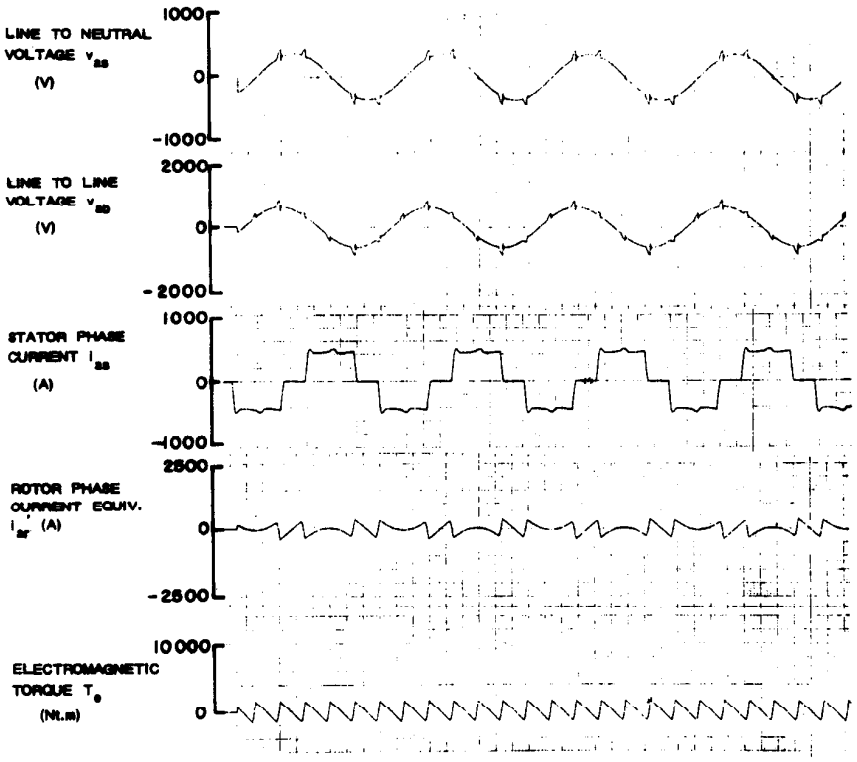


Fig. 10 ASCI Inverter Feeding Induction Motor Operating at No Load and at Base Frequency (45 Hz).

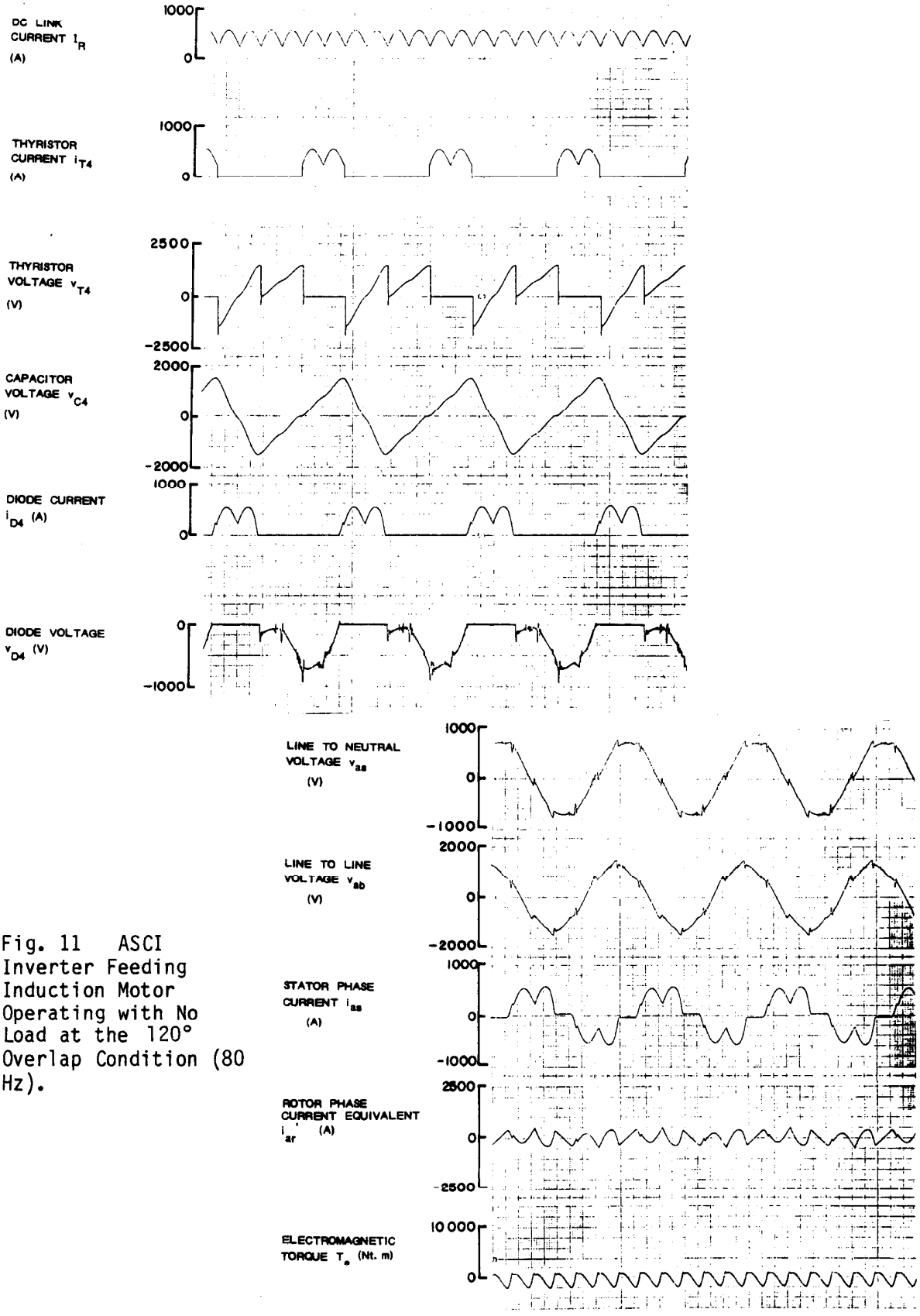


Fig. 11 ASCI Inverter Feeding Induction Motor Operating with No Load at the 120° Overlap Condition (80 Hz).

Conclusion

A detailed hybrid computer simulation of a controlled current ASCI inverter has been described. Several computer runs were included to verify the analysis. The simulation is particularly useful in the investigation of abnormal phenomena such as double overlap, discontinuous current operation and thyristor misfire. Because of the extensive use of computer components, it appears that this simulation will be practical only on a large scale analog computer having a complete logic complement. However, the approach which has been described is not restricted to analog computation and can be directly implemented in digital form by using any of a number of simulation software such as ACSL, CSSL IV or SuperSceptre.

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