The College of Engineering
University of Wisconsin-Madison

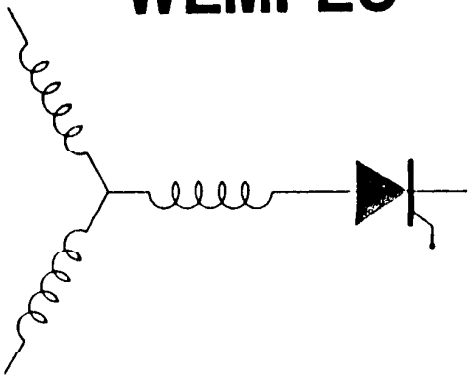
Wisconsin Electric Machines and Power Electronics Consortium

RESEARCH REPORT
86-18

Power Conversion Distribution System Using a Resonant High Frequency AC Link

Pradeep K. Sood and Thomas A. Lipo
Department of Electrical and Computer Engineering
University of Wisconsin
1415 Johnson Drive
Madison, Wisconsin 53706

WEMPEC



Department of Electrical and Computer Engineering
1415 Johnson Drive
Madison, Wisconsin 53706

POWER CONVERSION DISTRIBUTION SYSTEM USING A RESONANT HIGH FREQUENCY AC LINK

Pradeep K. Sood and Thomas A. Lipo
University of Wisconsin
1415 Johnson Drive
Madison, Wisconsin 53706

Abstract – A power conversion system configuration based on a 20 kHz, single-phase voltage link is proposed for systems having distributed power requirements. The proposed configuration permits flexibility in the choice of voltage levels in the system without the penalty of bulky magnetic components, has a fast system response, high efficiency, freedom from acoustic noise, and provides a high degree of uniformity and ease of implementation. A zero-voltage switching pulse-density-modulated converter is proposed as the basic interface converter. It is shown that the technique of pulse-density-modulation (PDM) allows low distortion synthesis of fixed or variable amplitude dc and fixed or variable frequency, single- or three-phase ac from the half-cycle pulses of the link voltage. A breadboard system has been built to experimentally verify the models and to complement the theoretical work.

INTRODUCTION

High frequency link power converters are receiving increasing attention as an alternative to more conventional dc link power conversion systems. Use of a high frequency ac voltage link in a power conversion system permits adjustment of the link voltage to meet the individual needs of loads/sources in the system, allows stepping up of the voltage in sections, and realizes electrical isolation by using transformers on the link side of the interface converters. This flexibility can be very useful in system design, particularly in distributed power conversion systems where voltage levels can vary widely due to the need to integrate a wide variety of loads and sources into the system. By operating the link at a high frequency, the system can be made compact because of the large reduction in the size and the weight of the transformers and the passive components needed for filtering and temporary energy storage functions. High frequency operation also speeds up the system response and, if the frequency is above the audible range, reduces acoustic noise.

High-frequency link power conversion has been employed very successfully in dc-to-dc converters. Their enormous success has demonstrated the benefits and to some extent the difficulties of working at high frequencies. In particular, problems arise from the limitations of both the components and the circuit topologies. As the demand has grown and the technology has matured, there has been a large improvement in the quality of components. High quality capacitors, good magnetic materials for design of compact low-loss inductors and transformers, and the semiconductors devices designed especially for high-speed power applications have become available. This trend can be expected to continue with further improvements in performance and even larger gains in the cost and availability of these components. As the understanding of dc-dc converters has grown, circuit topologies optimized for high-frequency conversion have been evolving. Application of resonant converters, known and used for induction heating for quite some time [1,2], to the field of dc-to-dc power conversion is an excellent example of this evolutionary process [3-8].

A number of high-frequency link systems have also been proposed for dc-to-ac and ac-to-ac power conversion [9-13]. Nearly all of these systems use the favorable switching characteristics of resonant converters to realize dedicated conversion systems. The majority of the configurations, however, are not suitable for power conversion systems having more than one type of load and source. The work reported by Espelage and Bose [14] and Gyugyi and Cibulka [15] are notable exceptions. Espelage and Bose have proposed a single-phase voltage link operating at a frequency of 2 to 4 kHz with naturally-commutated phase angle controlled cycloconverters used to interface dc or ac loads/sources. System reported by Gyugyi and Cibulka uses a three-phase 400 Hz high power link and is intended for power system applications such as intertying power systems with different characteristics. The phase angle controlled cycloconverters used in these systems is not suitable for systems where link frequencies are a order of magnitude higher. The major reason for this limitation is the high loss associated with each switching in a phase angle controlled converter. At high frequencies, these losses add up to give a very high value of switching losses in the system. A variable reflected power factor and sharp transients in the generated voltages are the other drawbacks of these converters.

PROPOSED SYSTEM

Figure 1 shows the proposed high-frequency link power conversion system in block schematic form. A single-phase ac voltage link operating at a fixed frequency of 20 kHz or higher interconnects all sources and loads in the system through interface converters and link side transformers as needed. The interface converters operate directly from the bi-directional high-frequency voltage of the link to synthesize low-frequency (including the case of dc as zero frequency) voltage or current source outputs as appropriate for the source/load being interfaced. Converter switching is restricted to the zero crossing points of the link voltage so that the switching losses, which dominate the converter losses at these high-frequencies, do not become excessive. With such constrained switching, one half cycle of the high-frequency voltage becomes the basic unit of synthesis of the low frequency signals. A strategy of pulse-density modulation (PDM) is then used to control the amplitude of the synthesized signal. Average power balance is maintained in the system at all times by matching the power received from the source(s) and the power delivered to the various loads in the system. Resonant LC tank circuits provide the temporary energy storage and ensure near sinusoidal voltage at the link. If desired, a dedicated static converter can be used to start up the resonant link and to share in the temporary energy storage function. However, use of a dedicated excitation converter is not essential because the start up of the link can be performed through the interface converter that is connected to the source.

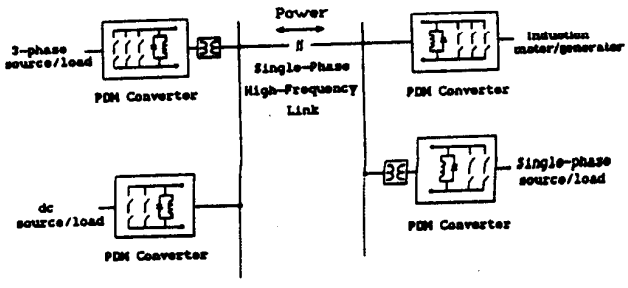


Fig. 1 High Frequency Link Based Static Power Conversion System.

OPERATION AND CHARACTERISTICS OF INTERFACE CONVERTERS

Feasibility of the proposed system depends heavily on the ability of static interface converters to efficiently generate low distortion low-frequency current or voltage signals from the fixed frequency regulated-amplitude voltage of the high-frequency link. The need for high efficiency clearly suggests a one-step power conversion process. Thus, rectifier-inverter type configurations are ruled out because they would fail either the efficiency or the low distortion criteria. Phase-angle controlled cycloconverters have traditionally been used to realize such a one-step conversion from an ac supply. In particular, phase angle control allows continuous control over the frequency and amplitude of the synthesized signals, a feature that is crucial for low-distortion synthesis when the frequency differential is small. However, the high value of loss per switching instant due to both the voltage and current being high during the switching interval will lead to excessive switching losses if phase angle control were to be used at these high frequencies. Another drawback of phase angle control is the varying (lagging if naturally commutated) power factor reflected back to the ac source. A varying value of the reflected power factor as a function of load is very undesirable in a fixed frequency voltage link system since it causes large distortion of the high frequency link voltage waveform. This paper proposes pulse-density- modulated converters for one-step synthesis of low-distortion dc or ac signals of arbitrary waveshapes without the limitations outlined above.

Principle of Pulse Density Modulation

Figure 2 (a) shows the block schematic of an area-comparison pulse-density modulation (AC-PDM) controller. Figure 2(b) shows the associated waveforms when the reference signal is a dc voltage. The power circuit is arranged such that either half- cycle of the high frequency voltage can be passed to the low- frequency end with either polarity. For a positive reference voltage, v^*_{LF} of constant amplitude the logic selects appropriate switches so that half-cycle pulses appear with positive polarity in the synthesized signal v_{LF} (Fig. 2 (b)). A difference integrator produces an error signal, $e(t)$ which is proportional to the integral of the difference between the reference and the synthesized signal. Thus $e(t)$ is a measure of the difference between the area under the two curves. A comparator compares the error signal against a preset threshold, ε. Gating logic then uses the comparator output and the polarity of the command v^*_{LF} to recognize when the area of the synthesized signal has exceeded, in absolute terms, the area of the reference signal and applies the next pulse with the polarity that reduces this difference. With this feedback action, a balance is inherently maintained between the areas under the two curves. This area balance results in the density of the half cycle pulses in the synthesized output being modulated by the amplitude of the reference signal. Hence the term *Area Comparison Pulse Density Modulation (AC-PDM)* is used in this paper to describe this type of converter/ controller.

Although Fig. 2(a) shows voltage feedback directly from the synthesized signal, it is more practical to sense the fixed frequency ac link voltage and then realize from it a scaled value of v_{LF} by applying the same logic that drives the power circuit. When synthesizing currents, of course, the direct feedback of current can be used.

The fundamental relationship of pulse density modulation for voltage synthesis can be written as

$$\frac{e(t)}{K} = \int \left(v^*_{LF}(t) - v_{LF}(t) \right) dt \qquad (1)$$

where K is the total gain associated with the difference integrator. The term on the right is the volt-time area difference of the synthesized and the reference signal. The feedback action of the controller has the effect of reducing this difference to the minimum attainable in a given system. Clearly, if the commanded value of the voltage remains beyond a maximum value then the controller will saturate. This maximum reference signal level, $V^*_{LF\,max}$ can be determined by assuming (then verifying later) that the synthesis errors are small and by equating the volt-time areas.

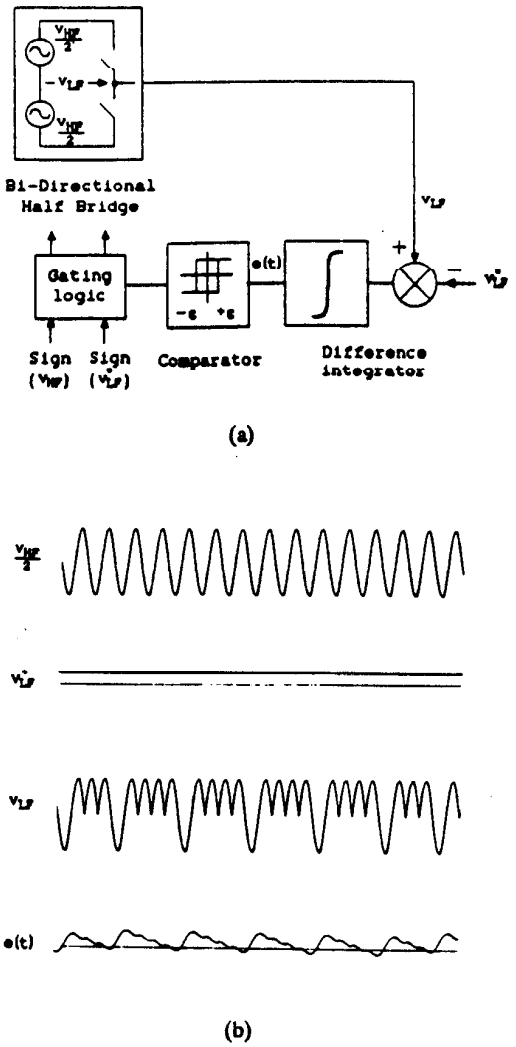


Fig. 2 Area Comparison Pulse Density Modulation (AC-PDM). (a) Block Schematic, (b) Associated Waveforms for the Case of a DC Reference Voltage

Consider first, the case of a dc reference signal synthesized using a half-bridge power circuit. From a volt-time area balance

$$V_{d\,max} = \frac{V_{HF}}{\pi} \qquad (2)$$

where $V_{d\,max}$ is the maximum level of the dc signal that can be synthesized from a high frequency link voltage of peak value V_{HF}. DC voltage levels below this maximum value are then expressed as

$$V_d = m \frac{V_{HF}}{\pi} \qquad (3)$$

where $m = \frac{V_d}{V_{d\,max}}$ is a modulation index which takes on values between zero and one.

Equation 2 still remains essentially valid when an ac voltage is synthesized using a half-bridge circuit. This result occurs because the reference signal changes relatively slowly near its peak and can be considered constant for the duration of several high-frequency pulses. Unsaturated operation in this region then requires that the areas be balanced just as in the case of dc voltage synthesis. Note that the larger the frequency differential the better is this approximation. Thus, for half- bridge operation with no saturation

$$V^*_{LF\,max} = \frac{V_{HF}}{\pi} \qquad \text{if } f_{LF} << f_{HF} \tag{4}$$

If the reference signal amplitude V^*_{LF} is increased steadily beyond this value, the controller becomes increasingly saturated until full saturation is reached at which time the synthesized voltage becomes a square wave composed of rectified half-cycles of the link voltage. Thus, if the increased harmonic distortion is not a problem, the fundamental component synthesized from a given value of the link voltage may be increased beyond the value given in Eq. 4 by a factor of $4/\pi$. Furthermore, the transition into saturation is automatic and gradual as compared to pulse width modulated inverters in which sudden jumps in output voltage fundamental occur when the inverter reaches maximum output.

In establishing the voltage relationships above it has been assumed that the volt-time area error is negligible. To check the validity of this assumption it is useful to examine the nature of the error signal for the case of voltage synthesis. In particular, let ΔA be the volt-time area of one half- cycle of the link voltage. For half-bridge circuit we have

$$\Delta A = \frac{V_{HF}}{2\pi f_{HF}} \tag{5}$$

Also, let ΔA^* denote the area under the reference voltage during this same interval of time. The change in the error signal $e(t)$ over any one half-cycle period is clearly proportional to the combination of these unit areas. The largest differences, i.e. the peaks of $e(t)$, vary even when the ΔA^*'s are constant because of the discrete nature of the AC-PDM controller. The largest of these peaks having the polarity opposite of the reference voltage can only be as large as $K\,\Delta A$ if $\frac{\varepsilon}{K} << 1$ and the controller operates unsaturated. The largest peak with the polarity of the reference voltage can be as much as $K\,(\Delta A + \Delta A^*)$ for two level synthesis of a half-bridge. Thus, the error is bounded as

$$e_A \equiv \left|\frac{e(t)}{K}\right| \le |\Delta A| + |\Delta A^*| \tag{6}$$

If the reference voltage has a peak amplitude of V^*_{LF}, then ΔA^* can be estimated as

$$|\Delta A^*| \le \frac{V^*_{LF}}{2f_{HF}} = \frac{m\,V_{LF\max}}{2f_{HF}} \tag{7}$$

where m is the modulation index defined earlier. Equations (4) and (7) then yield

$$e_{A\,max} \le \frac{(1+m)\,V_{HF}}{2\pi f_{HF}} \tag{8}$$

This inequality shows that for a given value of the link voltage, determined by requirements of the signal amplitudes to be synthesized, the maximum error decreases with an increase in the link frequency. This result confirms what common sense would suggest, i.e. the higher the link frequency the better is the fidelity of the synthesis. Note that Eq. 8 establishes a bound on the error. The actual error during the majority of half- cycles is much smaller than this maximum value. When synthesizing low frequency voltages, $e_{A\,max}$ may be compared to the area under one half-cycle of the reference signal, A^*_{LF}. For sinusoidal reference signals, this ratio is given as

$$\left|\frac{e_{A\,max}}{A^*_{LF}}\right| \le \frac{((1+m)/2\pi f_{HF})\,V_{HF}}{(V^*_{LF}/\pi f_{LF})} \tag{9}$$

Expressing V^*_{LF} in terms of its maximum value and using (4), we have

$$\left|\frac{e_{A\,max}}{A^*_{LF}}\right| \le \frac{\pi}{2}\,\frac{(1+m)}{m}\,\frac{f_{LF}}{f_{HF}} \tag{10}$$

For a frequency differential of 50 (i.e. synthesizing 400 Hz voltages from a 20 kHz link) the ratio in Eq. 10 varies from 0.06 at modulation index of unity to 0.35 for modulation index of one tenth. In an ac link system, the modulation indices can be expected to be high when fixed amplitude voltages are synthesized because the link voltage can be adjusted to suit the individual converter needs. Variable voltage synthesis frequently used in motor control fortunately requires constant Volts/Hertz characteristics. In such converters, the low values of the modulation indices are compensated by correspondingly higher frequency differentials so that low-distortion synthesis can be realized over a wide range of amplitude change.

Experimentation has shown that the controller performance is not very sensitive to the choice of difference integrator gain K. When the gains are very low or if they approach values such that the corresponding cut-off frequency of the equivalent low-pass filter approaches the sampling frequency $2f_{HF}$, then the controller malfunctions. However, within these bounds variations in K show no appreciable affect on the system performance.

If the reference signal v^*_{LF} is dc then it is straightforward to estimate the ripple frequency f_R of the error signal $e(t)$ as a function of the modulation index m. If m is zero then f_R equals f_{HF} as the controller oscillates between its two possible states. When m equals unity, f_R must be zero because the controller is on the threshold of its linear range. Thus, for constant values of modulation index m, $0 \le m \le 1$,

$$f_R = (1-m) f_{HF} \tag{11}$$

The finely discretized nature of the AC-PDM controller causes the actual ripple frequency to vary around this "average" value. The error signal e(t) and the synthesized voltages have the frequency $2f_{HF}$ and its subharmonics present besides the ripple frequency f_R.

Current Synthesis. PDM controller of Fig. 2(a) can be used to synthesize current instead of the voltage at the low frequency end by switching to a current reference signal, $i^*_{LF}(t)$ and feeding back the actual current $i_{LF}(t)$. The current synthesizer still operates by applying half cycle voltage pulses but the logic that selects the polarity of these pulses is now based on the integrated current difference

$$\frac{e(t)}{K'} = \int (\, i^*_{LF}(t) - i_{LF}(t)\,)\, dt \tag{12}$$

The term on the right is now the difference in amp-sec. Note that the controller action is now indirect. Application of a voltage pulse causes a current change that depends upon the low- frequency portion circuit. If the low-frequency circuit is composed of an emf behind a predominantly inductive impedance (i.e. $(L_{LF}\omega_{LF})/R_{LF} >> 1$), then the maximum current change resulting from the application of one pulse from a half bridge circuit is $\Delta I_{LF\,max} = V_{HF\,max}/(L_{LF}\omega_{HF})$. Thus, the unit area difference in current synthesis is of the order of $1/(L_{LF}\omega_{HF})$ of the values obtained for the case of voltage synthesis. If threshold values are assumed unchanged, then the gain K' of the difference integrator of such a current converter must be increased by this order of magnitude.

Area Comparison vs. Delta Modulation. Delta modulation is a technique used in quantization of analog signals that is finding increasing use in the digital transmission of voice [16]. Its application for control of static PWM inverters has been suggested as an easy to implement alternative to the commonly used sine-triangle method [17]. The Area Comparison method and Delta Modulation both use feedback and can be implemented using an integrator and a comparator. However, the two modulation techniques differ in several aspects. The fundamental difference between the methods is that the digital output (i.e. the pulse density) of the Delta Modulation technique is proportional to the *slope* of the reference signal while in the Area Comparison PDM it is proportional to the *amplitude* of the reference signal - a consequence of the fact that the integrator in the AC-PDM operates on the difference or error signal instead of the feedback signal alone. As a result, a PDM converter using area minimization can synthesize a wider variety of signal types including dc. An AC-PDM converter does not show slope overload and is also less sensitive to the variations in the controller parameters and the high-frequency noise that sometimes accompanies the reference signals when these quantities are generated digitally.

Circuits and Circuit Operation of AC-PDM Synthesizers

So far, we have assumed a half-bridge power circuit in our discussion. For the full bridge circuit the operation and the fundamental relationships are similar. However, a full bridge circuit offers more choices in the manner of implementing the AC- PDM technique. This fact is illustrated with the help of the line voltage waveforms of Fig. 3. When the full bridge circuit is operated simply as a combination of two half bridges with equal but phase displaced reference signals the line voltage waveform can be made up of three levels or possible combinations of the high frequency input including zero, see Fig. 3(a). Alternately, the line voltages can be synthesized directly using just two levels. Fig. 3(b) shows synthesis using positive and negative pulses. Fig. 3(c) shows the same synthesis but using zero as one of the levels. The other level used is that which corresponds to the instantaneous polarity of the reference signal. This type of waveform is sometimes called commutated waveform. The waveforms of Fig. 3 differ not only in their harmonic content but also in the waveform of the current they cause the converter to reflect back to the high-frequency side. For a given load current, the commutated waveform causes fewer reversals in the instantaneous power at the link. This can be desirable from the point of view of minimizing the temporary energy storage requirements in the system.

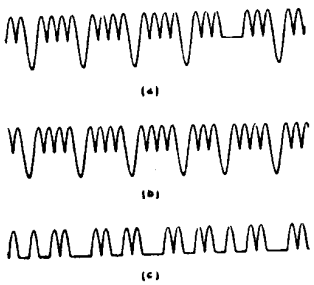


Fig. 3 Line Voltage Waveforms Realizable with a PDM Bridge. (a) All Three Levels Present When Each Pole of the Bridge is Controlled Independently, (b) Direct Synthesis of Line Voltage, (c) Direct Synthesis with Level Opposite to the Reference Signal Polarity Being Excluded - Commutated Waveform.

Power Switches. Direct operation from an ac link requires that the power switches used in PDM converters have bi-directional voltage blocking capability. Bi-directional current capability is also needed unless the low-frequency side current is unidirectional. The other characteristics that are especially desirable in converter power switch are the short switching and recovery times, a high di/dt capability and a low stray inductance. Figure 4 shows some of the possible device arrangements that may be used to realize switches for PDM converters. The first group, represented by Fig. 4(a), uses devices with built-in voltage blocking capability. Promising among this group of devices are the static induction thyristors [18] and fast GTO's [19]. These devices have high current densities and high voltage capabilities at switching speeds of 20 kHz and higher. In the second group, represented by Fig. 4(b) and 4(c), are the devices with no reverse blocking capability. Prominent in this group of devices are power darlingtons, power FET's, static induction transistors. MOS-IGT's or similar conductivity modulated switches being currently marketed belong to this group although devices with reverse blocking capability have been reported [20].

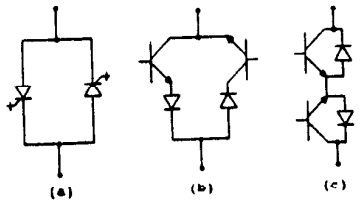


Fig. 4 Realization of Bi-Directional Switches. (a) Using Devices with Reverse Blocking Capability Such as GTO's and SITs, (b),(c) With Devices not Having Reverse Blocking Capability Such as Power Darlingtons, MOS-FETs and IGTs.

Thus far, we have discussed the use of only forced commutated devices although it is entirely possible to use naturally commutated devices such as inverter grade thyristors to realize power switches for PDM converters. Automatic reversal of the ac link voltage makes natural commutation of devices possible. However, the need to establish circulating current of appropriate polarity to achieve turn-off of the conducting device, makes the operation of the converter dependent on the power factor at the low-frequency end. The major difference in operation occurs during intervals when the power flow is in the direction of the high-frequency link. For the duration of this interval, the circulating current of the correct polarity is established only if the incoming switch is fired in advance of the voltage reversal. The angle of advance is determined by the commutation overlap (likely to be small due to the presence of the resonant tank capacitor) and the turn-off time of the device. This advance firing increases distortion, both in the synthesized output and the link voltage, and increases the switching losses in the converter. However, the performance in both aspects is still likely to be far superior to that of a conventional phase angle controlled cycloconverter. When near unity power factor loads need to be supplied from the high-frequency link, use of naturally commutated PDM converter should be considered.

Computer Simulation. Computer models of single- and three phase PDM converters have been developed in order to study their operation in more detail. For modeling purposes, switches are represented by series combinations of a small inductance and a logic controlled ideal switch. The current through the switch is obtained by integrating, for the duration of the switch closing, the voltage across the switch-inductance combination. When the switch is open, the current is zero and the voltage across the device is the voltage across the combination. Passive components and sources are modeled in the usual manner.

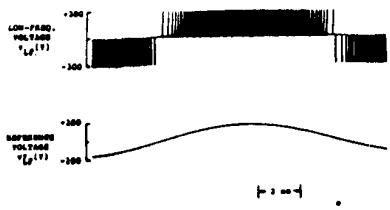


Fig. 5 Synthesis of a 120 V rms, 60 Hz AC Voltage Using a Single-Phase PDM Bridge.

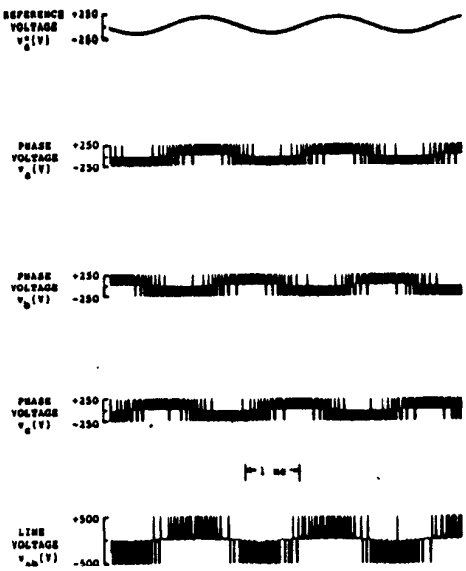


Fig. 6 Synthesis of a Balanced Set of Three-Phase, 400 Hz AC Voltages using a Three-Phase Bridge PDM Converter. Modulation Index is 0.9.

The computer models developed have been used to first study PDM synthesis of a variety of signal types. Waveforms of Figs. 5 to 7 are representative of these results. Figures 5 and 6 show no-load synthesis of ac voltages. In Fig. 5, a 120 V rms, 60 Hz voltage is synthesized from a 300 V peak, 20 kHz link voltage using a full bridge circuit. It can be noted that the synthesized waveform is of the commutated type. Figure 6 shows waveforms resulting when a three-phase bridge is used to synthesize a balanced set of three-phase voltages. Three phase displaced reference signals having a frequency of 400 Hz and a peak amplitude of 163 V (corresponds to 115 Vrms per phase) were used. The link frequency is again 20 kHz and its peak voltage is 500 V. Figure 7 is an example of PDM current synthesis. Again a single-phase bridge is used to command a zero current into a 115 V dc source. A 2 mH inductor has been used to limit the current ripple. During the synthesis the polarity of the dc source is reversed to show how the controller automatically adjusts to changing conditions at the low-frequency end. Note that the response to the step change is accomplished in essentially one- half cycle of the high frequency link voltage.

Loading. Figure 8 shows the circuit operation when the converter draws an average current of 10 A from the 115 V dc source. Observe that the current waveform reflected back to the link is a result of the converter switching action on the low frequency side current. The waveform shown is typical of that seen in zero

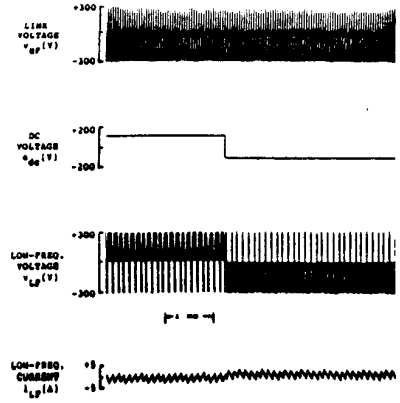


Fig. 7 PDM Synthesis of a Zero Current into a DC EMF. $e_d = 115V$, $L_d = 2mH$ and $V_{HF} = 300V$.

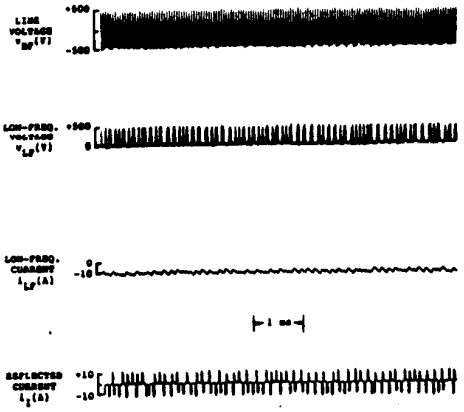


Fig. 8 Operation With Load. Current Synthesis into a DC EMF. Current Reference, $i_d^* = 10A$.

voltage switching PDM converters and illustrates several key characteristics of such converters. First, the current always flows for the entire duration of the link voltage half-cycle during which time it is nearly constant because of the frequency differential. This characteristic is an important feature from the point of view of regulating the link voltage and frequency. The polarity of this current determines whether the power flow for that half cycle is instantaneously positive or negative. Its peak value can be as much as the peak value of the low-frequency end current. It is apparent that the rate of change current can be very high with such a waveform. This suggests the use of capacitor on the link side so that fast changing currents can be supplied independent of the source impedance of the link. Note that the instantaneous power varies depending on the switching action of the converter but the average power is dependent only on the circuit conditions. It is clear that a mechanism for temporary energy storage is needed at the link side of the converter so that the instantaneous power swings can be accommodated and so that the current drawn from the link corresponds to the average power. DC voltage link converters have similar requirements. The role of temporary energy storage there is played by the large electrolytic capacitor connected across the dc link.

The equivalent circuit element of the dc link electrolytic capacitor for a resonant ac link is a parallel connected LC circuit resonant at the frequency of the link. The waveforms of Fig. 8 demonstrate that a synthesizer is capable of handling the fast changing currents which occur for non-unity power factor if such a parallel LC tank circuit is included on the link side. However, with a finite energy storage capacity, the link voltage waveshape and amplitude are adversely affected. If the reflected current has a dominant harmonic, for example the sixth for a three-phase bridge, then the link voltage amplitude can be expected to be modulated at this frequency. This is corresponds exactly to the the sixth harmonic ripple on the electrolytic capacitor of the dc voltage link system.

It is fortunate that variations in the link voltage amplitude do not affect the fundamental component of the low-frequency signal. This feature is due to the feedback mechanism of the AC-PDM controller which automatically compensates for such changes. However, considerations such as the distortion in the synthesized signals (especially in voltage synthesis), device protection and others require that the link voltage variations on a cycle to cycle basis or long term drifts not be allowed to become excessive.

SYSTEM OPERATION

The computer models of the converter which have been established together with other system components are now used to study the operation of the overall system. In order to limit the size of system model and yet provide a good idea of the system operation a reduced system, shown in Fig. 9, has been simulated. The inductance L_l shown represents the combined estimated value of the inductance of the ac link and the leakage inductance of one high frequency transformer. The three-phase PDM converter of Fig. 9 is capable of supplying a passive RL load or operate a three-phase induction machine.

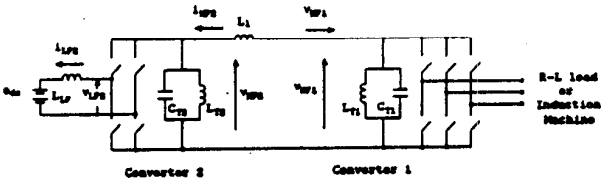


Fig. 9 Reduced System Modeled on the Hybrid Computer.

Starting and Regulation of the Link Voltage Since the operation of PDM converters depends on the availability of a high-frequency voltage at the link, a means of developing and regulating this link voltage is needed for a satisfactory operation of the entire system. One method of achieving this is to have a dedicated exciter in the system to charge up the resonant tanks. The converters are activated once the desired link voltage has been established. The exciter then regulates the link voltage but plays no role in the average power transfer in the system. Because of its role in regulating the link voltage, the exciter must share temporary energy storage with the resonant tank circuits. The sharing determines the nature of its link voltage regulation function. For example, low values of energy circulation allow regulation of only the "average" value of the link voltage magnitude. A more active regulation (on a cycle-by-cycle basis) requires a temporary energy storage capacity in the exciter that is comparable to or larger than that of the resonant circuits. The energy storage in the exciter can be provided by a large electrolytic capacitor if a dc input exciter is used. Electrolytic capacitors are extremely well suited to an energy storage function due to their high energy storage densities, low losses and low cost. Exciter power circuit losses can be minimized by using resonant circuit topologies [7].

The system described in Fig. 9 was first run with a dedicated exciter. For this reduced system, average power flow balance is a rather straight forward consideration. The average power on the link side of converter #1 is monitored and used as an input to a closed loop controller which then determines the value of the current reference signal for converter #2. With this implementation the exciter supplies the tank losses and maintains the link voltage amplitude (averaged over several cycles) near its nominal value. If the current reference of converter #2 is now determined on the basis of both the average power balance and the link amplitude then the link voltage amplitude (averaged value) can be maintained at a desired reference value without the presence of the exciter. A block diagram for the power balance and voltage regulator is shown in Fig. 10. Waveforms of Fig. 11 show the system operation with the converter #2 operated to meet the power demand of the three-phase load and to regulate the link voltage. It can be noted that good regulation of the ac link can be maintained.

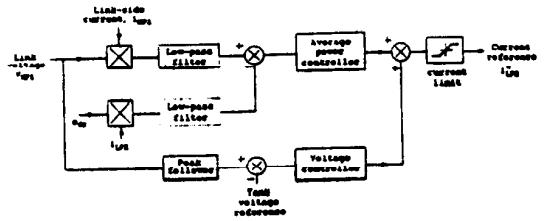


Fig. 10 Block Schematic of the AC Link Controller for the System of Fig. 9.

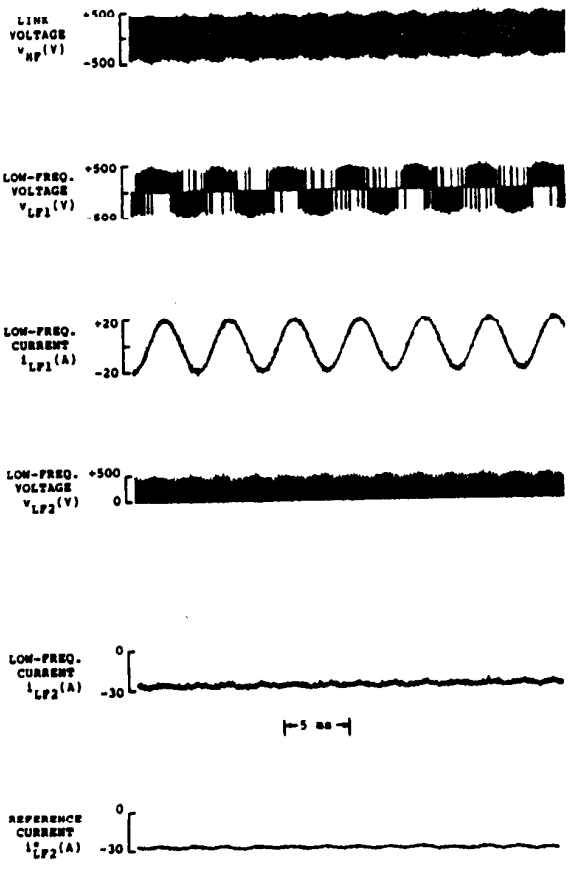


Fig. 11 Waveforms Showing System Operation with Power Flow from the DC Source to a 3-Phase R-L Load.

Although it has been demonstrated that the system can be operated without an exciter, it is not entirely clear whether the system can also be started without a dedicated exciter. The interface converters in the system clearly cannot be operated as PDM converters until the ac link voltage has been established. However, the bi-directional forced commutated switches of the converter power circuit are well suited for operating as a switched current source which is an ideal circuit element for charging the resonant tank circuits. If a converter in the system is already programmed for operation with a dc emf then the start up is straight forward. Should the converter be set up for current synthesis, e.g. converter #2 in the system of Fig. 9, even the control circuit does not have to be modified. The waveforms of Fig. 12 demonstrate the link voltage build-up using converter #2. In particular, a current is built up in the low-frequency side inductor by simply shorting the low frequency end of the converter. As this current approaches a predetermined value the switches begin to operate normally thus causing energy to transfer from the inductor to the link resonant tanks. The transition to PDM converter operation with synthesis of just enough current needed to sustain this voltage is automatic for this type of current controlled converter.

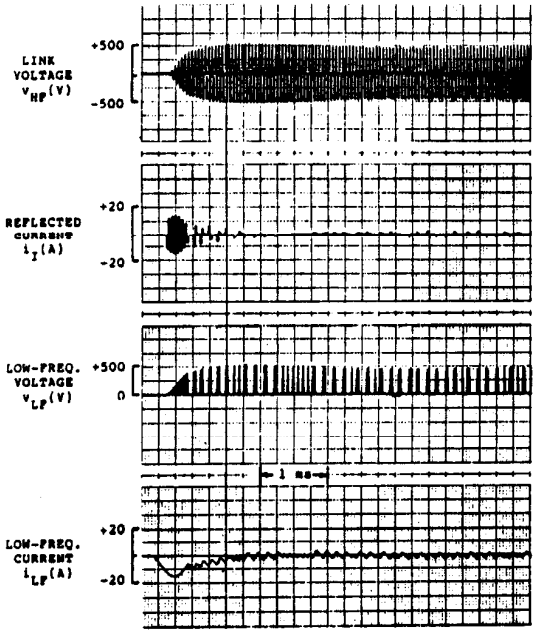


Fig. 12 Startup of LC Tanks Using Synthesizer #2 of Fig. 9.

If none of the converters in the system are connected to, or can be switched to a dc emf, it may still be possible to start up the tanks from a low-frequency ac emf (at least, one source in the system is assumed) because the slow changing emf amplitudes together with the bi-directional devices in the system can be viewed as simply an approximation of a dc emf supply. However, this aspect has not, as yet, been investigated.

Experimental Verification. In order to experimentally demonstrate the operation of PDM converters and to verify the computer models used in the simulation of the system operation a laboratory breadboard has been built. A second objective is to obtain data for a possible future breadboard of a more extensive system. In the laboratory, a three-phase bridge PDM converter and its input resonant LC tank operate from a high-frequency voltage to synthesize balanced low-frequency signals. The tank- converter combination is fed from a high impedance 20 kHz source that starts and maintains the "average" voltage across the tank. A parallel output series resonant converter with a large series inductance provides such a mechanism for regulating the link voltage. Note that the temporary energy storage is almost entirely accomplished by the resonant tank because of the relatively high impedance of the sourcing converter.

Reverse connected power darlington pairs, Fig. 4 (c), was used, primarily for convenience, as the configuration for the bi-directional switches of the PDM converter. For the tank circuit capacitor, polypropylene film capacitors (for example, General Electric 97 series) have been used for their high current capability and very low dissipation factors. The inductor is an experimental air-cored inductor wound with Litz wire. Tank circuit Q of 98 was measured for this experimental design. Q's of the order of two or three times this value are expected when the inductor is wound on cores having low-losses at high- frequencies such as ferrite, amorphous metals (MET GLASS) or half-mil supermalloy tape cores.

Figure 13 shows a typical set of voltage and current waveforms observed on the breadboard across one converter switch. The waveforms demonstrate the zero voltage switching of the PDM converters. Small deviations from the ideal of zero voltage switching can occur due to the variations in the storage times of the power switches. The sharp peaks in switch current waveform are due to the slow recovery of the reverse diodes in this back-to-back connected power darlington configuration of the bi-directional switch. Implementations in the manner of 4(a) or 4(b) should significantly reduce or eliminate these spikes.

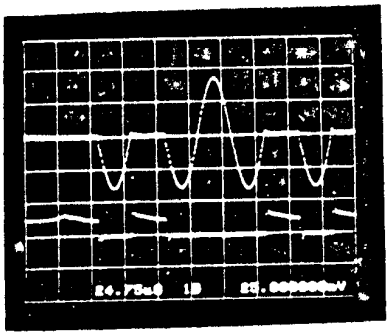
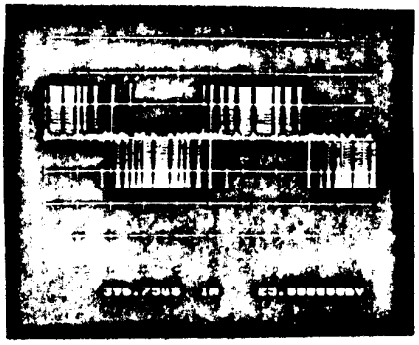
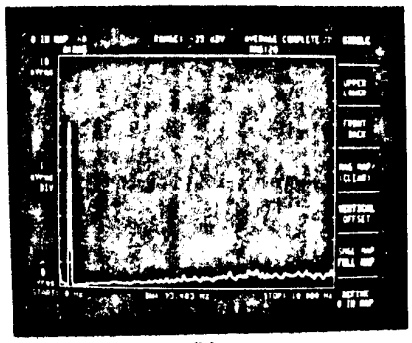


Fig. 13 Typical Voltage and Current Waveforms Observed Across one Converter Switch on the Breadboard System. Upper Trace: Switch Voltage; 125 V/div. Lower Trace: Switch current; 5 A/div.

Figure 14(a) shows a typical line voltage waveforms when low frequency three-phase voltages are synthesized on the breadboard. For this case the reference signal had a frequency of 400 Hz and a modulation index of unity. The corresponding harmonic spectrum is shown in Fig. 14(b). A spectrum of very low harmonic content is apparent. Discrete nature of AC-PDM controller causes slow variations in the waveforms. Therefore, a 20-sample rms averaging was used to obtain this spectrum. Frequency range was limited to 10 kHz to obtain detail in the lower frequency range. In the frequency range above 10 kHz, the prominant feature is the presence of dual peaks located at $2f_{HF} \pm f_{LF}$. For the case of unity modulation index, the peaks have an amplitude of less than one-third relative to the fundamental. For comparison, Fig. 15 shows the line voltage spectrum when the controller is fully saturated and the line voltage is a square wave composed of rectified half-cycles of the link voltage. An increase of $4/\pi$ in the fundamental component and the characteristic fifth, seventh, etc. harmonic components are observed as expected.

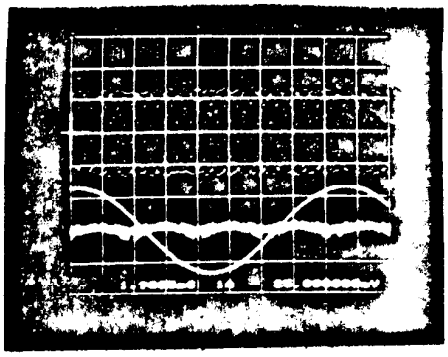


(a)

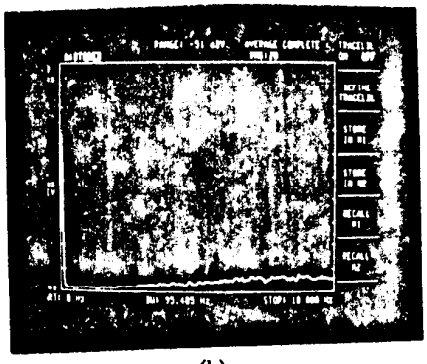


(b)

Fig. 14 Breadboard Converter Synthesizing 3-Phase, 400 Hz AC Voltages. Modulation Index is One. (a) Line Voltage V_{ab}. Scale 125 V/div. (b) Associated Harmonic Spectrum.



(a)



(b)

Fig. 16 Operation with Load. (a) Upper Trace: Link Voltage 125 V/div. Middle Traces: 60 Hz Load Current; 2.5 A/div and Phase "a" Error Voltage on a Time Base of 7.94 ms/div. (b) Harmonic Spectrum of the Line Voltage, v_{ab}.

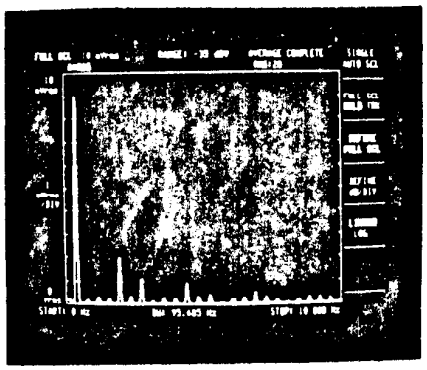


Fig. 15 Line Voltage Spectrum When the Controller is Saturated (Over Modulation) and the Synthesized Voltage is a Square Wave Composed of Rectified Half-Cycles of the Link Voltage.

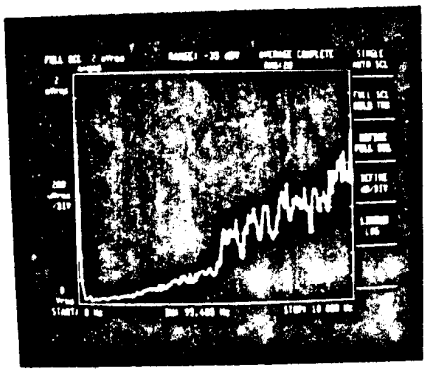


Fig. 17 Harmonic Spectrum of Line Voltage at 60 Hz and a Reduced Modulation Index. The Volts/Hertz is Same as in Fig. 14.

Figure 16 (b) shows line voltage spectrum when the link voltage has an induced ripple (Fig. 16(a)) due to load current. The frequency of synthesis is 60 Hz and the modulation index is one. Note that the harmonic spectrum is relatively unaffected by the link voltage ripple because of the feedback nature of the AC-PDM controller. Finally, Fig. 17 shows the line voltage spectrum for the case of a low value of the modulation index. The frequency is 60 Hz but the modulation index has been reduced so that the frequency to amplitude ratio is the same as in Fig. 14. It is apparent from all of this test data that the AC-PDM converters are capable of very low harmonic distortion when operating from a 20 kHz link frequency.

APPLICATIONS

NASA Lewis Research Center has been studying the feasibility of using high-frequency ac link converters as the auxiliary power system for the next generation of aircraft and space systems requiring multi-kiloWatt power systems [21,22]. A similar high frequency link system has been under study for use in the upcoming space station. Initial power requirements for the space station have been estimated at 75 kW level [23]. The system configuration presented in this paper appears to be a promising alternative for such applications

CONCLUSIONS

This paper has presented a new power converter scheme utilizing a 20 kHz high-frequency link suitable for a distributed power network requiring high efficiency and low weight. Sinusoidal currents as well as dc can be synthesized in single phase or three phase form with very low harmonic content. The proposed configuration permits flexibility in the choice of voltage levels in the system without the penalty of bulky magnetic components, as well a fast system response, high efficiency, freedom from acoustic noise, and provides a high degree of uniformity and ease of implementation since a static power converter of one basic type is used to interface a wide variety of loads/sources in the system.

A zero-voltage switching pulse-density-modulated converter is proposed as the basic interface converter. By restricting all switchings to the zero crossing point of the sinusoidal link voltage the switching losses in the interface converter, which are the dominant component of the converter losses at these high frequencies, are minimized. It has been shown that the technique of pulse-density-modulation together with area comparison control permits the synthesis of fixed or variable amplitude dc and fixed or variable frequency, single- or three-phase ac from the half- cycle pulses of the link voltage. In spite of the restrictions on the switching instants, the distortion in the synthesized signals had been demonstrated to be very low because of the large frequency differential on the two sides of the converter.

ACKNOWLEDGMENT

The work reported in this paper was supported by the NASA Lewis Research Center, Cleveland OH under contract NAG3-361. The authors wish to thank the Center personnel, in particular Mr. Irv Hansen, for their continued help and encouragement.

REFERENCES

[1] N. Mapham, *An SCR inverter with good regulation and sine-wave output*, IEEE Trans. Ind. Gen. Appl., vol. IGA-3, pp. 176-187, Mar./Apr. 1967.

[2] B. R. Pelly, *Latest developments in static high frequency power sources for induction heating*, IEEE Trans. Ind. Electron. Contr. Instrum., vol. IECI-17, pp. 297-312, June 1970.

[3] J. G. Kassakian, A. F. Goldgerg and D. R. Moretti, *A comparative evaluation of series and parallel structures for high frequency transistor inverters*, in Conf. Rec. 1982 Annual Meeting IEEE Power Electronics Specialist's Conf., pp. 20-26.

[4] R. Myers and R. D. Peck, *200-kHz power FET technology in new modular power supplies*, Hewlett-Packard Journal, pp. 3-10, August 1981.

[5] V. T. Ranganathan, P. D. Ziogas and V. R. Stefanovic, *Performance characteristics of high frequency links under forward and regenerative power flow conditions*, Conf. Rec. 1983 IEEE Ind. Appl. Soc. Annual Meeting, pp. 831-837.

[6] F. C. Schwartz, *An improved method of resonant current pulse modulation for power converters*, IEEE Trans. Ind. Electron. Cont. Inst., vol. IECI-23, pp. 133-141, May 1976.

[7] R. L. Steigerwald, *High-frequency resonant transistor dc-dc converters*, IEEE Trans. Ind. Elect., vol. IE-31, pp. 181-191, May 1984.

[8] V. Vorperian and S. Cuk, *Small signal analysis of resonant converters*, in Conf. Rec. 14th Annual IEEE Power Electronics Specialist's Conference, 1983.

[9] H. Huisman and S. W. H. de Haan, *A dc to 3-phase series resonant converter with low harmonic distortion*, IEEE Trans. Ind. Electron., vol. IE-32, pp. 142-149, May 1985.

[10] J. B. Klaasens, *DC to AC series-resonant converter system with high internal frequency generating synthesized waveforms for multikilowatt power levels*, in Conf. Rec. IEEE Power Electronics Specialists Conf., Gaithersburg, MD, June 1984.

[11] V. T. Ranganathan, P. D. Ziogas and V. R. Stefanovic, *A dc-ac power conversion technique using twin resonant high-frequency links*, IEEE Trans. Ind. Appl., vol. IA-19, pp. 393-400, May/June 1983.

[12] F. C. Schwartz, *A double sided cycloconverter*, IEEE Trans. Ind. Electron. Cont. Inst., vol. IECI-28, pp. 282-291, November 1981.

[13] R. L. Steigerwald and R. E. Tompkins, *A comparison of high frequency link schemes for interfacing a dc source to a utility grid*, in Conf. Rec. 1982 Annual Meeting IEEE Ind. Appl. Soc., pp. 759-766.

[14] P. M. Espelage and B. K. Bose, *High-frequency link power conversion*, IEEE Trans. Ind. Appl., vol. IA-13. pp. 387-394, Sept./Oct. 1977.

[15] L. Gyugyi and F. Cibulka, *The high-frequency base converter - A new approach to static high-power conversion*, IEEE Trans. Ind. Appl., vol. IA-15, pp. 420-429, July/Aug. 1979.

[16] H. R. Schindler, *Delta modulation*, IEEE Spectrum, vol. 7, pp. 69-78, Oct. 1970.

[17] P. D. Ziogas, *The delta modulation technique in static PWM inverters*, IEEE Trans. Ind. App., vol IA-17, pp. 199-204, March/April 1981.

[18] J. Nishizawa et al, *Low-loss high-speed switching devices, 2300-V 150-A static induction thyristors*, IEEE Trans. Electron Devices, vol. ED-32, pp.882, 1985.

[19] B. Thomas, D. Silber and H. Berg, *Progress in GTO's for industrial line inverter applications*, in Conf. Rec. 1985 Annual Meeting IEEE Ind. Appl. Soc., pp. 882-888

[20] H. Yilmaz et al,*Comparison of the punch through and non-punch through IGT structures*, Conf. Rec. 1985 Annual Meeting IEEE Ind. Appl. Soc., pp. 905-908

[21] I.G. Hansen and G.R. Sundberg, *Space station 20-kHz power management and distribution system*, 1986 Power Electronics Specialist's Conference, Vancouver, Canada, June 23-27, 1986.

[22] I.G. Hansen, *Description of a 20 kilohertz power distribution system*, 21st Intersociety Energy Conversion Engineering Conference (IECEC), San Diego, CA, August 25-29, 1986.

[23] A. F. Forestieri and C. R. Baraona, *Space station power system*, IEEE Trans. Aero. and Elect. Sys., vol. AES-20, pp. 666-670, Nov. 1984.