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HIGH FREQUENCY SERIES RESONANT DC LINK POWER CONVERSION

Yoshihiro Murai and Thomas A. Lipo
Dept. of Electrical & Computer Engineering
University of Wisconsin-Madison
1415 Johnson Drive
Madison, WI 53706-1691

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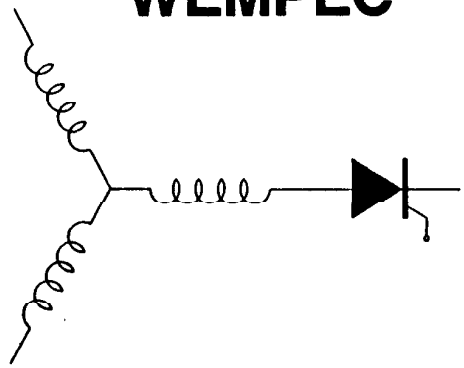

Department of Electrical and Computer Engineering
1415 Johnson Drive
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Y.Murai T.A.Lipo

Department of Electrical & Computer Engineering
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Abstract A new ac/ac conversion scheme is presented which eliminates the need for self commutated devices and requires only 12 thyristors for full double bridge ac to ac power conversion. The system utilizes a series resonant dc link between the ac/dc and dc/ac converters. This series resonant scheme is, in effect, the dual of the parallel dc resonant converter. The dc resonant circuit can be essentially considered as a commutating circuit which ensures turn-off of all 12 thyristors by providing the necessary zero-current instants. A significantly improved sinusoidal current waveform can be obtained at both the input and output compared to conventional high power converters by the use of high frequency pulse density modulation.

INTRODUCTION

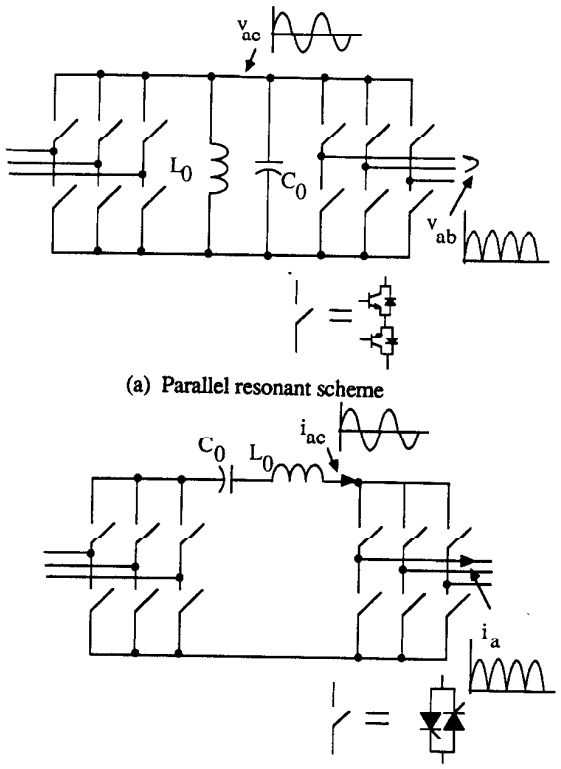
In the past few years remarkable progress has been made in the development of high power density ac/ac converters using resonant-link schemes which utilize high speed devices such as fast recovery transistors and GTOs. These new converters not only have high power density but also possess very low switching losses since switching of the devices are made at zero-voltage instants and thus enable the total system to operate at very high frequency compared to conventional dc link transistorized converters. Although these resonant-link converters are intended to operate at high power density, almost all the systems presented in the past require self commutated transistors and have some difficulty performing conversion at very high power levels because of the relatively low voltage and current margins that self commutated devices such as transistors typically have.

In general, switching schemes for resonant converters can be classified according to their resonant ac-link and resonant dc-link modes. Figures 1 and 2 offer a schematic illustrations of the resonant link circuits presently available [1]-[5]. The resonant ac circuits utilize a parallel resonant circuit as shown in the Fig. 1(a), or a series resonant circuit as in Fig. 1(b). The ac resonant circuit impresses both polarities of ac voltage and current on the link so that the switches of the input and output side converters are required to carry both positive and negative currents as well as block both polarities of voltage. The converter switches should therefore be bidirectional switches which are usually realized by two inverse-parallel transistors or thyristors for the parallel and series resonant circuits respectively, as shown in Fig. 1.

The dc-link circuits of Fig. 2 realize pulsating dc currents in the link by adding dc offsets to the ac resonant currents. All of the resonant dc-link converters reported in the past have been restricted to parallel resonant types [4]-[5]. As shown in Fig. 2(a), half of the transistor switches of Fig. 1(a) are replaced by diodes and the system has a very simple configuration much like the conventional dc link voltage source bridged converters. However, the converters still require transistors which have the self commutating ability necessary to maintain the resonance.

The series resonant dc-link scheme, corresponding to the dual of the parallel resonant dc-link does not yet appear to have been reported in the literature. This paper develops a new series resonant dc-link scheme utilizing a simple configuration which has only unidirectional switches as shown in Fig. 2(b). In this case, switching of the converters occurs only at the zero crossing instants of the link current. Since the current drops below the holding current, the natural turn off ability of a conventional SCR is utilized for commutation. Thus high power thyristors can thus be utilized with minimal switching loss. Since the link current is unidirectional, only the usual six thyristors are needed per converter bridge.

In this paper the series resonant dc-link circuit will be demonstrated to have a natural commutation capability and interruptible switching by first using a simple single phase equivalent



(a) Parallel resonant scheme

(b) Series resonant scheme

Fig. 1 Resonant ac link power converters.

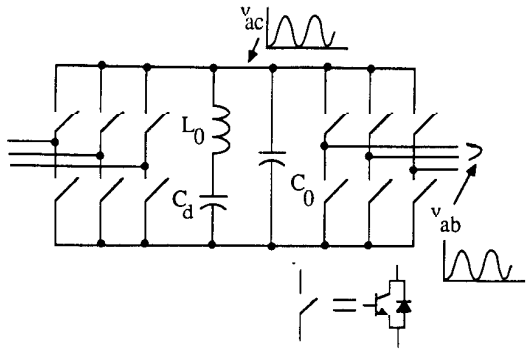
circuit. The three phase configuration and various control schemes will then be reviewed. Performance of the converter will be investigated by digital simulation. It will be shown that by using pulse density modulation this circuit will enable the realization of low distortion sinusoidal current as well as unity power factor on both the ac/dc and dc/ac side converters.

Finally; in this paper, the possible oscillation in the output which seems to be a common problem to current source inverter fed inductive load is dealt with. The use of derivative feedback and damping circuits are discussed for purposes of stabilization.

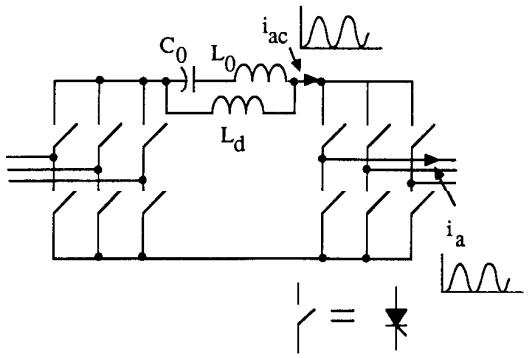
PRINCIPLE OF OPERATION OF PROPOSED CIRCUIT

A more complete depiction of the series resonant dc link converter is shown in Fig. 3. The inductor L_0 and capacitance C_0 are the resonant elements selected to resonate at a frequency consistent with the turn off capability of the converter, typically 10-20 kHz and are relatively small. The thyristor T_{crc} is a protection device, not normally active, used to circulate the current in the resonant circuit and ensure turn-off when the link is not requested to supply current to the load. The inductor L_d is a larger inductor which is controlled to support the dc bias current.

Figure 4 shows the principle of operation of the basic series resonant dc link circuit. The currents in Fig. 4.(a) are obtained from the following equations.



(a) Parallel resonant scheme



(b) Series resonant scheme

Fig. 2 Resonant dc link power converters.

$$E = \frac{1}{C_0}\int_0^t i_0\,dt + L_0\frac{di_0}{dt} + V_L \tag{1}$$

$$E = L_d\frac{di_d}{dt} + V_L \tag{2}$$

$$V_L = \frac{1}{C}\int_0^t i_s\,dt \tag{3}$$

$$i_s = i_0 + i_d \tag{4}$$

Assume the thyristor T_h shown in Fig. 4 is switched to the conducting state at t = 0. If L_d and C_L are sufficiently large to maintain the current i_d and voltage V_L constant, then the current i_s is easily solved by defining the initial conditions,

$$i_d = I_d,\quad i_0 = -I_d$$

$$(i_s = 0, \text{ at } t=0)$$

$$v_c = V_{c0} \tag{5}$$

where I_d and V_{c0} are constants. The solution to these differential equations is

$$i_0 = \sqrt{\frac{C_0}{L_0}}\,E' \sin \omega t - I_d \cos \omega t \tag{6}$$

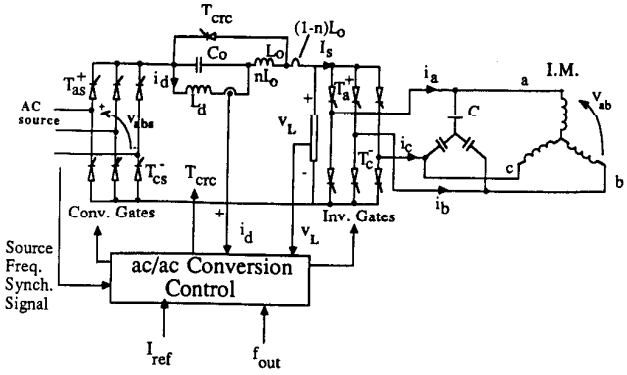


Fig. 3 Detailed circuit proposed for implementing the series resonant dc link scheme.

$$\omega = \sqrt{\frac{1}{L_0C_0}}$$

and

$$i_s = i_0 + i_d$$

$$= \sqrt{\frac{C_0}{L_0}}\,E' \sin \omega t + I_d(1 - \cos \omega t) \tag{7}$$

where $E' = E - v_L - v_{C0}$ (>0).

Letting,

$$i_x = I_d\,(1 - \cos \omega t),\quad i_y = \sqrt{\frac{C_0}{L_0}}\,E' \sin \omega t \tag{8}$$

the current in the link can then be written as,

$$i_S = i_X + i_Y.$$

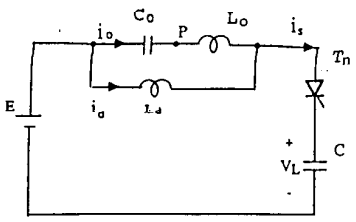
Typical waveforms for the currents i_x, i_y and i_s are shown in Fig. 4(b). As long as the voltage E' remains positive, the link current reaches zero and thyristor T_h is able to commutate at t = t_1. Unfortunately, however, in actual circuit with finite L_d and C_L, the current i_d continues to increase if E' is positive and this fact makes the commutation of thyristor T_h very difficult as shown in Fig. 4(c).

Figure 4(d) shows an improved connection in which L_d is connected in parallel with capacitance C_0. As the voltage across L_d changes according to the capacitor voltage V_0, commutation of the thyristor becomes possible because the resonant current has an oscillation which is not growing, as shown in Fig. 4(e).

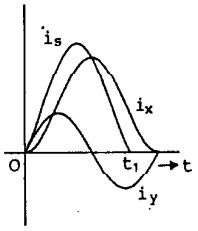
In order to prevent overcharging of the resonant capacitor during the zero current intervals, a circulating thyristor T_{crc} has been utilized as shown in Fig. 5. This thyristor is triggered to circulate the current i_0 whenever i_s becomes zero. (This zero current condition is also required to regulate the output current of the inverter for pulse density modulation and will be described later).

Figures 5(b) and 5(c) show the current i_s and V_L both with and without use of the circulating current thyristor T_{crc}. When a signal to stop firing T_h. occurs, a dead zone appears as shown in Fig. 5(b). As a result, the average output voltage does not change and a large pulse of current appears when conduction of T_h commences. Alternatively, for the case with thyristor T_{crc}, the current i_s is readily interrupted while triggering signal is set to zero and a current i_{crc} flows during this period as shown in Fig. 5(c).

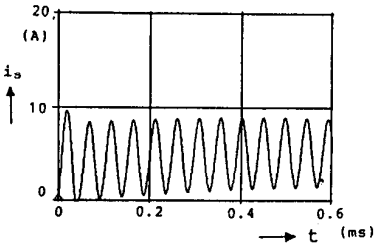
In practice, the circulating thyristor is fired not only when stop signal for i_s appears, but also functions as a clipper for i_s and V_L in which case the resonance of the L-C tank becomes quite stable. The tap ratio n (n< 1) of the inductance L_0 affects the sensitivity of the clipping ability of T_{crc}. If n is set to a large value, the overshoot



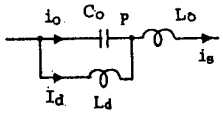
(a) Series resonant circuit with parallel inductance L_d



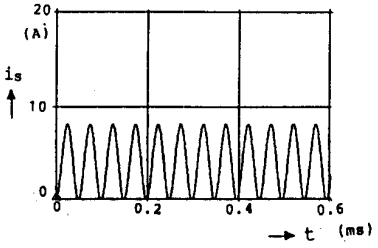
(b) Currents corresponding to the circuit of (a)



(c) Actual current i_S for the circuit of (a)

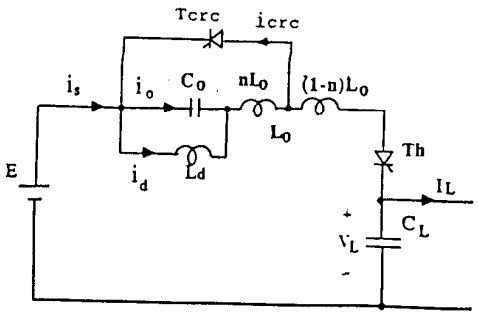


(d) Modification of the connection point of L_d

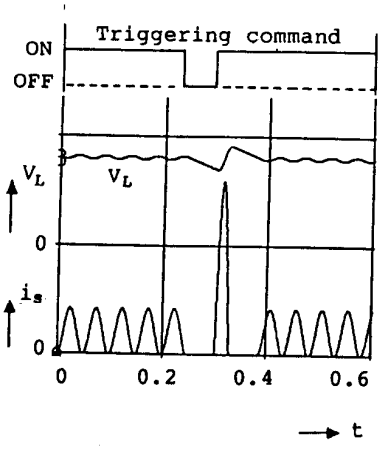


(e) Actual current i_S for circuit of (d)

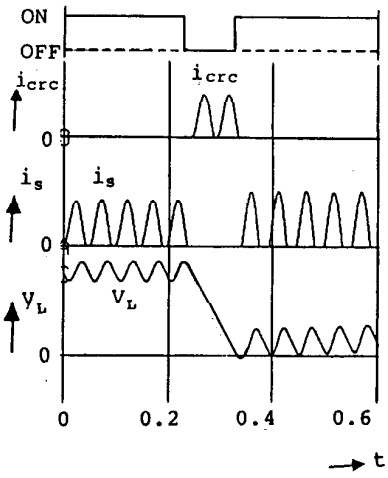
Fig. 4 Princple of operation of the series resonant circuit.



(a) Series Resonant Circuit with Circulating Current Thyristor



(b) Circuit Behavior without T_{crc}

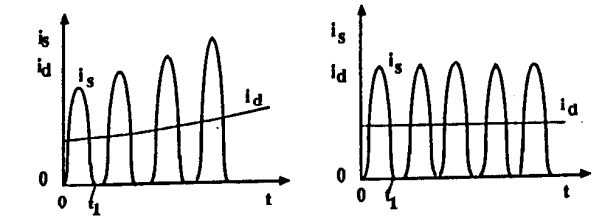


(c) Circuit Behavior with T_{crc}

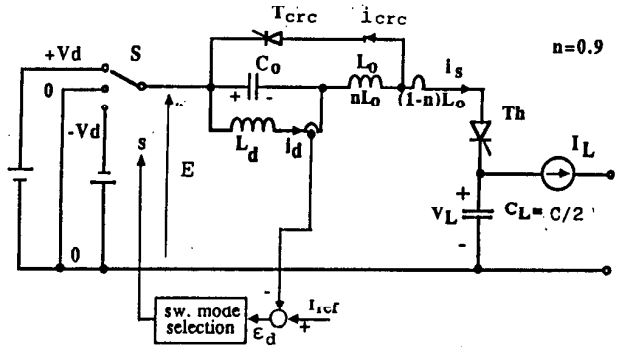
Fig. 5 Illlustrating Purpose of Circulating Current Thyristor.

of current i_s and the voltage V_L increase and the resonance tends to become unstable. On the other hand, when n is chosen very small *(nearly 0), the current i_s goes to zero rapidly whenever the voltage* V_L becomes equal to E and the necessary zero current condition cannot be attained. In this paper. a tap ratio of n = 0.1 is utilized.

In order to maintain control of the amplitude of the pulses as illustrated in Fig. 4(e), regulation of the dc link current is required. Figures 6(a) and 6(b) illustrate how the link current varies with and without regulation. In general, the average value of the current pulse is approximately proportional to i_d. When E' is large, i_s increases and i_d also increases as shown in Fig. 6(b). After i_s reaches zero at t = t_1, T_h turns off and current i_d charges up C_o generally to a larger value than which existed on the capacitor before the previous pulse. After each subsequent turn-on of the thyristor T_h, the currents i_d and i_s pulses continue increase as shown. Hence, current regulation for this type of converter is a mandatory condition.



(a) Non-Controlled i_d (b) Controlled i_d

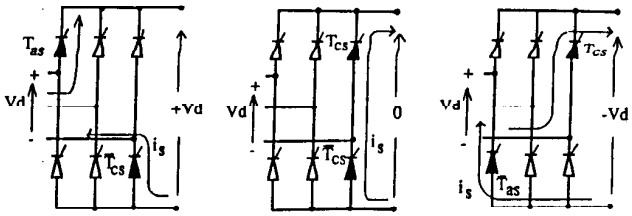


(c) Current control scheme

Fig. 6 Current control of dc inductance.

Regulation of the dc inductor current i_d is accomplished very easily by current feedback as shown in Fig. 6(c). After comparing i_d with the current reference I_{dref}, the source voltage E is adjusted to make the error small. For example the error $\varepsilon_d = I_{dref} - I_d$ is positive, E is changed from V_d to 0 or $-V_d$; if ε_d is negative it goes vice versa. As the controlling ability to i_d also depends on E' (= E-V_L). the measured value of V_L is used for this purpose. While the thyristor T_h is off, L_d charges up C_0 to a negative polarity to prepare for conduction of T_h. The current i_s carries the energy from the resonant circuit to the load or ac source depending upon the polarity of V_L and E. When E is negative, energy flows back to source and when V_L is positive, the energy also flows to load.

Thusfar, it has been assumed that the source voltages are essentially constant. Since the source voltages are, in fact, alternating, the identity of the most positive and most negative phase must be established before switching of the source side bridge can commence. The selection of the source voltages are easily accomplished as shown in Fig.7. When positive, a large positive voltage E' is needed to cause the current i_d to increase. The thyristors are triggered as shown in heavy lines in Fig.7(a) and supply positive voltage V_d to the resonant current. Figure 7(b) shows the zero voltage mode and Fig.7(c) the negative voltage mode.



(a) Motoring mode (b) Circulating mode (c) Regenerating mode

Fig. 7 Illustrating ac/dc conversion modes.

These modes are used to decrease the current i_d. As i_s is always positive, mode (c) regenerates energy back to the ac source.

THREE PHASE CONFIGURATION

In the three phase configuration, the pulses generated in the resonant circuit msut be distributed to each phase. The thyristors in Fig. 3 function as a distributor to switch or redirect the link current at the instants where the current $i_s = 0$. Since the circuit is resonant this instant occurs when nearly zero voltage exists across the thyristor so that the losses in the thyristors are relatively small. Figure 8 shows an example of the pulse density distribution for each phase in the output of the dc/ac side converter.

The distribution of the pulses to each phase is illustrated in Fig. 8 and are automatically determined by comparing the current pulses with the instantaneous phase currents. Figure 9 shows the current references i_{1r} and i_{2r}, the corresponding phase currents i_{sa}, i_{sb}, and i_{sc} and the conducting thyristors in the converter. For example, the current references i_{1r} and i_{2r} correspond to i_{sa} and i_{sb} within the first 60 degrees at which point thyristors T_a, T_b, $\bar{T}_c$ are triggered. In the next 60 degrees these currents correspond to $-i_{sc}$ and $-i_{sa}$, and thyristors $\bar{T}_c$, $\bar{T}_a$, T_b are triggered and so on. Accordingly, the same reference table is repetitively used and makes the ROM table very small. The currents i_1 and i_2 are detected from a current sensor with sampling switch S as shown in Fig. 9(b) which is operated synchronized to the triggering signal of the dc/ac converter thyristor firing instants.

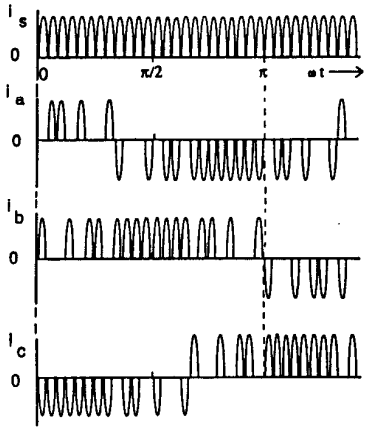
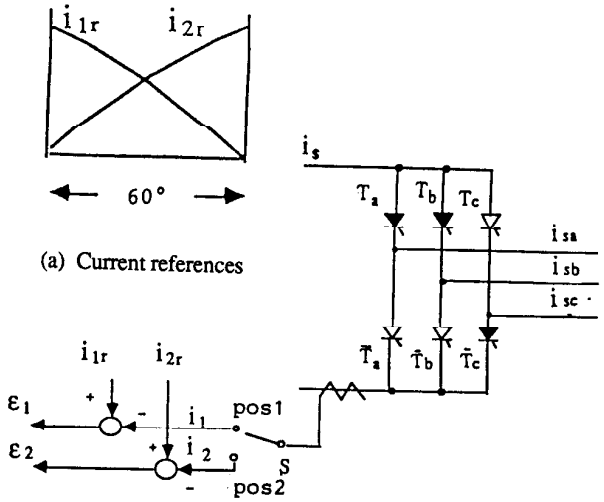
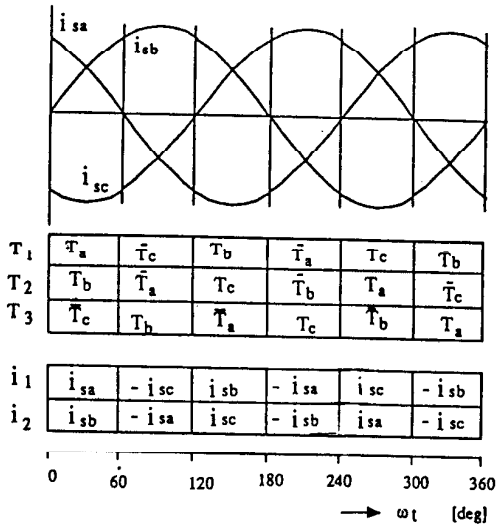


Fig. 8 Illustrating distribution of current pulses to a three phase load.



(a) Current references

(b) Current feedback selection circuit



(c) Current and thyristor selection table.

Fig. 9 Current references and the corresponding current and thyristor selection for each 60° interval.

TRIGGERING SCHEME

The dc/ac converter thyristors are triggered to reduce the maximum error of the three phase currents. Errors ε_a, ε_b, ε_c are obtained from ε_1, ε_2 depending upon the chart in Fig. 9(c). Figure 10 shows the possible combinations of the ε_a, ε_b, ε_c for i_{sa}, i_{sb}, i_{sc}, respectively.

As the sum of the errors must satisfy the relation

$$\varepsilon_a + \varepsilon_b + \varepsilon_c = 0 \qquad (9)$$

all the three errors clearly can not have the same polarity. As the output circuit does not have any neutral line, the current pulse should flow into the positive error phase and flow out from the negative error phase. Hence, the triggering principle is

(i) The thyristor in the phase having the larger error out of the two phases of the same polarity is chosen to be triggered.

(ii) The phase corresponding to the error with the opposite polarity error is selected as the other triggering phase.

For example, in Fig. 10, if ε_a and ε_b are positive then ε_c must be negative. This condition can be termed as mode 1. *If ε_a is* larger than ε_b, the triggering thyristor is selected to be T_a, and the other thyristor becomes T_{c-}. Figure 11 shows the schematic diagram of the overall control system. The mode matrix and comparison gate of currents are included in the block "switching matrix". The ac/dc thyristors are triggered by applying the chart shown in Fig. 9(c). The thyristors shown on the chart are triggered when positive V_d is required on the dc side and these patterns are synchronized to the ac input voltage by the timing pulse f_{in}.

When a negative voltage E =-V_d is required, the triggering thyristors in the chart are replaced from top to bottom or bottom to top of the bridge. As explained previously, thyristor T_{crc} is not triggered while E' = E - V_L is less than V_d (>0). Current i_d is regulated to a value three times that of I_{dref} (k_d =3) in order to ensure sufficient gain to control the load current.

MODE

	I	II	III	IV	V	VI
ε_a	+	+	+	—	—	—
ε_b	—	—	+	—	+	+
ε_c	—	+	—	+	—	+

Fig. 10 Polarity of current error for each of the operating modes.

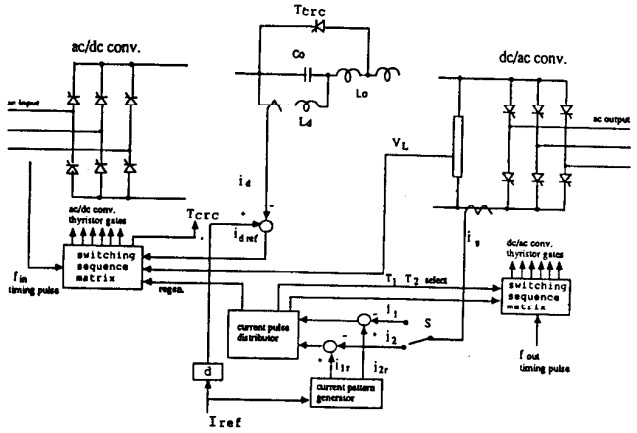
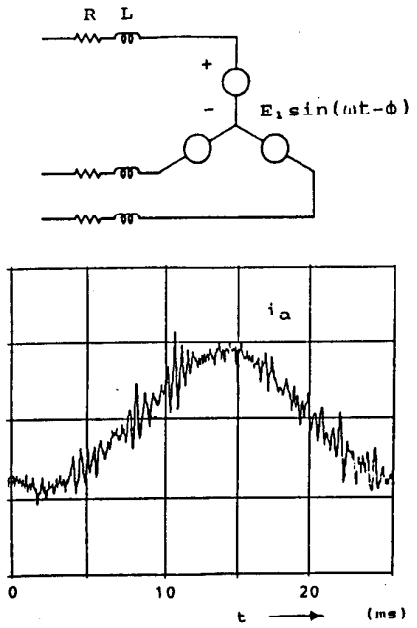


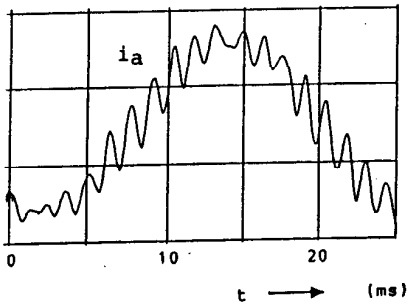
Fig. 11 Control diagram for the overall system.

RESULTING WAVEFORMS

Figure 12 shows the resulting current waveforms obtained by computer simulation. A three phase R-L load with back emf has been utilized. Figure 12(a) was obtained for the case R=5 Ω, L =1.0 mH, E=100v, ϕ = -10 deg, L_d = 5 mH, L_o = 79 μH, C_o = 0.79 μF, $\omega_o = 2\pi$ x 20,000 rad/sec. In addition the actual simulation includes a resistance r_o = 0.05 Ω as part of the inductor L_0. to express the lossy component in the resonant circuit. The waveform appears to be very satisfactory. However, when the resistance R and L are replaced by an induction motor load (200 v, 1.5 kw), i.e. R = 1.0 Ω and L =2 mH, a high frequency oscillation appears as shown in Fig. 14(b). This oscillation is clearly caused by interaction of the filter capacitance C and motor load inductance L. Since the loop of the oscillation involves two Cs and two Ls in series, the resonant frequency f_r is



(a) Circuit load model and current waveform for the case R=5.0Ω, E_1 = 100 V, ϕ = 10°



(b) Current waveform utilizing an induction motor model, R_1 = 1.0Ω, L_1+L_2=4.0 mH.

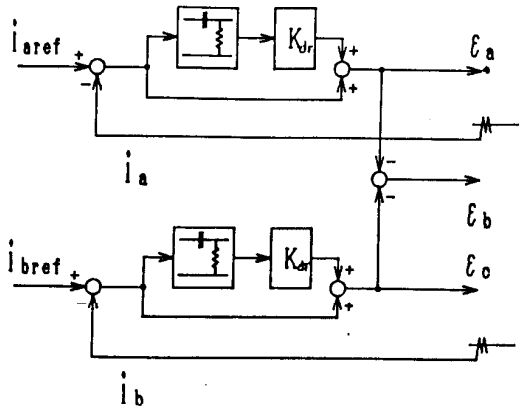
Fig. 12 Output line currents obtained by digital simulation.

$$f_r = \frac{1}{2\pi\sqrt{(2L)(C/2)}} = \frac{1}{2\pi\sqrt{LC}} \qquad (10)$$

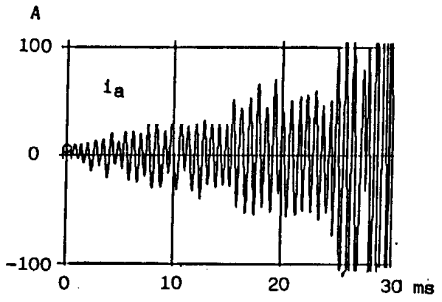
For this case f_r= 1250 Hz. This phenomena appears to be a generic problem for any current source inverter having output capacitance and is not peculiar to this circuit alone.

STABILIZATION

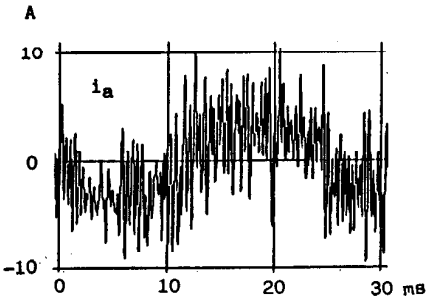
The stabilization of the system is difficult by controlling the current i_s only . Even if the system is accurately controlled, the oscillation remains between the capacitor C and load inductance L almost independent of the current from the inverter i_s. Stabilization was, however, accomplished by controlling the motor currents i_a, i_b, i_c instead of the output currents i_{sa}, i_{sb}, i_{sc}. Figure 13 shows the current feed back loop with a derivative element. Two loops are needed to obtain i_a, i_b, and i_c. In this case, ac link frequency corresponding to L_0 and C_0 is almost completely filtered by the load capacitances C. Hence, feedback was easily done without any further filtering. The derivative circuit was implemented by a simple R - C circuit as shown in Fig.13(a). The time constant was selected as 50 μs and the gain was 2.0. The resulting waveform is shown in the Fig. 13(c) and can be compared to the case without derivative feedback, i.e., K_{drv} =0 in Fig. 13(b). The system is completely unstable as shown in Fig. 13(b) but the system is stabilized by using derivative feedback although it still has an oscillation as shown in Fig. 13(c). The remaining high frequency oscillation over 2 kHz does not have the frequency of Eq. 10 and seems not to be caused by system instability but is ripple caused by the discrete current pulses.



(a) Current feedback loop



(b) Without derivative feedback



(c) With derivative feedback

Fig. 13 Simulated results employing output current feedback.

DAMPING CIRCUIT

In order to further reduce or absorb the high frequency component caused by the current pulses, the damper circuit shown in Fig. 14(a) has been found to be effective. The damping circuit utilizes a resistance R_{dmp} and capacitance C_{dmp}. If the voltage of ripple component is assumed to be E_{rpl} in the expression of the rms phasor, the current through R_{dmp} is obtained from

$$I_{dmp} = \frac{E_{rpl}}{\sqrt{R_{dmp}^2 + \frac{1}{\omega_{rpl}^2 C_{dmp}^2}}} \quad (10)$$

and the dissipated energy P_{dss} in R_{dmp} will be

$$P_{dss} = I_{dmp}^2 R_{dmp} \text{ (for single phase model)}$$

$$= E_{rpl}^2 C_{dmp} \Big/ \left[\left(\sqrt{R_{dmp}} - \frac{1}{\sqrt{R_{dmp} C_{dmp} \omega_{rpl}}} \right)^2 + \frac{2}{\omega_{rpl} C_{dmp}} \right] \quad (11)$$

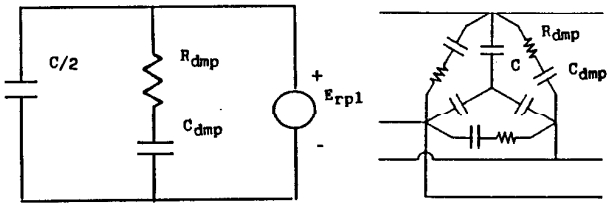
Hence, the resistance R_{dmp} is selected as

$$R_{dmp} = \frac{1}{\omega_{rpl} C_{dmp}} \quad (12)$$

and the maximum dissipation P_{dmax} can be calculated in the form

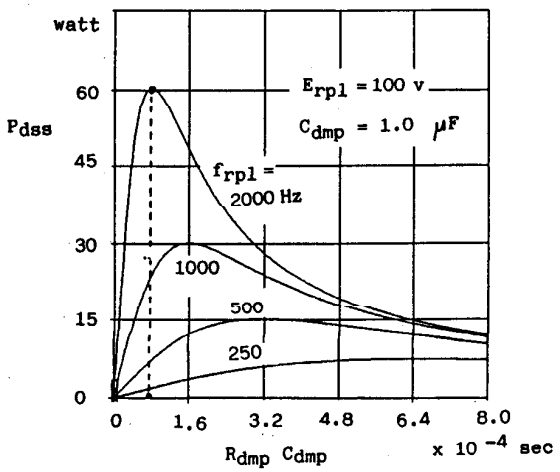
$$P_{dmax} = E_{dmp}^2 C_{dmp} \omega_{rpl} \quad (13)$$

When Eq.12 is satisfied, the dissipation in the output at fundamental frequency becomes extremely small. Figure 14(b) shows the dissipation P_{dss} as a function of the time constant $\tau_{dmp}=R_{dmp} C_{dmp}$ and ripple frequency f_{rpl} when the capacitance C_{dmp} is assumed constant. For example, if the ripple frequency and capacitance C_{dmp} are assumed to be 2000 Hz and 1.0 μF, respectively. Then R_{dmp} becomes 80 Ω from Eq. (9) and the time constant $\tau_{dmp}=R_{dmp} C_{dmp}$=80 microseconds.



Single phase model Actual circuit

(a) R-C damping circuit



(b) Dissipated energy in damping resistor R_{dmp}

Fig. 14 Damping circuit for attenuating load current oscillation.

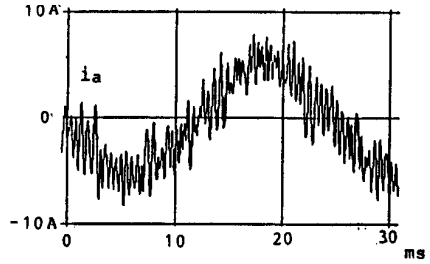
If the fundamental frequency is 50 Hz, then, from the characteristic for τ_{dmp}=80 μs in Fig.16(b), the dissipated energy both in ripple frequency and in fundamental frequency are

P_{dss} =60 watts (2000 Hz)

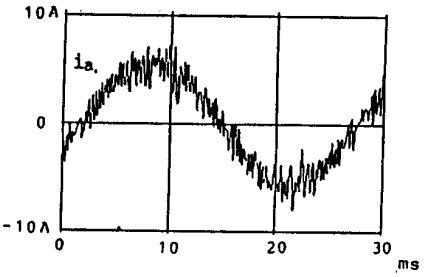
=0.56 watts (50 Hz) (14)

Hence, the fundamental component is negligible and dominant dissipating energy is the ripple component. and very strong selective frequency damping will be performed.

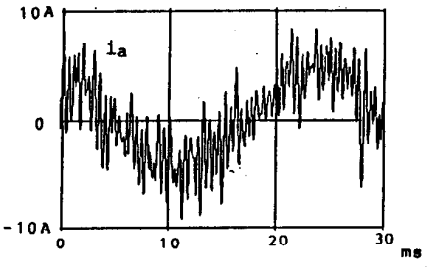
Figures 15(a) and (b) are the results of using damping circuit for the cases in Figs. 13(b) and (c), respectively. Remarkable improvement is apparent in both cases. In the case of non derivative feedback (Fig. 15(b)), the system was stabilized and a much smaller ripple in the current was obtained. As shown in the figure, the damping capacitance is almost comparable to the output capacitance, so that the capacitance C's are increased in Fig. 16(c) while the other parameters are the same as in Fig.15(b). Though a better result was obtained in Fig. 15(c), this waveform still contains a larger ripple than in Fig. 15(b).



(a) With damping circuit only



(b) With both derivative feedback and damping circuit



(c) Without both damping circuit and derivative feedback

Fig. 15 Output current waveforms illustrating the effects of damping circuit.

Accordingly, it can be said that damping capacitance is much more effective to reduce the high frequency current ripple than increase the output capacitance C's. However, the high frequency loss in the damper may increase for machines with very low losses and an upper limit exists from the point of view of total efficiency.

CONCLUSION

In this paper a new high frequency series resonant dc-link ac/ac conversion scheme was described. This new resonant scheme was accomplished by introducing a dc inductance in parallel with a series resonant circuit thus enabling the system to operate with only unidirectional current conducting, bidirectional voltage blocking switches, i.e., thyristors. In addition, the number of the switching devices has been reduced to half the number required in the conventional ac resonant current link. Accordingly, very high levels of power conversion can be realized since the thyristor retains very high margins of voltage and current compared to the transistors utilized in conventional high frequency resonant ac/dc voltage link converters. As this scheme utilizes current pulse density modulation, the output current waveform is significantly improved. Since the input side ac/dc converter also utilizes the same modulation algorithm, the input current waveform becomes sinusoidal and operation at unity power factor is available.

Also in this paper, a circuit with a circulating thyristor was proposed to ensure natural commutation of the converter thyristors. The thyristor serves to circulate a current equal to three times of the load current so that very high response will be obtained even if the loading condition is suddenly changed.

Finally, the paper has also been concerned with the ocillations and instability arising from the output capacitance and inductive load when supplied from a current source inverter. Derivative feedback and damping circuits were utilized and were shown to be an effective means for reducing these undesirable components.

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