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CURRENT PULSE CONTROL OF HIGH FREQUENCY SERIES RESONANT DC LINK POWER CONVERTER

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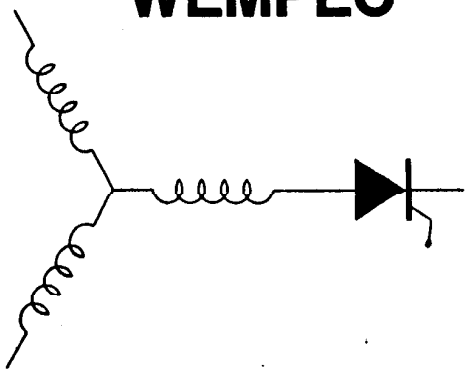

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Current Pulse Control of High Frequency Series Resonant DC Link Power Converter

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Abstract

High power density ac/ac converters utilizing resonant -link schemes which use high speed devices such as fast recovery transistors and FETs have been developed enormously recently. These converters have not only high power density but also possess very low switching losses since the switching of the devices is made at zero-voltage or zero-current instants. The high frequency series resonant dc link ac to ac power converter is the dual of the parallel resonant dc link type and switchings are made at zero-current instants. Further, it utilizes only 12 thyristors for full double bridge. Thus the switching losses can be minimal. Minimum devices and high current and voltage margins because of thyristors utilization is one of the important features of this scheme. However, the dc link converter involves problems such as current pulse fluctuation and system instability because the current pulse is difficult to control sufficiently. This paper develops the control technique of individual current pulses utilizing an auxiliary circulating thyristor. As the current pulses can be adjusted continuously from almost zero to full size, the output voltage waveform can be improved and the instability is removed because of the exact current control. In this paper, performance of the system including such variables as voltage and current for different operating frequencies are presented by digital simulation.

Introduction

High power density ac/ac converters utilizing resonant-link schemes which use high speed devices such as fast recovery transistors and FETs recently expanded enormously. Those converters have not only high power density but also very low switching losses since the switching of the devices is made at instants of zero-voltage or zero-current.

The resonant ac circuits utilize parallel resonant or series resonant circuits as previously presented [1] - [5]. The ac resonant circuit impresses both polarities of ac voltages and current on the link so the switches should be bidirectional.

The dc-link circuits realize pulsating dc current in the link by adding dc offsets to the ac resonant current. We also proposed a new high frequency series resonant dc-link ac to ac power converter at IAS annual meeting, 1988 [6]. This converter is the dual of the parallel resonant dc-link type [4] and utilizes only 12 thyristors for a full double bridge as shown in Fig. 1-a. The capacitor C_0 in series with the inductor L_0 resonates, causing a high frequency pulse current flow from ac source to load; the inductance L_d adds dc offset to this current. Four thyristors conducting in series in two bridges turn on and off at zero-current instants and thus the switching losses are greatly reduced. Minimum rated devices, high current and high voltage margins because of the utilization of thyristors are important features of this converter. However, the prototype converter, involves problems such as current pulse fluctuation and system instability because the individual current pulse was not controlled sufficiently and the load current was adjusted only by PDM (Pulse Density Modulation). Different control strategies were investigated and oscillations were present in the output, which seems to be a common problem to current source inverter fed inductive load. The use of derivative feedback of the output load current and damping circuits (R and C in series) appears to stabilize the system and sinusoidal current and voltage were obtained at the induction machine. The proposed stabilization and control method has the disadvantage of increasing losses in the system and load dependence for the feedback loop, mainly for very low and high load torques.

A circuit with a circulating thyristor was already proposed in Ref.6. This thyristor - T_{CRC} in Fig. 1 - prevents overcharge of the resonance capacitor C_0 during the zero current intervals. T_{CRC} is triggered to circulate the current i_0 whenever i_s becomes zero. The utilization of this thyristor allows a better control of the output voltage and current when changes in current reference or loading conditions occur.

Different approaches have been presented for the realization of soft switching techniques. In particular, concepts for quasi-resonant switches for dc/dc converters utilized zero current switchings have appeared[7]. Diode recovery problems soon required the use of a zero voltage switching strategy [8]. The pseudo- resonant full bridge dc/dc converter[9] represents an alternative to the quasi-resonant switches for higher power levels.

This paper develops a control technique for the individual link current pulses utilizing the auxiliary thyristor T_{CRC} shown in Fig.1, in different improved topologies where better waveforms are obtained and solve the instability problem with no load dependence at all. The series resonant circuit single phase model is utilized to study the circulating current dependence of the output voltage of the input converter, load voltage and current for different reverse recovery time. A complete method is developed to control the

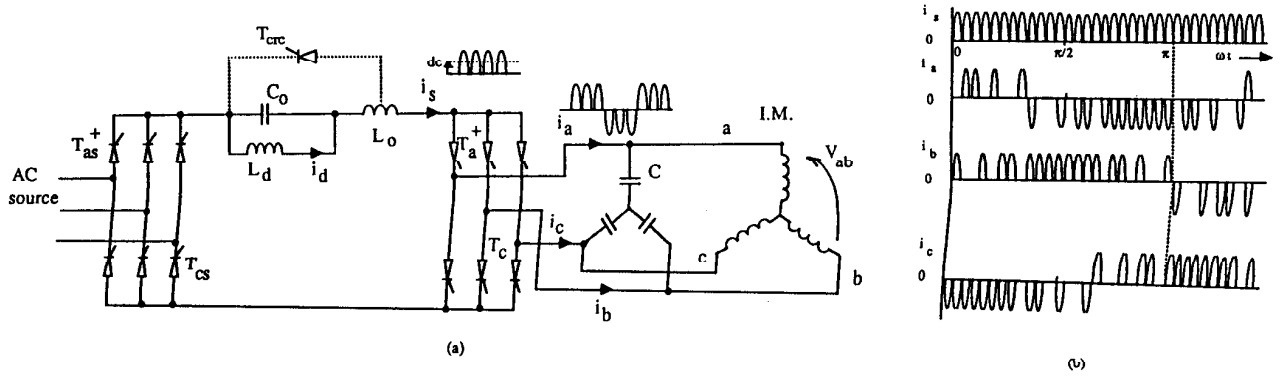

Fig. 1. Series resonant dc link ac to ac converter

individual current pulses i_s which is applied to the three phase model, for different load requirements. Since the input side ac/dc converter utilizes a simple PDM modulation algorithm with a feedback of the dc offset current I_d, the input current waveform is sinusoidal and operation at unity power factor is also available.

Single Phase Model - Pulse Amplitude

Fig. 2 shows the principle of this series resonant circuit utilizing a single phase model. In the circuit voltage sources $+V_d$, 0, $-V_d$ denote the the input converter voltage which is obtained by the selection of the thyristors conducting in the input bridge according to the error I_{d0}-I_d. Switch S makes this selection and controls the dc offset current I_d. Thyristor T_h represents the four thyristors to be triggered in series and Capacitor C_L is equivalent to the output three capacitors which filter the high frequency components. Current pulses i_s are distributed to the output three phases as shown in Fig. 1-b by utilizing the PDM technique.

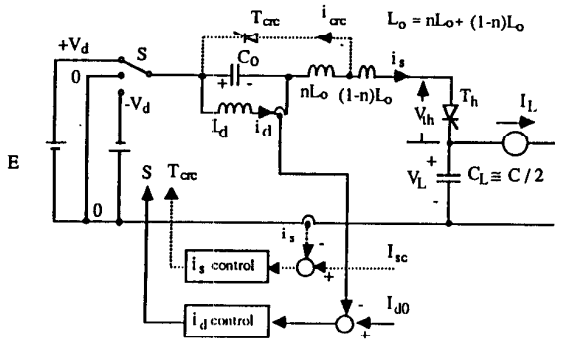

Fig. 2. Equivalent circuit for Fig.1.

From Fig.2, for E = V_d it can be written

$$-V_d + V_{C0} + V_{L0} + V_L = 0 \qquad (1)$$

where

$$V_{C0} = \frac{1}{C_0}\int_0^t i_s\,dt - \frac{I_d}{C_0}t + V_{C0I}$$

$$V_L = \frac{1}{C_L}\int_0^t i_s\,dt - \frac{I_L}{C_L}t + V_{LI}$$

$$V_{L0} = L_0\frac{di_s}{dt}$$

and V_{C0I}, V_{LI} are the initial voltages of capacitors C_0 and C_L respectively. Replacing this expressions in (1), the following differential equation is obtained:

$$\frac{d^2 i_s}{dt^2} + i_s\left(\frac{1}{C_0}+\frac{1}{C_L}\right)\frac{1}{L_0} = \left(\frac{I_d}{C_0}+\frac{I_L}{C_L}\right)\frac{1}{L_0} \qquad (2)$$

Considering

$$C_L >> C_0$$
$$I_d > I_L$$

and solving (2), the basic expression for $i_s(t)$ is

$$i_s(t) = I_d - I_d\cos\omega_0 t + C\sin\omega_0 t$$

where

$$\omega_0 = \frac{1}{\sqrt{L_0 C_0}}$$

and C is a constant determined by the voltages on the capacitors C_0 and C_L at the beginning of the pulse and by the pulse time duration. The first two pulses of Fig.3 represents an ideal condition where the duration of the pulse is

$$t_0 = \frac{2\pi}{\omega_0}$$

and the constant C reduces to zero.

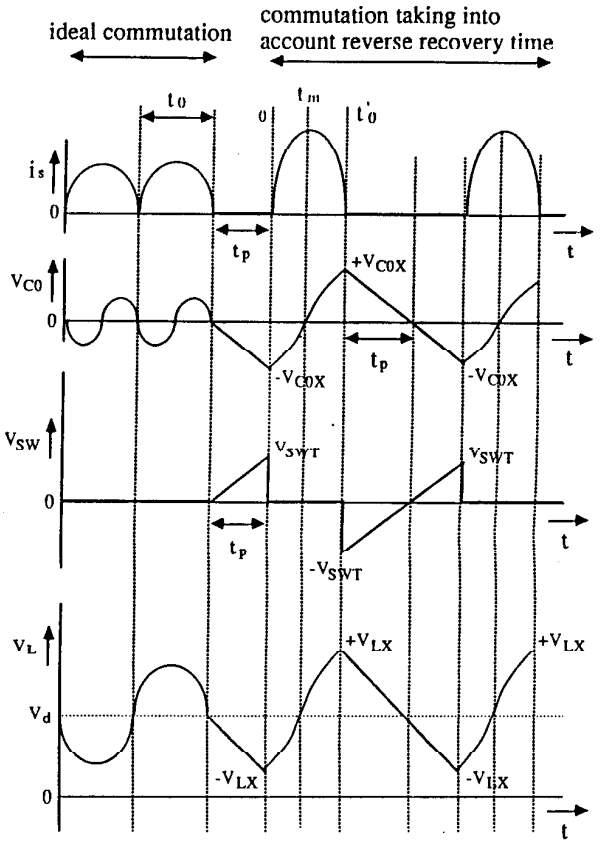

Fig. 3. Approximate waveform for the monophase resonant model.

If an allowance for the reverse recovery time of the thyristors is considered (t_p, in Fig. 3) through the requirement of a positive large voltage over T_h (V_{SWT}) a period of linear discharge of C_0 and C_L is introduced.

During the time interval t_p in Fig. 3 the voltages over the capacitors are

$$V_{C0} = V_{C0X} - \frac{I_d}{C_0}\cdot(t - t_0')$$

$$V_L = (V_d + V_{LX}) - \frac{I_L}{C_L}\cdot(t - t_0')$$

where V_{C0X} and V_{LX} are the voltages at C_0 and C_L at t = 0.

As a consequence a pulse of different amplitude will be obtained according to V_d, V_L and the initial value of the voltage across the capacitors C_0 and C_L, as can be observed in Fig. 3. The pulse has now a duration of t_0' and the constant C in expression (2) assumes a value different from zero, introducing a sinusoidal component in the current pulse.

The positive trigger voltage to be utilized can be calculated by the following expression:

$$V_{SWT} = \frac{I_d}{C_0} t_p$$

Figures 4-a, b illustrate the relationship between the current pulse i_s and its average value I_s. In Fig. 4-a at $t = t_c$, the current i_s starts to flow by triggering the thyristor T_h, and flows like a sinusoid, finally reaching zero at $t = T$ when T_h becomes off. As the peak value of i_s depends upon the initial voltage V_{th} ($t = t_c$) across the thyristor T_h, it seems reasonable to control the current is by varying V_{th} at $t = t_c$. However to control the system adequately, the average current I_s should be controlled. Fig. 4-b denotes the current pulses for higher V_{th}; the charging period t_c of the capacitor C_0 has to be longer because of the constant charging up current Id and the average current I_s does not change substantially as shown in Fig. 4-b in comparison with Fig. 4-a. However it can be noted that the peak value goes up higher. A more dominating factor to control i_s is the voltage $V_{th}(0)$(V_{th} at the beginning of the pulse). It strictly affects the average value I_s but unfortunately it cannot be controlled in the actual three phase circuit in Fig. 1. The output pulses i_s with different amplitudes are shown in Fig. 4-c due to the random voltage $V_{th}(0)$ arising from different output capacitors with different output line voltages and input voltages.

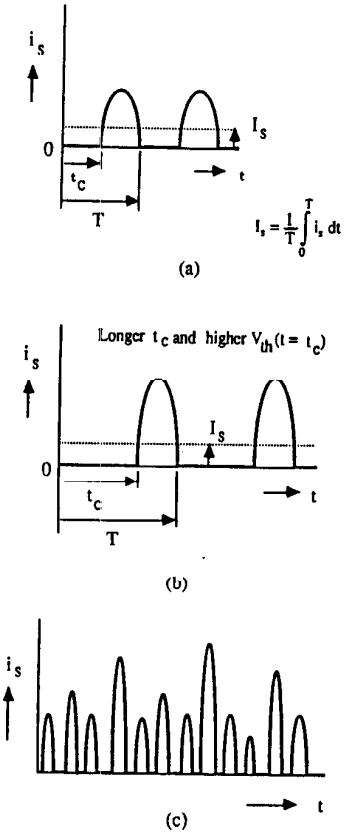

Fig. 4. Current pulses i_s in the previous system.

Current Pulse Trimming Method

To implement a trimming control method for each individual pulse, the circulating thyristor T_{CRC} is proposed. The basic objective of individual pulse control is to apply the exact amount of current into the output to produce the required voltages. At the same time, by diverting energy through the circulating thyristor T_{CRC}, excessive energy would be avoided in the capacitors C_0 and C_L.

As shown in the Fig. 5, the basic strategy is the following :
1) If the pulse amplitude of i_s becomes bigger than the required threshold value determined by the pulse trimming control, I_{sc}, T_{CRC} is triggered when i_s becomes equal to I_{sc}, as shown in Fig. 5-a.
2) When a small value of i_s current is required at the output, a better control technique was obtained triggering initially T_{CRC}; in this case I_{sc} represents the value of i_{crc} (current in T_{CRC}) in which T_h should be triggered for applying the correct pulse amplitude at the output, as shown in Fig. 5-b.

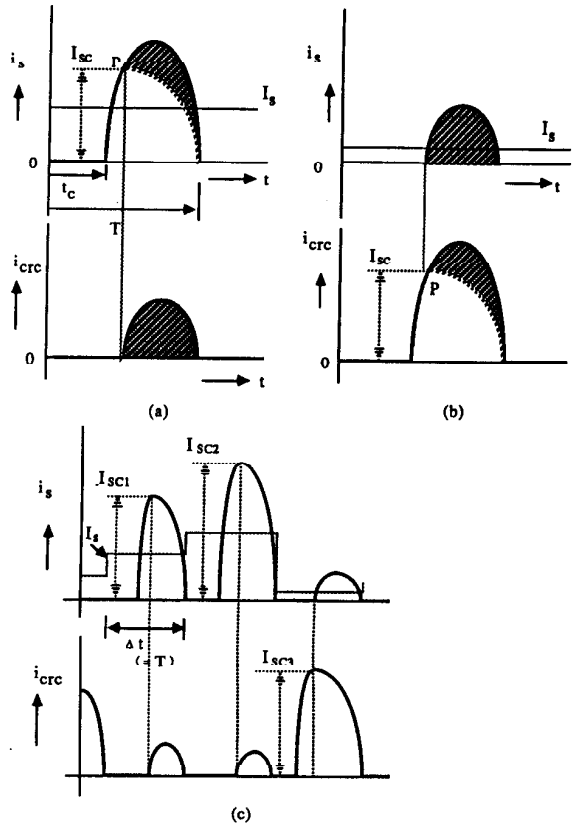

Fig. 5. Illustrating control method of current pulse control.

In this way a more precise output voltage control can be achieved and an improved energy flow is obtained in both C_0 and C_L and an optimized average i_s (I_s) is observed in the resonant current. Figure 5-c shows the general expected waveforms for i_s and i_{crc}. The output waveform will be more precise than the previous system using only the PDM method since the current pulses can be adjusted continuously from almost zero to full size. Further, the instability caused by the strong stimulation in the previous system because of large periods of charge and discharge of Co and CL would be almost avoided by the individual pulse control.

Improved Topologies

The previous topology shown in Fig. 2 requires additional *conditions for V_L and V_d to allow T_{CRC} or T_h to turn on.*

The following four modes of operation can be defined accordingly to the triggering order of T_h and T_{CRC} :

Mode 0 : T_h off , T_{CRC} off
Mode 1 : T_h on , T_{CRC} off
Mode 2 : T_h off , T_{CRC} on
Mode 3 : T_h on , T_{CRC} on

A transition from mode 1 to mode 3 (turning T_{CRC} on) would require that V_d be less than V_L during the duration of the pulse. A transition from mode 2 to mode 3 (turning T_h on) would require that V_d be greater than V_L. Since the control strategies for V_d and V_L are independent, these conditions would represent a limitation for the overall efficiency of the control system.

To increase trimming ability with more flexibility and so avoid the last requirements, two new topologies have been proposed with the inclusion of the inductor L_{CRC} as shown in Fig. 6-a and b. An extra degree of freedom is then added to the system, increasing the pulse current control ability. Both configurations were investigated for all possible combinations of V_d and V_L, with different values of positive trigger voltage for T_h and T_{CRC}. Defining swis as being:

$$swis = \frac{I_{sc}}{I_d}$$

where I_{sc} is the threshold value for i_s and i_{CRC} and I_d is the dc offset current added to i_s, characteristic triggering curves (I_s x swis) are obtained for this topology.

The system depicted in Fig. 6-b shows a much more linear characteristic triggering curve which represents an important feature in its control implementation for the three phase system. The value of L_{CRC} for which a more linear characteristic for different load conditions was obtained is $L_{CRC} = L_0/2$. Different values for the mutual inductance between L_{CRC} and (1-n)L0, M_{CRC}, were investigated but slight improvements in the characteristic triggering curves were observed. The results are presented for M_{CRC} equals to zero. The ratio between the inductances nL_0 and $(1-n)L_0$, n shows a good performance for a value equal to 0.5.

The following expressions are derived from the monophase model circuit shown in Fig. 6-b:

$$\begin{cases} v_{12} = L_{12}\, pi_s + L_{1M}\, pi_{CRC} \\ v_{13} = L_{1M}\, pi_s + L_{13}\, pi_{CRC} \end{cases}$$

$$pi_1 = pi_s + pi_{CRC}$$

$$pi_s = \frac{L_{13}\, v_{12} - L_{1M}\, v_{13}}{L_{13}\, L_{12} - L_{1M}^2}$$

$$pi_{CRC} = \frac{v_{13} - L_{1M}\, pi_s}{L_{13}}$$

$$L_{12} = L_1 + L_2$$
$$L_{13} = L_1 + L_3$$
$$L_{1M} = L_1 - M_{CRC}$$

where $p = \frac{d}{dt}$, represents the derivative operator.

Characteristic Triggering Curves for the Monophase Model

From the simulation for all possible values and combinations of V_d, V_L, n and I_{sc} the following important points can be observed from the characteristic triggering curves:

1) The value of V_d has minimum influence on the curve; V_d can assume positive, null and negative values.

2) Increasing the amplitude of V_L, a shift to the right in the characteristic curve is observed. The same slope is maintained.

3) By the introduction of a displacement factor m in the definition of swis:

$$swis = \pm \frac{I_{sc}}{I_d} = K\, I_s + m$$

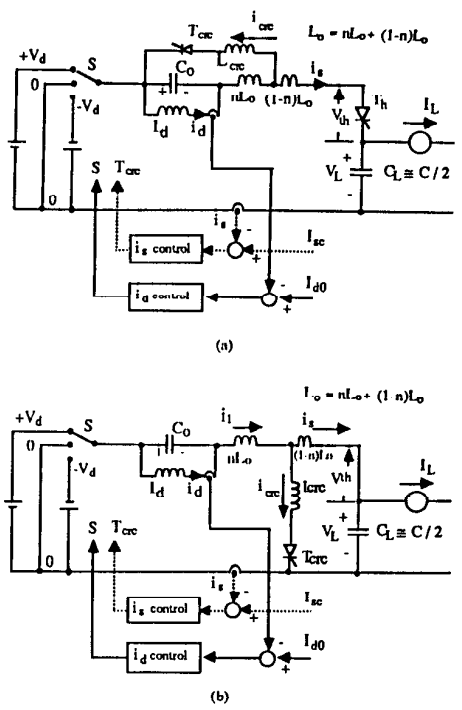

Fig. 6. Improved topologies for the monophase model with a circulating thyristor.

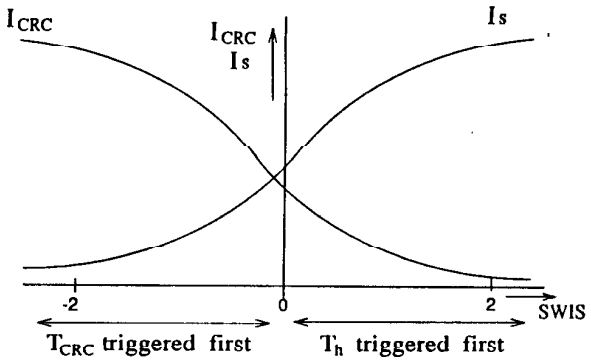

Fig. 7. Characteristic triggering curve for V_d = 300 V and V_L = 0 V.

where K is the slope and m the curve displacement for I_s equals to zero, it can be noticed that for negative values of swis T_{CRC} is triggered before than T_h, while for positive values of swis, T_h is triggered before than T_{CRC}. In this way the variable swis holds additional information for the system, that is, the triggering priority for the circulating and bridge thyristors.

4) The trigger voltage for the thyristor(s) first triggered is approximately 2 times larger than the voltage for the thyristor(s) triggered afterwards. With this procedure a safe reverse recovery time could be adjusted for the semiconductors devices.

5) The relation between the average current values can be expressed as follows

$$I_{CRC} + I_s = I_d$$

as demonstrated in Fig.7.

6) For swis smaller than -2.5, I_s reduces to zero for all values of V_L.

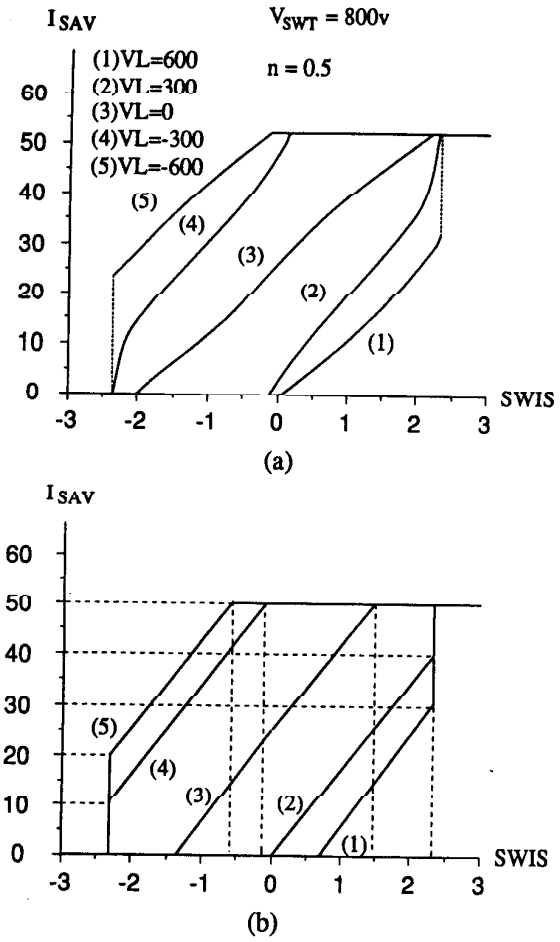

Fig. 8. Complete set of characteristic triggering curves and linearized model.

	I	II	III	IV	V	VI
ε_a	+	+	+	−	−	−
ε_b	−	−	+	−	+	+
ε_c	−	+	−	+	−	+

Fig. 9. Polarity of voltage error for each of the possible operating modes.

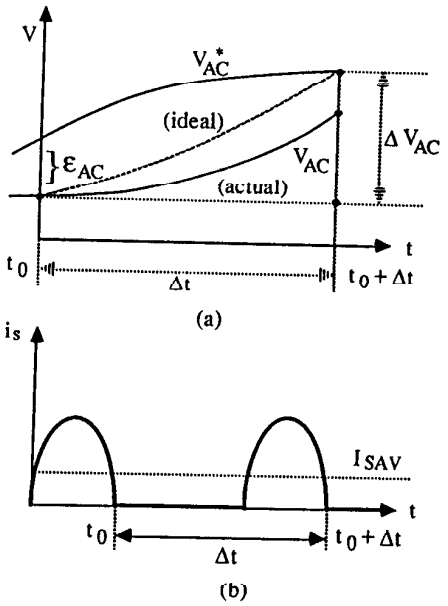

Fig. 10. Error and required correction factor for line voltages in a three phase system.

Figure 8 shows a complete set of characteristic triggering curves for the monophase model of the three phase resonant dc link system. The utilization of these curves in the control scheme would allow the determination of the values of swis from the calculated value of I_s. Consequently it is possible to establish whether T_{CRC} or T_h is first triggered and the threshold value of the current pulse that would make the second thyristor to be triggered.

Control Strategy

A. Voltage Feedback Loop Control

For the control of the output voltage in a three phase converter a voltage feedback loop of the load line to line voltage is utilized. These voltages are compared with a set of three phase voltage references and three errors (ε_{ab}, ε_{bc}, ε_{ca}) are generated, such that:

$$\varepsilon_{ab} + \varepsilon_{bc} + \varepsilon_{ca} = 0$$

All three errors clearly can not have the same polarity. The triggering principle is:
(i) The thyristor in the phase having the larger error out of the two phases of the same polarity is chosen to be triggered.
(ii) The phase corresponding to the error with the opposite polarity error is selected as the other triggering phase.

Fig. 9 shows the table of possible combination of errors that can be obtained and the possible operation modes.

B. Voltage Error Minimization Process

From the phase selection step utilizing voltage errors, two thyristors are chosen to be triggered corresponding to the phases x and y (a, b or c).

Figure 10-a shows the determination of the voltage error at the instant t_0 and the required correction factor for line voltages (ΔV) necessary after a pulse of the current i_s is delivered to the load. The quantity Δt represents the duration of the pulse as can be seen in Fig. 10-b.

For determination of the voltage V_{ac} the following expressions are valid:

$$\varepsilon_{ac}^* = V_{ac}^*(t_0) - V_{ac}(t_0)$$

$$\Delta V_{ac} = V_{ac}^*(t_0+\Delta t) - V_{ac}(t_0)$$

After the application of a current pulse i_s the amount of current delivered to the system should be such that the required correction factors for line voltages (ΔV_{ab}, ΔV_{bc}, ΔV_{ca}) are obtained.

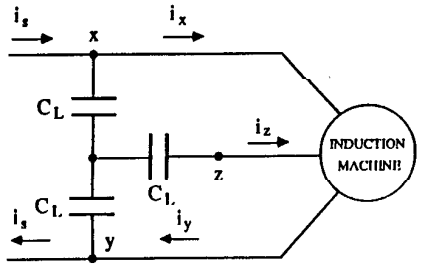

Fig. 11. Three phase configuration for output capacitor bank and load.

From the three phase configuration the output circuit is shown in Fig. 11.

From Fig. 11, the required correction factor for line voltages necessary after each pulse can be easily determined, assuming constant current during the interval Δt.

$$\Delta V_{xy} = (i_s - i_x + i_s - i_y) \frac{\Delta t}{C_L}$$

$$\Delta V_{zy} = (- i_z + i_s - i_y) \frac{\Delta t}{C_L}$$

$$\Delta V_{xz} = (i_s - i_x + i_z) \frac{\Delta t}{C_L}$$

Defining:

$$\Delta q_x = i_x \Delta t$$
$$\Delta q_z = i_z \Delta t$$
$$\Delta q_y = i_y \Delta t$$
$$\Delta q_s = i_s \Delta t$$
$$\Delta q_{xy} = C_L \Delta V_{xy}$$
$$\Delta q_{zy} = C_L \Delta V_{zy}$$

these expressions can be written:

$$\Delta q_{xy} = 2\Delta q_s - \Delta q_x - \Delta q_y \qquad (3)$$

$$\Delta q_{zy} = \Delta q_s - \Delta q_z - \Delta q_y \qquad (4)$$

$$\Delta q_{xz} = \Delta q_s - \Delta q_x + \Delta q_z \qquad (5)$$

Since it is not possible to find an amount of current $i_s(\Delta q_s)$ that could perfectly eliminate the voltage error in all three phases, a minimization process should be applied. Defining $\Delta\varepsilon_{xy}$, $\Delta\varepsilon_{xy}$, $\Delta\varepsilon_{xz}$ as being the introduced errors in each phase when a certain Δq_s is chosen, (3), (4) and (5) can be rewritten as:

$$\Delta\varepsilon_{xy} = 2\Delta q_s - (\Delta q_x + \Delta q_y + \Delta q_{xy})$$
$$\Delta\varepsilon_{zy} = \Delta q_s - (\Delta q_z + \Delta q_y + \Delta q_{zy})$$
$$\Delta\varepsilon_{xz} = \Delta q_s - (\Delta q_x - \Delta q_z + \Delta q_{xz})$$

Since only two phases are active in each pulse, two minimization processes can be considered, taking into account two or three of the introduced errors. The minimization processes are the following:

a) Defining

$$\Delta\varepsilon^2 = \Delta\varepsilon_{xy}^2 + \Lambda\varepsilon_{zy}^2$$

and calculating Δq_s such that:

$$\frac{d\Delta\varepsilon^2}{d\Delta q_s} = 0$$

results

$$\Delta q_s = \frac{1}{5} [2 (\Delta q_x + \Delta q_y + \Delta q_{xy}) + \Delta q_z + \Delta q_y + \Delta q_{zy}]$$

when just the two active phases are considered in this process.

b) Defining

$$\Delta\varepsilon^2 = \Delta\varepsilon_{xy}^2 + \Delta\varepsilon_{zy}^2 + \Delta\varepsilon_{xz}^2$$

and calculating Δq_s in the same way, results

$$\Delta q_s = \frac{1}{2} (2 \Delta q_x + \Delta q_z + \Delta q_{xy})$$

when the three phases are considered for error minimization.

From simulation it could be observed that better results were obtained from the second minimization process.

C. Compensation process

Considering the fact that it is possible to increase the output voltage tracking efficiency if the average value of the output line to line voltage ($\overline{V_{xy}}$) is utilized instead of its instantaneous value and the fact that in t_0 an accumulated error already exists. a compensation process can be implemented.

Fig. 12 represents the average value of the output voltages and the compensated errors and required compensated voltage factor for the line voltage V_{ac}.

The compensated voltage error is

$$\varepsilon_{cac} = V_{ac}^*(t_0) - \overline{V_{ac}}(t_0)$$

and the compensated required voltage factor is defined as

$$\Delta_c V_{ac} = \Delta V_{AC} + \varepsilon_{cac}$$

In this way a better performance of the voltage regulator was obtained and more precise sinusoidal waveforms were observed in the output.

D. Overall Control

Figs. 13 and 14 show the complete control scheme utilizing a voltage feedback loop, a minimization process step for obtaining minimum errors in the line voltages and an implementation of the linearized characteristic triggering curves from the monophase model.

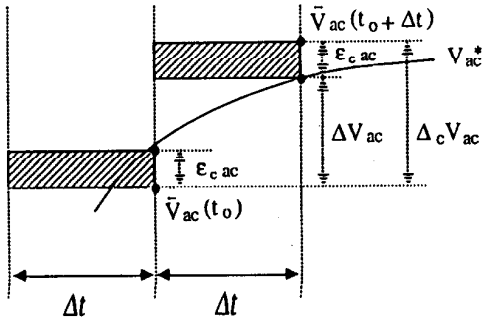

Fig. 12. Compensation process utilizing average value for line to line voltages.

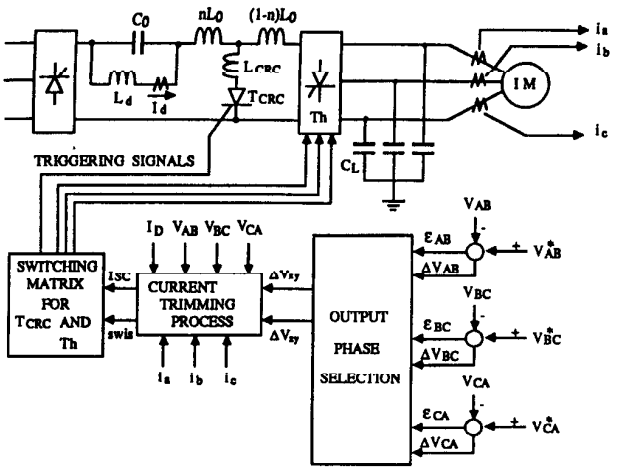

Fig. 13. Overall diagram for current pulse control of series resonant dc link converter.

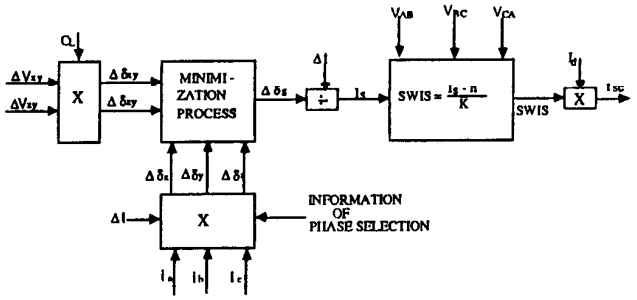

Fig. 14. Detailed block diagram for the current trimming process.

The amount of current i_s to be delivered to the load is the output of the minimization process, being then utilized to obtain the correct value of swis that will determine the threshold value for the pulse current and the triggering priority order for T_{CRC} and T_h (three phase bridge in the three phase model).

This information - I_{sc} and swis - is then input into the general switching matrix responsible for the liberation of the triggering signal for T_{CRC} and the three phase current source inverter bridge. In this way the amount of current i_s applied to the output should be the value that will cause a minimum line to line voltage (and consequently current) error in the three phase system.

The output voltage of the input rectifier is chosen from the error determined by the regulation of I_d, as being $+V_d$, 0, $-V_d$.

In Figs. 12 and 13, x and y are the two general phases selected to be triggered in the output converter.

E. Resulting Waveforms

The waveforms obtained from digital simulation are shown in Figs. 15 and 16. Nearly sinusoidal voltages and currents can be observed in the system and no oscillation was noticed for a wide variety of output voltages and currents.

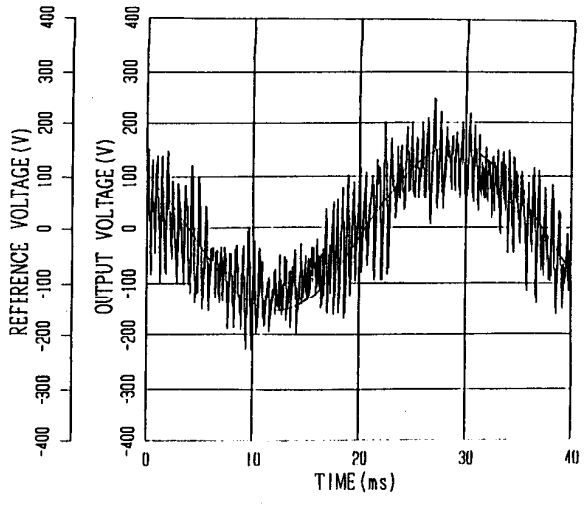

Fig. 15. Simulated waveforms(f = 30 Hz.).

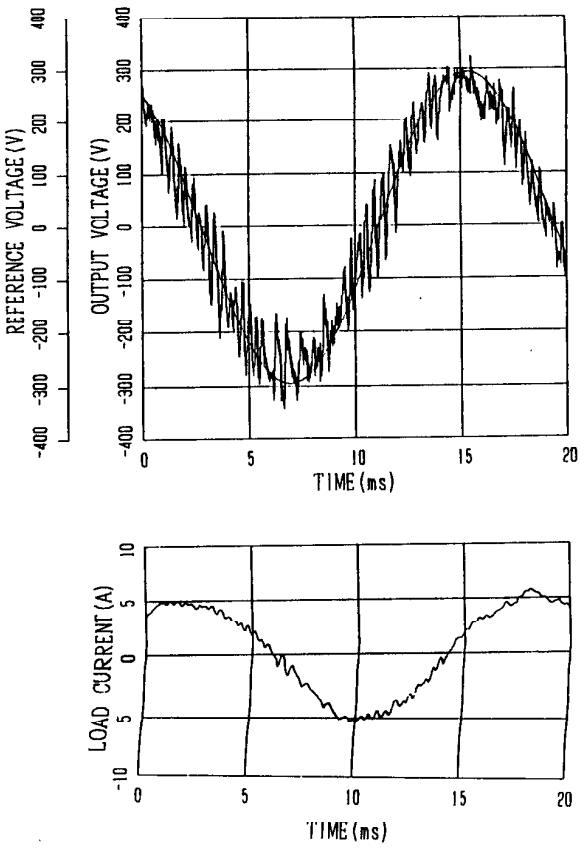

Fig. 16. Simulated waveforms(f = 60 Hz.).

Conclusion

In this paper a trimming method of the pulse obtained in a high frequency series resonant dc-link ac/ac converter was proposed and described. Oscillations were obtained in this kind of conversions due to the overexcitation of the link capacitor C_0 and the output capacitor C_L. A different combination of the output voltage of the input converter and load voltage caused uncontrolable pulse current i_s.

With the proposed scheme this problem was eliminated. Characteristic triggering curves were established for the monophase model and implemented in a three phase control strategy. A minimization process for the output voltage error was investigated. It was shown that the current pulses can be trimmed depending on the calculated threshold value of the required amount of i_s and the triggering priority between T_{CRC} and T_h.

Sinusoidal waveforms of voltage and current were obtained in the input and output and unitary power factor operation is available through an adequate power control scheme.

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