The College of Engineering
University of Wisconsin-Madison

Wisconsin Electric Machines and Power Electronics Consortium

Research Report
89-24

IMPLEMENTATION OF A CONTROLLED RECTIFIER USING AC-AC MATRIX CONVERTER THEORY

D.G. Holmes
Dept. of Elec. & Computer Sys. Engrg.
Monash University
Wellington Road, Clayton
Melbourne, Australia, 3168

T.A. Lipo
Dept. of Electrical & Computer Engrg.
University of Wisconsin-Madison
1415 Johnson Drive
Madison, WI 53706-1691

WEMPEC

Department of Electrical and Computer Engineering
1415 Johnson Drive
Madison, Wisconsin 53706

IMPLEMENTATION OF A CONTROLLED RECTIFIER USING AC-AC MATRIX CONVERTER THEORY

D.G. Holmes
Dept. of Elec. & Computer Sys. Engineering
Monash University
Wellington Road, Clayton
Melbourne, Australia, 3168

T.A. Lipo
Dept. of Elec. & Computer Engineering
University of Wisconsin-Madison
1415 Johnson Drive
Madison, WI, 53706

Abstract It is well known that a PWM controlled rectifier can offer advantages of reduced low order harmonics and unity input power factor when compared to a conventional thyristor converter. However, current optimum PWM strategies are often difficult to physically implement, or not easily extended to regenerative operation. This paper proposes an alternative PWM strategy based on current ac-ac matrix converter theory, which generates only high order switching harmonics, presents a unity power factor load to the supply, implicitly extends to regeneration (and operation with a center tapped dc output), and is feasible to physically implement for real-time output voltage control. Both the theory and physical simulation results are presented in the paper.

Introduction

It is well known that a pulse width modulated rectifier (or ac-dc converter) can ideally produce a variable ripple free dc output current while drawing sinusoidal input current from the supply at unity power. In contrast, a conventional thyristor converter produces substantial output voltage and input current low order harmonics and operates at a lagging power factor which becomes progressively worse as the output voltage is reduced. Hence, attention is increasingly being directed to modulation strategies which improve the performance of ac-dc rather than dc-ac power converters.

Significant improvements in performance over a conventional thyristor converter can be achieved by using a PWM switched GTO bridge [1], which reduces low order harmonics at the expense of increased high order components, and provides unity input power factor operation. However, real time implementation of such PWM switching algorithms can be difficult.

It is well known that the so-called ac-ac matrix converter is optimal from the point of view of minimum switch number and minimum filtering requirements. The voltage output is an optimal pattern based on the constraint of fixed modulation frequency, minimum harmonic distortion output and prescribed fundamental power factor at the input. The power factor at the input is readily adjusted over a range determined by the power factor of the output. The modulation strategy which produces these benefits has been derived in rigorous form by Venturini and Alesina [2,3]. Thus far, however, the benefits of these powerful modulation strategies have not been exploited for other input/output requirements.

This paper proposes to utilize the Venturini switching theory by employing a reduced ac-ac matrix converter as an ac-dc converter. The implementation is achieved by setting the desired output frequency to zero, leaving one output phase unconnected and allowing dc current to flow through a load connected across the other two phases. The resulting converter draws sinusoidal input current at unity input power factor over the full range of output voltage, generates only high order switching harmonics, and is easily extended to regenerative or center tapped operation. Moreover, the switching algorithm is readily implemented in real time using modern microprocessors.

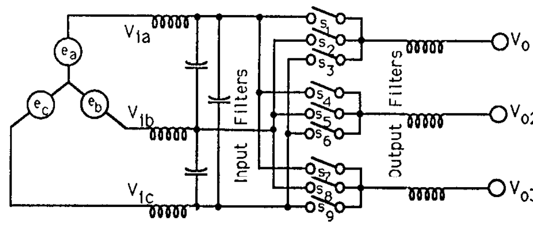


Fig. 1 Three Phase AC/AC Matrix Converter.

Review of AC-AC Matrix Converters

A three phase ac-ac matrix converter basically consists of 9 bi-directional voltage blocking, current conducting switches arranged in a matrix so that any input phase can be connected to any output phase at any time, Fig. 1. In principle, for a given set of input three phase voltages, any desired set of output voltages can then be synthesized by suitably toggling the matrix switches.

The ac-ac matrix topology was first investigated in 1976 [4] and then more recently using a generalized high frequency switching strategy [2]. Reference 2 reported a limited output to input voltage ratio (0.5), but a more recent paper [3] demonstrates how zero sequence third harmonic voltage components can be added to the desired ac output voltage so as to increase the voltage transfer ratio to 0.866. The scheme proposed in Ref. 4 also implicitly generates sinusoidal input currents (except for switching harmonics) at unity power factor, independent of the power factor of the output load current.

Other researchers have also investigated the operation of matrix converters using PWM converter and inverter switching strategies [5,6], but their approach generally gives higher levels of harmonic distortion and is difficult to implement in a real-time controller [7]. Furthermore, the input power factor is generally not independent of the output power factor in such schemes.

Physical Limits on the Operation of a Matrix Converter

For a three phase matrix converter, the fundamental requirement can be stated as follows. Given a set of 3 phase input voltages:

$$\left[V_i(t)\right] = \begin{bmatrix} V_i \cos(\omega_i t) \\ V_i \cos(\omega_i t - 2\pi/3) \\ V_i \cos(\omega_i t + 2\pi/3) \end{bmatrix} \quad (1)$$

determine the switching function M(t) which will produce the set of 3 phase output voltages:

$$\left[V_o(t)\right] = [M(t)]\cdot\left[V_i(t)\right] = \begin{bmatrix} V_o \cos(\omega_o t + \theta_o) \\ V_o \cos(\omega_o t + \theta_o - 2\pi/3) \\ V_o \cos(\omega_o t + \theta_o + 2\pi/3) \end{bmatrix} \quad (2)$$

where θ_o = arbitrary output voltage phase angle.

Irrespective of the switching strategy adopted, there are, however, physical limits on the output voltage achievable with this system, as follows. Consider the three phase input voltage envelopes of Fig. 2(a). For complete control of the output voltage at any time, the envelope of the target output voltages must be wholly contained within the continuous envelope of the input voltages. This constraint limits the available output voltage to 0.5 of the input voltage. This limit can be improved by adding a third harmonic at the input frequency to all target output voltages. The addition of this third harmonic modulates the available output voltage envelope to follow the maximum possible input voltage continuous region (Fig 2(b)), and hence increases the available output voltage range to 0.75 of the input when the third harmonic has a peak value of $V_i/4$ (Fig 2(c)). Further improvement of the transfer ratio can be achieved by subtracting a third harmonic at the output frequency from all target output voltages to minimize the range of the output voltage envelope to 0.866 of the peak phase voltage, Fig. 2(d), which allows an absolute maximum transfer ratio of 0.75/0.866 = 0.866 of V_i when this third harmonic has a peak value of $V_o/6$

To achieve the maximum output voltage magnitude, the desired output voltage then becomes:

$$\left[V_o(t)\right] = [M(t)]\cdot\left[V_i(t)\right]$$

$$= \begin{bmatrix} V_o \cos(\omega_o t + \theta_o) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \\ V_o \cos(\omega_o t + \theta_o - \frac{2\pi}{3}) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \\ V_o \cos(\omega_o t + \theta_o + \frac{2\pi}{3}) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \end{bmatrix} \quad (3)$$

In 1981, Venturini and Alesina [2] demonstrated how a low frequency modulation function [m(t)] can be considered equivalent to [M(t)], provided the switching frequency is high, and input and output low pass filters are installed on the converter. In 1988 [3], they presented an analytic solution for such a modulating function which achieves the maximum possible output voltage transfer ratio (0.866). This solution is presented in the next section with minor modifications to suit the ac-dc converter application.

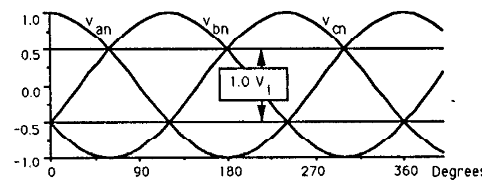


Figure 2(a) - Output PU Amplitude Limits of Basic Matrix Converter

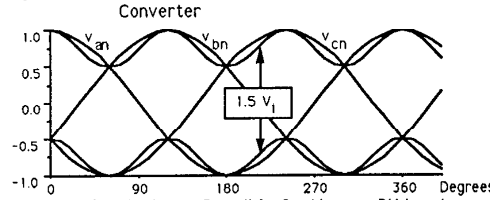


Figure 2(b) - Maximum Possible Continuous PU Input Voltage Envelope for Matrix Convertor

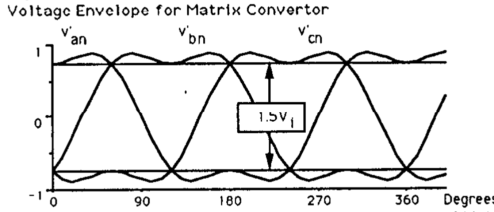


Figure 2(c) - Available PU Output Voltage Envelope of Matrix Converter with Input Third Harmonic Added to Output Voltages

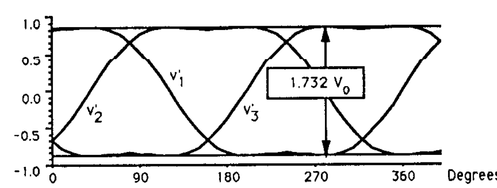


Figure 2(d) - PU Output Voltage Envelope of Matrix Converter withOutput Third Harmonic Subtracted from Output Voltages

Fig. 2 Physical Operating Limits for AC/AC Matrix Converter.

Modulation Strategy for an AC/AC Matrix Converter

The problem at hand is to find a low frequency modulation strategy [m(t)] such that

$$[V_o(t)] = [m(t)]\cdot[V_i(t)] = V_o \begin{bmatrix} \cos(\omega_o t + \theta_o) \\ \cos(\omega_o t + \theta_o - \frac{2\pi}{3}) \\ \cos(\omega_o t + \theta_o + \frac{2\pi}{3}) \end{bmatrix}$$

$$+ \frac{V_o}{2\sqrt{3}} \begin{bmatrix} \cos(3\omega_i t) \\ \cos(3\omega_i t) \\ \cos(3\omega_i t) \end{bmatrix} - \frac{V_o}{6} \begin{bmatrix} \cos(3\omega_o t + 3\theta_o) \\ \cos(3\omega_o t + 3\theta_o) \\ \cos(3\omega_o t + 3\theta_o) \end{bmatrix}$$

$$= \quad [A] \quad + \quad [B] \quad + \quad [C] \tag{4}$$

where $[V_i(t)]$ is defined by Eq. 1 above, and the elements of [m(t)] are limited by the existence constraint:

$$0 \le m_{ij} \le 1 \quad \text{for} \quad 1 \le i \le 3,\ 1 \le j \le 3 \tag{5}$$

and the current continuity constraint

$$\sum_{j=1}^{3} m_{ij} = 1 \quad \text{for} \quad 1 \le i \le 3 \tag{6}$$

Note that the scale factor for the [B] output voltage set has been changed to enable the analytic solution to be determined. This does not affect the output voltage waveform, since the scale factor equals $V_i/4$ at the maximum transfer ratio.

Consider the partial output voltage set [A] in Eq. 4. This voltage set can be obtained by multiplying the input voltage either by a positive sequence set of $(\omega_o + \omega_i)$ sinusoids, or by a negative sequence set of $(\omega_o - \omega_i)$ sinusoids, as follows:

$$[m]_A = \frac{\beta_1}{3} \begin{bmatrix} m_+(1) & m_+(2) & m_+(3) \\ m_+(2) & m_+(3) & m_+(1) \\ m_+(3) & m_+(1) & m_+(2) \end{bmatrix} + \frac{\beta_2}{3} \begin{bmatrix} m_-(1) & m_-(3) & m_-(2) \\ m_-(2) & m_-(1) & m_-(3) \\ m_-(3) & m_-(2) & m_-(1) \end{bmatrix} \tag{7}$$

where: $m_+(i) = \cos((\omega_o + \omega_i)t + \theta_o - (i-1)2\pi/3)$,
$m_-(i) = \cos((\omega_o - \omega_i)t + \theta_o - (i-1)2\pi/3)$.

Balance of power considerations through the converter give

$$\beta_1 = \frac{V_o}{V_i}\left(1 - \frac{\tan\phi_i}{\tan\phi_o}\right); \quad \beta_2 = \frac{V_o}{V_i}\left(1 + \frac{\tan\phi_i}{\tan\phi_o}\right) \tag{8}$$

where: ϕ_o = load output power factor,
ϕ_i = desired input power factor.

A similar approach for partial output voltage sets [B] and [C] gives

$$[m]_B = \frac{\gamma_1}{3} \begin{bmatrix} n_+(1) & n_+(2) & n_+(3) \\ n_+(1) & n_+(2) & n_+(3) \\ n_+(1) & n_+(2) & n_+(3) \end{bmatrix} + \frac{\gamma_2}{3} \begin{bmatrix} n_-(1) & n_-(3) & n_-(2) \\ n_-(1) & n_-(3) & n_-(2) \\ n_-(1) & n_-(3) & n_-(2) \end{bmatrix} \tag{9}$$

where: $n_+(i) = \cos((4\omega_i t - (i-1)2\pi/3)$
$n_-(i) = \cos((2\omega_i t - (i-1)2\pi/3)$

and: $\gamma_1 + \gamma_2 = V_o/(\sqrt{3}\, V_i)$.

$$[m]_C = \frac{\delta_1}{3} \begin{bmatrix} q_+(1) & q_+(2) & q_+(3) \\ q_+(1) & q_+(2) & q_+(3) \\ q_+(1) & q_+(2) & q_+(3) \end{bmatrix} + \frac{\delta_2}{3} \begin{bmatrix} q_-(1) & q_-(3) & q_-(2) \\ q_-(1) & q_-(3) & q_-(2) \\ q_-(1) & q_-(3) & q_-(2) \end{bmatrix} \tag{10}$$

where: $q_+(i) = \cos[(3\omega_o+\omega_i)t + 3\theta_o - (i-1)2\pi/3)]$,
$q_-(i) = \cos[(3\omega_o-\omega_i)t + 3\theta_o - (i-1)2\pi/3)]$

and: $\delta_1 + \delta_2 = -V_o/(3V_i)$.

To satisfy the current continuity constraints Eq. 6, a 3x1 identity matrix is added to [m(t)], to make the complete solution:

$$[m(t)] = \frac{1}{3}[I] + [m]_A + [m]_B + [m]_C \tag{11}$$

The coefficients $\gamma_1, \gamma_2, \delta_1, \delta_2$ are chosen so as to maximize the transfer ratio v_o/v_i without violating the existence constraint, Eq. 5, and are found to be:

$$\gamma_1 = \frac{-1}{6\sqrt{3}}\frac{v_i}{v_o}; \qquad \gamma_2 = \frac{7}{6\sqrt{3}}\frac{v_o}{v_i}$$

$$\delta_1 = \frac{-1}{6}\frac{v_o}{v_i} \qquad \delta_2 = \frac{-1}{6}\frac{v_o}{v_i} \tag{12}$$

For each switching period, the modulation strategy then becomes:

(1) Calculate the scale coefficients $\beta_1, \beta_2, \gamma_1, \gamma_2, \delta_1, \delta_2$ for the required v_o/v_i ratio,
(2) Calculate the modulation function sinusoidal values for the current time instance (typically from a look up table),
(3) Calculate the composite modulation function values [m(t)],
(4) Arrange to turn on switches 1-9 for the period $t_i = m_i(t)\Delta t$.

The arithmetic requirements for this computation are primarily sinusoidal lookup, with 9 multiplications. Any reasonably high speed microprocessor with a hardware multiply facility can manage this computing load in real time, even at switching periods of several kHz. Hence on-line implementation of this algorithm is quite feasible.

Using a Matrix Converter as an AC/DC Rectifier

To operate a matrix converter as an ac-dc rectifier, the output frequency is set to zero, and the output voltage phase angle is set to 30°. This sets the output phases to maximum, minimum and zero voltage respectively as shown in Figure 3. A maximum dc voltage of $1.5*V_i$(peak) is then achievable between the two extreme phases (if the "ac" output voltage magnitude is set to 0.866 of V_i), while the third phase is available as a zero voltage center tap terminal.

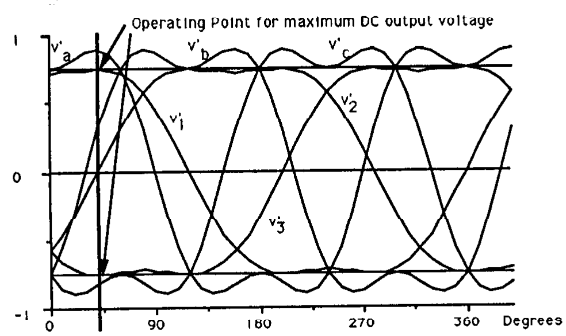


Fig. 3 Operation of Matrix Converter as DC Rectifier.

The implementation of a full ac-ac matrix converter requires 9 bi-directional switches as shown in Fig. 1. Since no generic bi-directional switches are yet available, this can be implemented using 18 uni-directional switches (every two switches are connected back-to-back to make one bi-directional switch). However, for the controlled rectifier implementation, the number of uni-directional switches required can be substantially reduced, as follows:

(a) For a single ended dc output, the load impedance is connected between the two extreme phases (Fig 4(a)), and the 3 bi-directional switches of the zero voltage phase need not be physically implemented, since they do not carry current. Output voltage control is achieved by modulating the target output voltage magnitude (V_o) between 0V and $0.866V_i$.

This configuration will support load regeneration implicitly, since the remaining 6 switches are bi-directional, and hence it has potential as a regenerative dc motor drive. Such drives are conventionally implemented using a separate forward and reverse SCR or PWM bridge [8], and usually require either deadtime or careful bridge firing control to cross over from motoring to regeneration. The matrix converter requires no such consideration, since bi-directional current flow is implicit within the modulation algorithm. Effectively, the modulation controller chooses to reverse the load power factor, and the bridge follows within one switching cycle (ignoring inductive transients caused by reversing impulse currents, which must be snubbed).

The matrix converter requires 12 uni-directional switches to implement the 6 bi-directional switches that are required, but this is no worse than the 12 uni-directional switches required by the conventional dual-bridge approach, and has the advantage of implicit regenerative cross-over without the need for dead time.

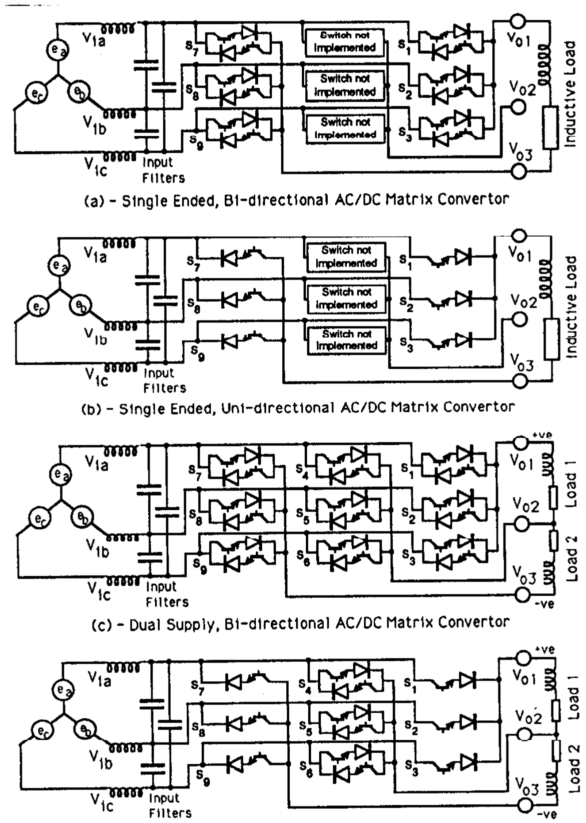
(b) For a single ended dc output with no regenerative capability, the 6 bi-directional switches of (a) above can be made unidirectional, since they now only conduct current in one direction (Fig. 4(b)). In this configuration, the converter has the same topology as a standard PWM controlled rectifier, and uses the same number of switches. No free-wheeling diodes are required to carry the inductive load current, since the Venturini algorithm implicitly creates a continuous load current path as a condition of its solution. This topology also has the advantage of being able to generate a positive or a negative output voltage simply by a modulation change (i.e. add 180° to the output voltage arbitary phase angle).

(c) The converter also can be used to create a dual centre tapped dc supply, with regenerative capability on both the positive and negative supply. This has particular interest for reluctance motor drives, and to the authors' knowledge cannot be achieved by any other single bridge topology. To operate in this mode, load impedances are connected between the zero voltage third phase and the two extreme voltage phases (Fig 4(c)).

The load impedances need not be balanced, since the resulting dc load currents can be viewed as a time snap-shot of an ac load with non-unity power factor. Hence the load currents are simply out of phase with the load voltage. Since the Venturini algorithm decouples the input and the output power factor of the converter, the supply input currents remain sinusoidal at unity power factor irrespective of the state of the output load currents.

This implementation requires the complete set of 9 bi-directional switches, but offers a capability which cannot be matched by any other single bridge topology.

(d) Some reduction in number of switches in (c) above can be achieved by operating the converter as a dual centre tapped dc supply without regenerative capability. In this case, the upper phase switches can be made uni-directional in the forward direction, and the lower phase switches can be made uni-directional in the reverse direction (Fig 4(d)). However, bi-directional switches are still required for the zero voltage phase to conduct the difference between between the positive and negative phase currents under unbalanced load conditions. Hence 12 switches are still required to implement the converter - the same number as would be required to implement two conventional SCR or PWM bridges side-by-side. However, the matrix converter implementation offers the advantage of implicit tracking of the positive and the negative supplies, controlled by one modulating system.



(a) - Single Ended, Bi-directional AC/DC Matrix Convertor

(b) - Single Ended, Uni-directional AC/DC Matrix Convertor

(c) - Dual Supply, Bi-directional AC/DC Matrix Convertor

(d) - Dual Supply, Uni-directional AC/DC Matrix Convertor

Fig. 4 Alternative Topologies for AC/DC Matrix Converter.

Simulation Results

The converter has been extensively investigated in simulation, both theoretically and as a simulated physical implementation. The theoretical simulation assumes infinite switching frequency, and was used to confirm the equivalent low frequency transfer function developed in equations [4] to [12] earlier. The physical simulation represents the converter as a set of ideal bi-directional switches coupled into differential equations which represent the load impedance, source impedance and filter elements as physical resistances, inductances and capacitors. The switching algorithm is implemented as discrete time step switch transitions which cause discontinuities to these differential equations.(exactly as the real physical converter currently under construction will be switched) This physical simulation has been used to confirm the converter operation in detail under a variety of operating conditions, including different switching switching frequencies, single and dual dc supply configurations, and a variety of load types. In particular, this simulation has been used to confirm the specific current flow through each simulated bi-directional switch under various operating conditions.

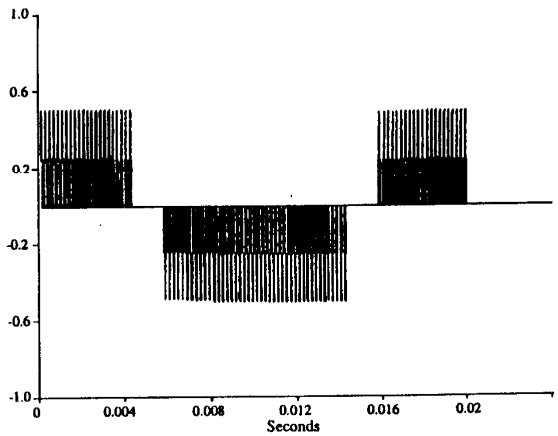
Results are presented in Figures 5,6,7,8 for the case of single ended dc output, feeding an inductive/resistive load, with LC filters on the input phases (Figure 4(b)). The switching rate was set at 5 kHz, the input LC filters have a natural resonant cut-off frequency at 1.5 kHz, and the load has a time constant of 3.3 milliseconds.

Figure 5 shows the instantaneous current feeding into phase a of the converter (time and frequency domain). As predicted by theory, the only significant harmonic components are centered around the switching frequency, with virtually no significant low order harmonics.

Figure 6 shows the supply input current drawn by the converter through the input LC filter (time and frequency domain). (The input inductance is partly due to the voltage source impedance which cannot be eliminated), The high order switching harmonics have been virtually eliminated, leaving only a unity power factor sinusoidal input current. Note that the initial deviation of the input current waveform from sinusoidal is only due to initial condition perturbations of the simulation

Figure 7 shows the instantaneous output voltage from the converter (time and frequency domain). Again, the only significant harmonics are of the order of the switching frequency.

Figure 8 shows the output load current, filtered only by the load inductance (time and frequency domain). Once more, all switching harmonics have been eliminated by the filtering, leaving only the desired dc component.



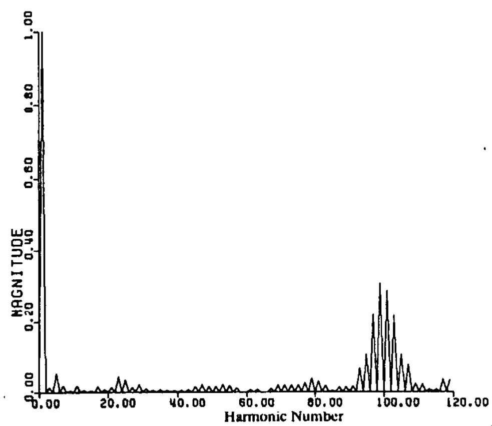
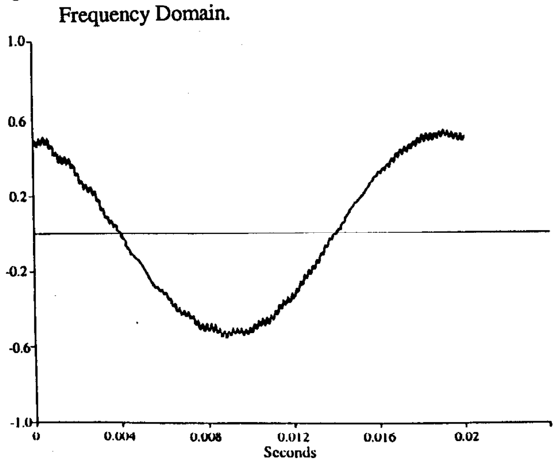


Fig. 5 Converter Input Current. (a) Time Domain, (b) Frequency Domain.



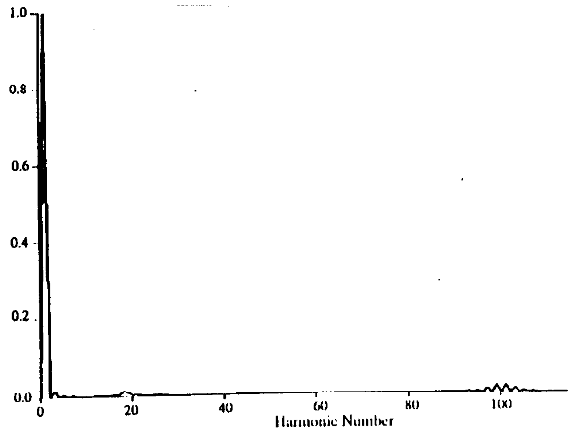
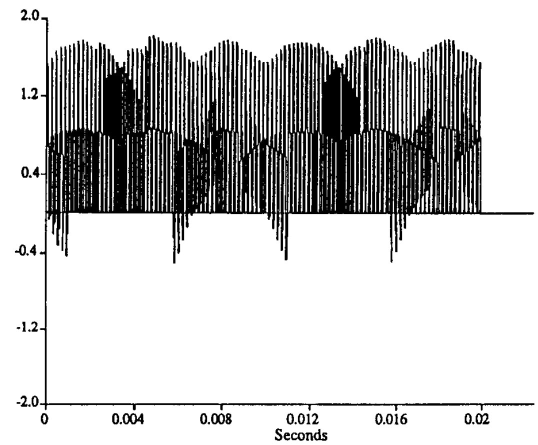


Fig. 6 Filtered Line Input Current. (a) Time Domain, (b) Frequency Domain.



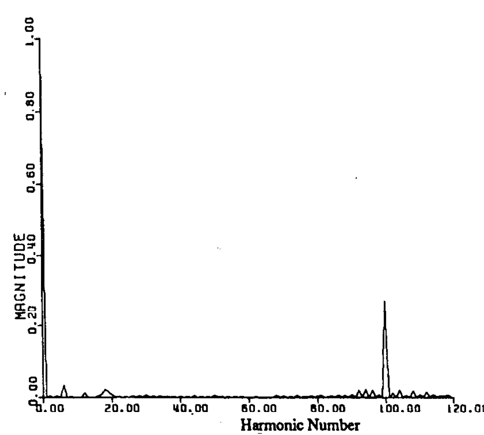
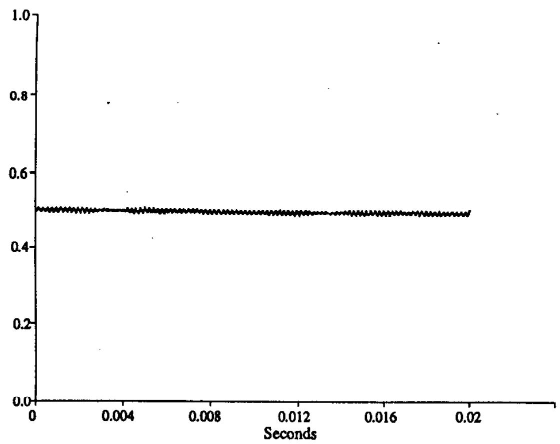


Fig. 7 Converter Output Voltage. (a) Time Domain, (b) Frequency Domain.



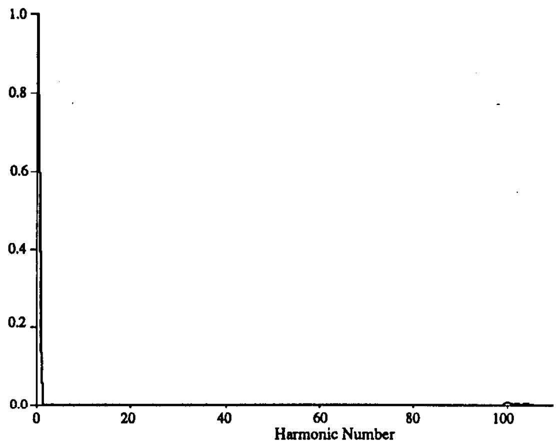


Fig. 8 Inductive Load Current. (a) Time Domain, (b) Frequency Domain.

A variety of other operating conditions have also been simulated (especially including operation as a center tapped supply), and in all cases the converter operated as predicted by theory. Of particular note is the fact that the frequency of the harmonic components produced by the converter does not vary significantly with changes in output voltage, in contrast to other PWM switching strategies. Hence the input filters can be matched to a small frequency range of high order input harmonics without having to be detuned to trap a wider range of input harmonics which vary as the modulation ratio changes.

Conclusions

Controlled rectifiers using PWM switching strategies are currently attracting considerable interest, because of their ability to minimize low order harmonics and to present unity power factor loads to the ac supply. However, many of the modulation techniques proposed are difficult to implement on-line, or do not extend to regeneration or center tapped operation.These limitations can be overcome by using ac-ac matrix converter theory, without any additional hardware penalty.

The main benefits of the proposed modulation strategy are four fold:

(i) the algorithm is readily implemented in real time, unlike most other optimal PWM strategies;

(ii) the input current is implicitly sinusoidal with unity power factor (except for high order switching harmonics);

(iii) regenerative operation is implicit by constructing the converter using bi-directional switches (no dead time going from forward to reverse power flow)

(iv) operation as a center-tapped dc supply, with regeneration, is also implicit, and is easily implemented with three additional bi-directional switches.

References

[1] D.G. Holmes and C.H Vun, *A Multiple Microprocessor System to Control a GTO Based D.C. Machine Drive*, 1987 I.E. Aust. Electric Energy Conf, Adelaide, pp. 141-146.

[2] M.G.B. Venturini and A. Alesina, *Solid State Power Conversion: A Fourier Analysis Approach to Generalized Transformer Synthesis*, IEEE Trans. Circuits & Systems, 1981, #4, pp. 319-330.

[3] M. Venturini and A. Alesina, *Intrinsic Amplitude Limits and Optimum Design of 9-Switches Direct PWM AC-AC Converters*, Conf. Record IEEE-PESC, 1988, pp. 1284-1291.

[4] L. Gyugyi and B. Pelly, *Static Power Frequency Changers*, Wiley, New York, 1976 (book).

[5] P.D. Ziogas, et al., *Some Improved Forced Commutated Cycloconverter Structures*, Conf. Record IEEE-IAS Annual Meeting, 1984, pp. 739-748.

[6] P.D. Ziogas et al., *Analysis and Design of Forced Commutated Cycloconverter Structures with Improved Transfer Characteristics*, Conf. Record IEEE-PESC 1985, pp. 610-621.

[7] A. Ishiguro et al., *A New Method of PWM Control for Forced Commutated Cycloconverters using Microprocessors*, Conf. Record IEEE-IAS Annual Meeting, 1988, pp. 712-721.

[8] B.H. Khan et al., *A New Simultaneous Gating GTO Dual Converter-Fed D.C. Motor Drive without Circulating Current*, Conf. Record, IEEE-IAS Annual Meeting, 1988, pp. 520-526.