Implementation of a Controlled Rectifier Using AC–AC Matrix Converter Theory

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***Abstract*—It is well known that a PWM-controlled rectifier can offer advantages of reduced low-order harmonics and unity input power factor when compared to a conventional thyristor converter. However, theoretically optimum PWM strategies are often difficult to implement physically or are not easily extended to regenerative operation. This paper proposes an alternative PWM strategy based on ac–ac matrix converter theory, which generates only high-order switching harmonics, presents a unity power factor load to the supply, implicitly extends to regeneration (and operation with a center tapped dc output), and is feasible to physically implement for real-time output voltage control. Both the theory and physical simulation results are presented in the paper.**

I. Introduction

It is well known that a pulse-width modulated (PWM) rectifier (or ac–dc converter) can ideally produce a variable ripple-free dc output current while drawing sinusoidal input current from the supply at unity power. In contrast, a conventional thyristor converter produces substantial output voltage and input current low-order harmonics and operates at a lagging power factor that becomes progressively worse as the output voltage is reduced. Hence, attention is increasingly being directed to modulation strategies that improve the performance of ac–dc rather than dc–ac power converters.

Significant improvements in performance over a conventional thyristor converter can be achieved by using PWM-switched gate turn-off (GTO) bridge [1], which reduces low-order harmonics at the expense of increased high-order components, and provides unity input power factor operation. However, real-time implementation of such PWM switching algorithms can be difficult.

It is also well known that the so-called ac–ac matrix converter is optimal from the point of view of minimum switch number and minimum filtering requirements. The voltage output is a switched PWM pattern based on the constraint of fixed modulation frequency, minimum harmonic distortion output, and a specified fundamental power factor at the input. The power factor at the input is readily adjusted over a range that is limited by the power factor of the output. The modulation strategy that produces these benefits has been derived in rigorous form by Venturini and Alesina [2], [3]. Thus far, however, the benefits of this powerful modulation strategy have not been exploited for other input/output requirements.

This paper proposes to utilize the Venturini switching theory by employing a reduced ac–ac matrix converter as an ac–dc converter. The implementation is achieved by setting the desired output frequency to zero, leaving one output phase unconnected, and allowing dc current to flow through a load connected across the other two phases. The resulting converter draws sinusoidal input current at unity input power factor over the full range of output voltage, generates only high-order switching harmonics, and is easily extended to regenerative or center-tapped operation. Moreover, the switching algorithm is readily implemented in real time using modern microprocessors.

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II. Review of AC–AC Matrix Converters

A three-phase ac–ac matrix converter basically consists of nine bidirectional voltage-blocking current-conducting switches arranged in a matrix so that any input phase can be connected to any output phase at any time (Fig. 1). In principle, for a given set of input three-phase voltages, any desired set of output voltages can then be synthesized by suitably toggling the matrix switches.

The ac–ac matrix topology was first investigated in 1976 [4] and then developed to use a generalized high-frequency switching strategy [2] that reported a limited input to output voltage ratio (0.5). A more recent paper [3] demonstrated how zero-sequence third-harmonic voltage components can be added to the desired ac output voltage to increase the voltage transfer ratio to 0.866. The scheme proposed in [3] also implicitly generates sinusoidal input currents (except for switching harmonics) at unity power factor, independent of the power factor of the output load current.

Other researchers have also investigated the operation of matrix converters using PWM converter and inverter switching strategies [5], [6], but their approaches generally give higher levels of harmonic distortion and/or are difficult to implement in a real-time controller [7]. Furthermore, the input power factor is often not independent of the output power factor in such schemes.

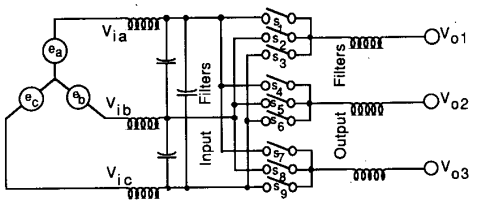


Fig. 1. Structure of three-phase ac-ac matrix converter.

III. Physical Limits on the Operation of a Matrix Converter

For a three-phase matrix converter, the fundamental requirement can be stated as follows. Given a set of three-phase input voltages:

$$[V_i(t)] = \begin{bmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{bmatrix} = \begin{bmatrix} V_i \cos(\omega_i t) \\ V_i \cos(\omega_i t - 2\pi/3) \\ V_i \cos(\omega_i t + 2\pi/3) \end{bmatrix} \quad (1)$$

determine the switching function $M(t)$ that will produce the set of three-phase output voltages

$$[V_o(t)] = \begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{bmatrix} = [M(t)] \cdot \begin{bmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \end{bmatrix}$$

$$= \begin{bmatrix} V_o \cos(\omega_o t + \theta_o) \\ V_o \cos(\omega_o t + \theta_o - 2\pi/3) \\ V_o \cos(\omega_o t + \theta_o + 2\pi/3) \end{bmatrix} \quad (2)$$

where θ_o = arbitrary output voltage phase angle.

Regardless of the switching strategy adopted, there are physical limits on the output voltage achievable with this system as follows. Consider the envelope of the three-phase input voltage set shown in Fig. 2(a). For complete control of the output voltage at any time, the envelope of the target output voltages must be wholly contained within the continuous envelope of these input voltages. This constraint limits the available output voltage to 0.5 of the input voltage. This limit can be improved by adding a third harmonic at the input frequency to all target output voltages. The addition of this third harmonic modulates the available output voltage envelope to follow the maximum possible input voltage continuous region, shown in Fig. 2(b), and hence increases the available output voltage range to 0.75 of the input when the third harmonic has a peak value of $V_{in}/4$. Fig. 2(c) is an alternative presentation of Fig. 2(b), which shows this available output voltage envelope flattened out.

One further improvement in the transfer ratio can be achieved by subtracting a third harmonic at the output frequency from all target output voltages. This minimizes the envelope of the output voltage waveforms to 0.866 of the peak output phase voltage, as shown in Fig. 2(d), when the third harmonic has a peak value of $V_o/6$. Hence the maximum possible voltage transfer ratio becomes

$$V_o/V_{in} = \frac{0.75}{0.866} = 0.866$$

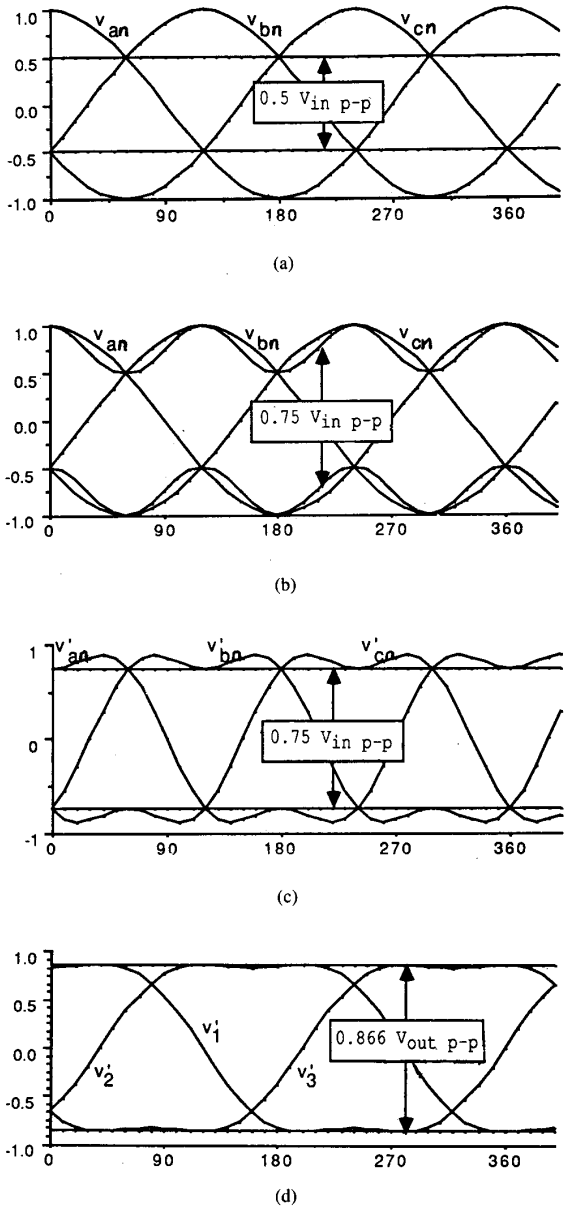


Fig. 2. Physical operating limits for ac-ac matrix converter. (a) Continuous pu input voltage envelope for basic matrix converter. (b) Maximum possible continuous pu input voltage envelope for matrix converter with addition of third harmonic voltage at input frequency. (c) Maximum possible continuous pu input voltage envelope for matrix converter (alternative presentation from output side perspective). (d) Reduction of required pu output voltage envelope by subtraction of third harmonic voltage at output frequency.

and to achieve this maximum possible transfer ratio, the target output voltage becomes

$$[V_o(t)] = \begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \\ V_{o3}(t) \end{bmatrix} = \begin{bmatrix} V_o \cos(\omega_o t + \theta_o) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \\ V_o \cos(\omega_o t + \theta_o - 2\pi/3) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \\ V_o \cos(\omega_o t + \theta_o + 2\pi/3) + \frac{V_i}{4}\cos(3\omega_i t) - \frac{V_o}{6}\cos(3\omega_o t + 3\theta_o) \end{bmatrix}. \quad (3)$$

In 1981, Venturini and Alesina [2] demonstrated how a low-frequency modulation function $[m(t)]$ can be considered equivalent to the switching function $[M(t)]$, provided the switching frequency is high, and input and output low-pass filters are installed on the converter. In 1988 [3], they presented an analytic solution for such a modulating function that achieves the maximum possible output voltage transfer ratio (0.866). This solution is presented in the next section with minor modifications to suit the ac–dc converter application.

IV. Modulation Strategy for an AC–AC Matrix Converter

The problem at hand is to find a low-frequency modulation strategy $[m(t)]$ such that:

$$\begin{aligned} \lceil V_o(t) \rceil &= [m(t)] \cdot \lceil V_i(t) \rceil \\ &= V_o \cdot \begin{bmatrix} \cos(\omega_o t + \theta_o) \\ \cos(\omega_o t + \theta_o - 2\pi/3) \\ \cos(\omega_o t + \theta_o + 2\pi/3) \end{bmatrix} + \frac{V_o}{2\sqrt{3}} \cdot \begin{bmatrix} \cos(3\omega_i t) \\ \cos(3\omega_i t) \\ \cos(3\omega_i t) \end{bmatrix} - \frac{V_o}{6} \cdot \begin{bmatrix} \cos(3\omega_o t + 3\theta_o) \\ \cos(3\omega_o t + 3\theta_o) \\ \cos(3\omega_o t + 3\theta_o) \end{bmatrix} \\ &= \quad [A] \quad + \quad [B] \quad + \quad [C] \end{aligned} \quad (4)$$

where $[V_i(t)]$ is defined by (1), and the elements of $[m(t)]$ are limited by the existence constraint

$$0 \le m_{ij} \le 1 \quad \text{for} \quad 1 \le i \le 3 \quad 1 \le j \le 3 \quad (5)$$

and the current continuity constraint

$$\sum_{j=1}^{3} m_{ij} = 1 \quad \text{for} \quad 1 \le i \le 3 \quad (6)$$

Note that the scale factor for the [B] output voltage set has been changed to enable the analytic solution to be determined. This does not affect the output voltage waveform, since the new scale factor equals $V_i/4$ at the maximum transfer ratio of 0.866.

Consider the partial output voltage set [A] in (4). This voltage set can be obtained by multiplying the input voltage either by a positive sequence set of $(\omega_o + \omega_i)$ sinusoids or by a negative sequence set of $(\omega_o - \omega_i)$ sinusoids, as follows:

$$[m]_A = \frac{\beta_1}{3} \cdot \begin{bmatrix} m_+(1) & m_+(2) & m_+(3) \\ m_+(2) & m_+(3) & m_+(1) \\ m_+(3) & m_+(1) & m_+(2) \end{bmatrix} + \frac{\beta_2}{3} \cdot \begin{bmatrix} m_-(1) & m_-(3) & m_-(2) \\ m_-(2) & m_-(1) & m_-(3) \\ m_-(3) & m_-(2) & m_-(1) \end{bmatrix} \quad (7)$$

where

$$m_+(i) = \cos[(\omega_o + \omega_i)t + \theta_o - (i-1)2\pi/3]$$
$$m_-(i) = \cos[(\omega_o - \omega_i)t + \theta_o - (i-1)2\pi/3].$$

Balance of power considerations through the converter give

$$\beta_1 = \frac{V_o}{V_i}\left(1 - \frac{\tan(\text{input pf angle})}{\tan(\text{output pf angle})}\right)$$
$$\beta_2 = \frac{V_o}{V_i}\left(1 + \frac{\tan(\text{input pf angle})}{\tan(\text{output pf angle})}\right). \quad (8)$$

A similar approach for partial output voltage sets [B] and [C] yields

$$[m]_B = \frac{\gamma_1}{3}\begin{bmatrix} n_+(1) & n_+(2) & n_+(3) \\ n_+(1) & n_+(2) & n_+(3) \\ n_+(1) & n_+(2) & n_+(3) \end{bmatrix} + \frac{\gamma_2}{3}\begin{bmatrix} n_-(1) & n_-(3) & n_-(2) \\ n_-(1) & n_-(3) & n_-(2) \\ n_-(1) & n_-(3) & n_-(2) \end{bmatrix} \quad (9)$$

where

$$n_+(i) = \cos\,[4\omega_i t - (i-1)2\pi/3]$$

$$n_-(i) = \cos\,[2\omega_i t - (i-1)2\pi/3]$$

$$\gamma_1 + \gamma_2 = \frac{1}{\sqrt{3}} \cdot \frac{V_o}{V_i}$$

$$[m]_C = \frac{\delta_1}{3}\begin{bmatrix} q_+(1) & q_+(2) & q_+(3) \\ q_+(1) & q_+(2) & q_+(3) \\ q_+(1) & q_+(2) & q_+(3) \end{bmatrix} + \frac{\delta_2}{3}\begin{bmatrix} q_-(1) & q_-(3) & q_-(2) \\ q_-(1) & q_-(3) & q_-(2) \\ q_-(1) & q_-(3) & q_-(2) \end{bmatrix} \quad (10)$$

where

$$q_+(i) = \cos\,[(3\omega_o + \omega_i)t + 3\theta_o - (i-1)2\pi/3],$$

$$q_-(i) = \cos\,[(3\omega_o - \omega_i)t + 3\theta_o - (i-1)2\pi/3]$$

$$i = 1, 2, 3$$

$$\delta_1 + \delta_2 = -\frac{1}{3} \cdot \frac{V_o}{V_i}.$$

To satisfy the current continuity constraints, (6), a 3×1 identity matrix is added to $[m(t)]$, to make the complete solution:

$$[m(t)] = \tfrac{1}{3}[I] + [m]_A + [m]_B + [m]_C. \quad (11)$$

The coefficients γ_1, γ_2, δ_1, and δ_2 are chosen to maximize the transfer ratio V_o/V_i without violating the existence constraint (5), and are found to be

$$\gamma_1 = -\frac{1}{6\sqrt{3}} \cdot \frac{V_o}{V_i} \qquad \gamma_2 = \frac{7}{6\sqrt{3}} \cdot \frac{V_o}{V_i}$$

$$\delta_1 = -\frac{1}{6} \cdot \frac{V_o}{V_i} \qquad \delta_2 = -\frac{1}{6} \cdot \frac{V_o}{V_i}. \quad (12)$$

For each switching period, the modulation strategy then becomes:

1) Calculate the scale coefficients β_1, β_2, γ_1, γ_2, δ_1, and δ_2 for the required V_o/V_i ratio.
2) Calculate the modulation function sinusoidal values for the present time instance (typically from a look-up table).
3) Calculate the composite modulation function values $[m(t)]$.
4) Arrange to turn on switches 1–9 for the period $t_i = m_i(t)\,\Delta t$.

V. Reduction of a Matrix Converter to a Controlled AC/DC Rectifier

To operate a matrix converter as an ac–dc rectifier, the output frequency ω_o is set to zero, and the output voltage phase angle θ_o is set to 30°. This sets the output phases

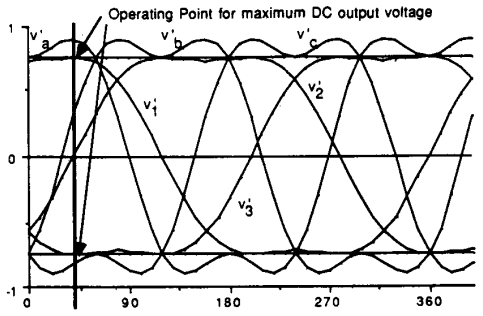


Fig. 3. Operation of a matrix converter as a dc rectifier.

to maximum, minimum, and zero voltage, respectively, as shown in Fig. 3. A maximum dc voltage of $1.5 \times V_{\text{in}}$(peak) is then achievable between the two extreme phases (if the ac output voltage magnitude is set to 0.866 of V_{in}), whereas the third phase is available as a zero-voltage center tap terminal. Mathematically, the reduction causes the target output voltage $[V_o(t)]$ to reduce to

$$[V_o(t)] = \begin{bmatrix} V_o \cdot \cos 30° + \dfrac{V_o}{2\sqrt{3}} \cdot \cos(3\omega_i t) \\ \text{zero} + \dfrac{V_o}{2\sqrt{3}} \cdot \cos(3\omega_i t) \\ -V_o \cdot \cos 30° + \dfrac{V_o}{2\sqrt{3}} \cdot \cos(3\omega_i t) \end{bmatrix} \quad (13)$$

and the matrix converter modulation function $[m(t)]$ reduces to

$$[m(t)] = \begin{bmatrix} m_{11}(t) & m_{12}(t) & 1 - m_{11}(t) - m_{12}(t) \\ m_{21}(t) & m_{22}(t) & 1 - m_{21}(t) - m_{22}(t) \\ m_{31}(t) & m_{32}(t) & 1 - m_{31}(t) - m_{32}(t) \end{bmatrix} \quad (14)$$

where

$$m_{11}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{\frac{1}{2}\cos(\omega_i t) + \frac{7}{36}\cos(2\omega_i t) - \frac{1}{36}\cos(4\omega_i t)\right\} + \frac{1}{3}$$

$$m_{12}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{\frac{1}{2}\cos(\omega_i t - 2\pi/3) + \frac{7}{36}\cos(2\omega_i t + 2\pi/3) - \frac{1}{36}\cos(4\omega_i t - 2\pi/3)\right\} + \frac{1}{3}$$

$$m_{21}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{\text{zero} + \frac{7}{36}\cos(2\omega_i t) - \frac{1}{36}\cos(4\omega_i t)\right\} + \frac{1}{3}$$

$$m_{22}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{ \text{zero} + \frac{7}{36} \cos(2\omega_i t + 2\pi/3) - \frac{1}{36} \cos(4\omega_i t - 2\pi/3) \right\} + \frac{1}{3}$$

$$m_{31}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{ -\frac{1}{2} \cos(\omega_i t) + \frac{7}{36} \cos(2\omega_i t) - \frac{1}{36} \cos(4\omega_i t) \right\} + \frac{1}{3}$$

$$m_{32}(t) = \frac{2}{\sqrt{3}} \cdot \frac{V_o}{V_i} \cdot \left\{ -\frac{1}{2} \cos(\omega_i t - 2\pi/3) + \frac{7}{36} \cos(2\omega_i t + 2\pi/3) - \frac{1}{36} \cos(4\omega_i t - 2\pi/3) \right\} + \frac{1}{3} \quad (15)$$

under the simplifications of ω_i, θ_i equal to zero, θ_o equal to 30°, unity input power factor, calculate only $m_{11}(t)$, $m_{12}(t)$, $m_{21}(t)$, $m_{22}(t)$, $m_{31}(t)$, $m_{32}(t)$ because of current continuity constraints.

The six expressions in (15) define the fractional on-time of the six switches S_1, S_2, S_4, S_5, S_7, S_8 in the matrix bridge shown in Fig. 1, leaving switches S_3, S_6, and S_9 to conduct for the remainder of each switching period Δt. These expressions each require one table lookup, one multiplication, and one addition for their computation, and this can readily be achieved within one switching cycle using a microprocessor with a hardware multiply facility. The summed cosine expressions can be stored to any desired degree of accuracy, without undue microprocessor memory requirements (e.g., table storage to 0.5° accuracy would require less than 5 kilobytes of EPROM), and even only an 8-b multiply would allow for 0.5% changes in modulation depth. Hence, the new algorithm allows for very fine control of the bridge modulation and hence output voltage. Furthermore, as discussed in Section VI, for some topological variations of the reduced converter, switches S_4, S_5, and S_6 need not be physically implemented, and hence the modulation expressions $m_{21}(t)$ and $m_{22}(t)$ need not be computed. This further reduces the computational load on the controlling microprocessor.

VI. Topological Variations of the Reduced Matrix Converter Operating as an AC–DC Rectifier

The implementation of a full ac–ac matrix converter requires 9 bidirectional switches as shown in Fig. 1. Because no generic bidirectional switches are available as yet, this converter can be implemented using 18 unidirectional switches (every two switches are connected back to back to make one bidirectional switch). However, for the controlled rectifier implementation, the number of unidirectional switches required can be substantially reduced as follows:

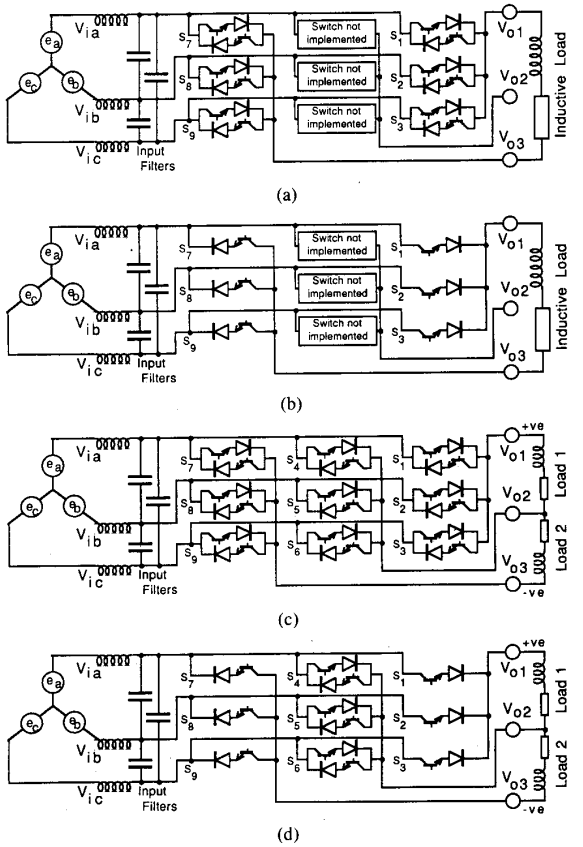


Fig. 4. Alternative topologies for an ac–dc matrix converter. (a) Single-ended, bidirectional ac–dc matrix converter. (b) Single-Ended, unidirectional ac–dc matrix converter. (c) Dual supply, bidirectional ac–dc matrix converter. (d) Dual supply, unidirectional ac–dc matrix converter.

1) For a single-ended dc output, the load impedance is connected between the two extreme phases (Fig. 4(a)), and the three bidirectional switches of the zero-voltage phase need not be physically implemented as they do not carry current. Output voltage control is achieved by modulating the target output voltage magnitude (V_o) between V and 0.866 V_{in}.

This configuration will support load regeneration implicity, as the remaining 6 switches are bidirectional, and hence it has potential as a regenerative dc motor drive. Such drives are conventionally implemented using a separate forward and reverse semiconductor-controlled rectifier (SCR) or PWM bridge [8] and usually require either deadtime or careful bridge-firing control to cross over from motoring to regeneration. The matrix converter requires no such consideration as bidirectional current flow is implicit within the modulation algorithm. Effectively, the modulation controller chooses to reverse the load power factor by changing the dc output voltage, and the bridge follows within one switching cycle (ignoring inductive transients

caused by reversing impulse currents, which must be snubbed).

The matrix converter requires 12 unidirectional switches to implement the 6 bidirectional switches that are required, but this is no worse than the 12 unidirectional switches required by the conventional dual-bridge approach and has the advantage of implicit regenerative crossover without the need for dead time.

2) For a single-ended dc output with no regenerative capability, the 6 bidirectional switches of 1) can be made unidirectional as they now only conduct current in one direction (Fig. 4(b)). In this configuration, the converter has the same topology as a standard PWM-controller rectifier and uses the same number of switches. No freewheeling diodes are required to carry the inductive load current, as the Venturini algorithm implicitly creates a continuous load current path as a condition of its solution. This topology also has the advantage of being able to generate a positive or a negative output voltage simply by a modulation change (i.e., add 180° to the output voltage arbitrary phase angle).
3) The converter also can be used to create a dual-center tapped dc supply with regenerative capability on both the positive and negative supply. This realization has particular interest for reluctance motor drives, and, to the author's knowledge, cannot be achieved by any other single-bridge topology. To operate in this mode, load impedances are connected between the zero-voltage third phase and the two extreme voltage phases (Fig. 4(c)).

   The load impedances need not be balanced, as the resulting dc load currents can be viewed as a time snapshot of an ac load with nonunity power factor. Hence the load currents are simply out of phase with the load voltage. Because the Venturini algorithm decouples the input and the output power factor of the converter, the supply input currents remain sinusoidal at unity power factor regardless of the state of the output load currents.

   This implementation requires the complete set of 9 bidirectional switches, but offers a capability that cannot be matched by any other single-bridge topology.
4) Some reduction in number of switches in 3) can be achieved by operating the converter as a dual center tapped dc supply without regenerative capability. In this case, the upper phase switches can be made unidirectional in the forward direction, and the lower phase switches can be made unidirectional in the reverse direction (Fig. 4(d)). However, bidirectional switches are still required for the zero voltage phase to conduct the difference between the positive and negative phase currents under unbalanced load conditions. Hence, 12 switches are still required to implement the converter—the same number as would be required to implement two conventional SCR or PWM bridges side by side. However, the matrix converter implementation offers the advantage of implicit tracking of the positive and the negative supplies, controlled by one modulating system.

VII. Simulation Results

The converter has been extensively investigated in simulation, both theoretically and as a simulated physical implementation. The theoretical simulation assumes infinite switching frequency and was used to confirm the equivalent low-frequency transfer function developed in [4] to [15] earlier. The physical simulation represents the converter as a set of ideal bidirectional switches coupled into differential equations, which represent the load impedance, source impedance, and filter elements as physical resistances, inductances, and capacitors. The switching algorithm is implemented as discrete time-step switch transitions that cause discontinuities to these differential equations (exactly as the real physical converter would be switched). This physical simulation has been used to confirm the converter operation in detail under a variety of operating conditions, including different switching frequencies, single and dual dc supply configurations, and a variety of load types. In particular, this simulation has been used to confirm the specific current flow through each simulated bidirectional switch under various operating conditions.

Results are presented in Figs. 5–10 to illustrate the operation of the new converter in a number of configurations. In all cases, the switching rate is set to 5 kHz. The switched voltage and current waveforms are smoothed for display purposes by a low-pass *RC* filter set to 1 kHz, and the *RL* load has a natural time constant of 3.3 ms.

Fig. 5 shows the operation of the converter acting as a single-quadrant rectifier, with the step change in output voltage from $m = 0.866$ to $m = 0.433$ occurring at $t = 30$ ms. The input power factor seen by the supply is clearly unity, with no low-order harmonics present within the ac line current.

Figs. 6 and 7 show the raw switched dc output voltage and ac input current, respectively, (time and frequency domain for each). As predicted by theory, the only significant harmonic components are centered around the switching frequency with virtually no low-order harmonics.

Fig. 8 shows the simulated supply input current drawn by the converter through the input *LC* filter (time and frequency domain). The input *LC* filter has a natural resonant frequency of 1.5 kHz, and partly uses the source impedance of the ac voltage supply, as this cannot be determined in practice. The high-order switching harmonics have been eliminated by the input filter, leaving only a unity power factor sinusoidal input current. It should be noted that the initial deviation of the input current waveform from sinusoidal is due to the initial condition perturbation of the simulation.

Fig. 9(a) shows the converter operating as a four-quad-

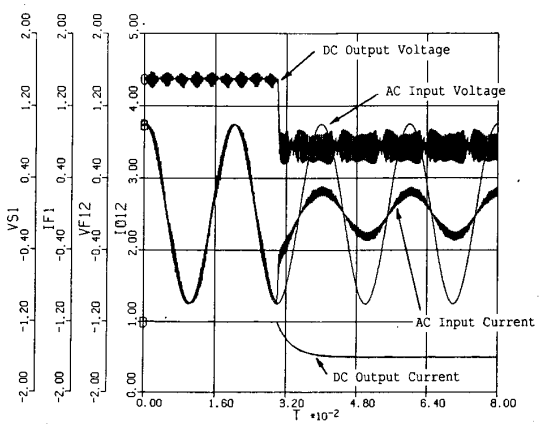
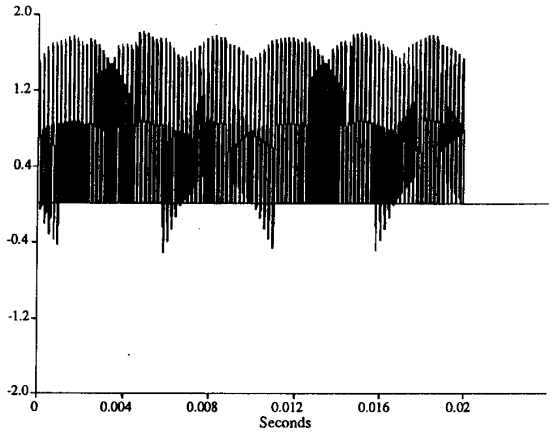
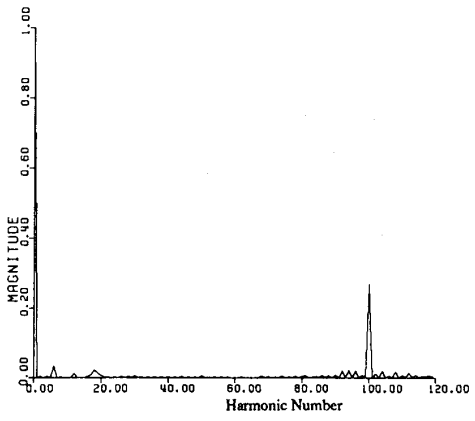


Fig. 5. Single-quadrant operation of the ac–dc converter (time domain).

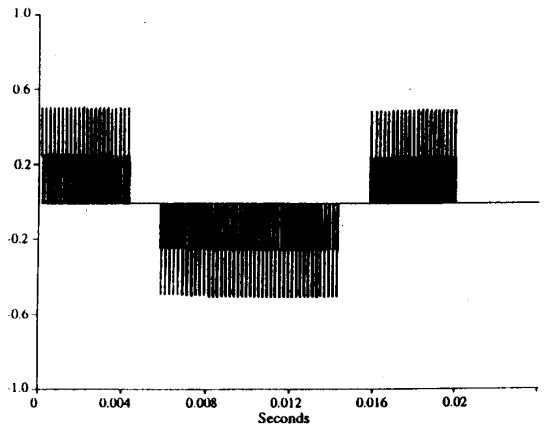


(a)

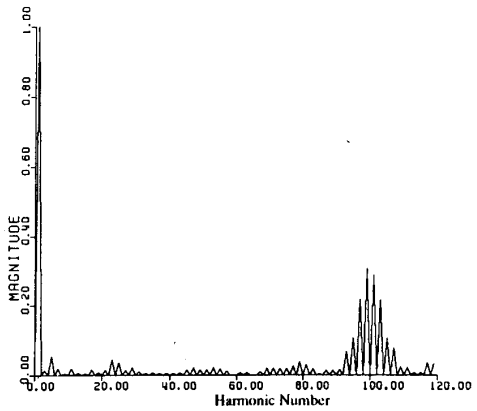


(b)

Fig. 6. Converter dc output voltage. (a) Time domain. (b) Frequency spectrum.



(a)



(b)

Fig. 7. Converter ac input current. (a) Time domain. (b) Frequency spectrum.

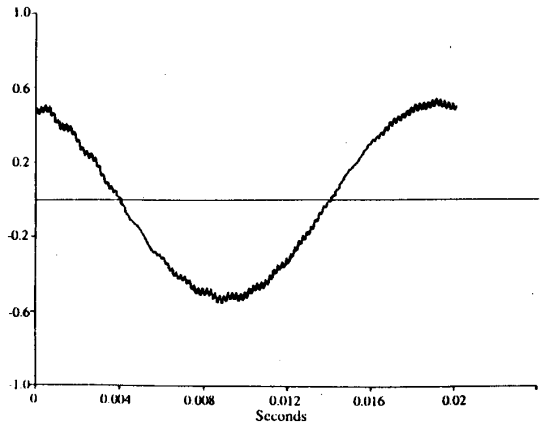


Fig. 8. AC line input current to the converter (time domain).

rant regenerating rectifier, feeding into a passive *RL* load. When the output voltage reverses polarity in a step change, the bridge briefly regenerates until the output current through load inductor reverses also. Fig. 9(b) shows the regenerating rectifier feeding a dc motor load. When the dc output voltage steps from greater than to less than the dc motor back emf voltage, the dc motor current reverses sign with the time constant of the motor armature winding. The ac line current also reverses sign to become regenerative at unity power factor as predicted by theory.

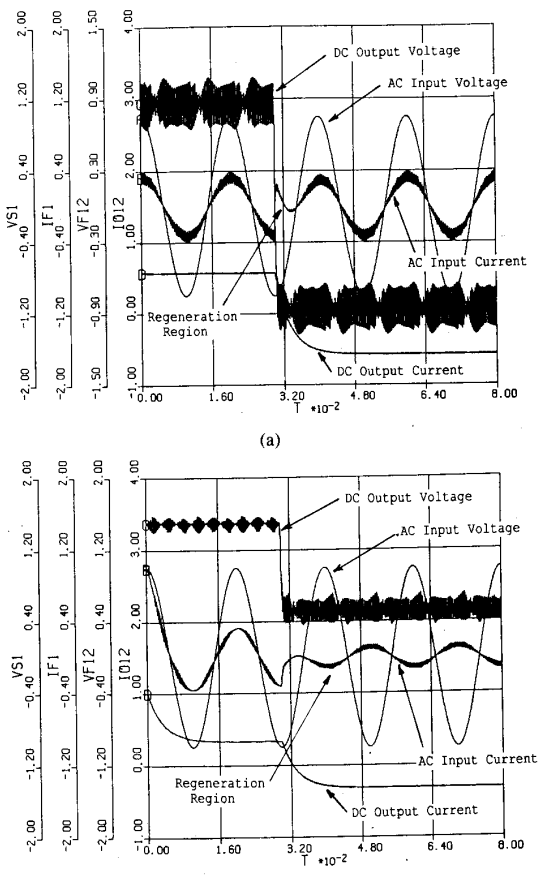


Fig. 9. Four-quadrant regenerative operation of the converter. (a) Resistive-inductive load (time domain). (b) DC motor load (time domain).

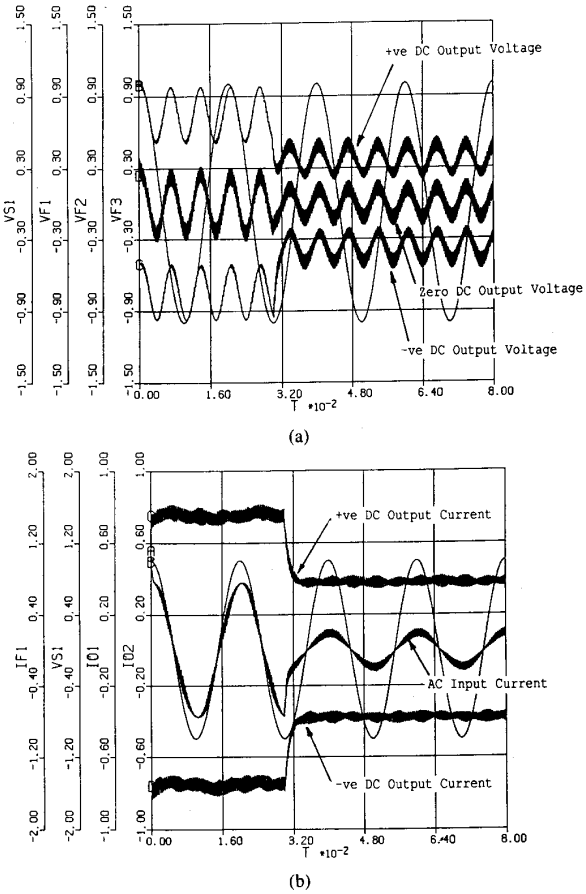


Fig. 10. Dual supply operation of the converter. (a) DC output voltages (time domain). (b) AC input and dc output currents (time domain).

Fig. 10 shows the operation of the converter as a dual supply dc rectifier. Fig. 10(a) shows the positive, negative, and zero-output voltages as a step change occurs. Note the common mode input voltage third harmonic, which is present on all output terminals to achieve the maximum possible voltage transfer ratio. Fig. 10(b) illustrates the dc output currents under dual supply operation and again illustrates that the converter presents a unity power factor load to the incoming ac supply.

A variety of other operating conditions have also been simulated, and in all cases the converter operated as predicted by theory. Of particular note is the fact that the frequency of the harmonic components produced by the converter does not vary significantly with changes in output voltage, in contrast to other PWM switching strategies. Hence the input filters can be matched to a small frequency range of high-order input harmonics without having to be detuned to trap a wider range of input harmonics that vary as the modulation ratio changes.

VIII. Physical Implementation of the New Converter

The previous sections of this paper presented the theoretical foundations for the new converter modulation algorithm and showed by physical simulation, that the converter will operate as predicted. However, two final issues must be considered if the converter is to be implemented in practice. First, it must be confirmed that the computational demands of the modulation strategy can be executed in real time within one switching cycle. Second, the switching of the bidirectional switches, which are made up from reverse paralleled unidirectional switches, must be considered carefully to avoid possible bridge leg shoot-through failure. Both these issues will be considered.

A. Computational Requirements

Equation (15) shows that the computational requirements for the full converter implementation consist of the calculation of some six modulation expressions. Each calculation requires:

1) A table lookup, using time as an index variable to extract a composite sinusoidal sum (all three sinusoidal terms can be lumped together) from a stored data table. As noted before, storage of six tables, to say 0.5° degree accuracy is not at all difficult. A typical microprocessor could execute this procedure in say 10 μs.

2) A single multiplication sinusoidal sum and the scaled modulation ratio. The modulation ratio can be scaled so that the result of the multiplication is a number of clock counts that can be directly fed into the hardware output timers of the controller. A typical microprocessor with hardware multiply facility could execute this procedure in say 20 μs, allowing for the housekeeping of loading the input registers and saving this result.
3) A single addition to add in the final one-third offset. Typically, this would add 5 μs computation time for each addition.

The overall computation time for each expression is therefore 10 + 20 + 5 μs = 35 μs, but say 50 μs to allow for software overhead. To compute six such expressions would therefore require 300 μs leaving 200 μs available to manage other tasks such as loading the output timers, etc., for a 2-kHz switching rate.

This analysis has been verified using a 9-MHz 8-b microprocessor and six channels of hardware counter/timers to generate the switching signals required for the single-ended unidirectional controlled rectifier (Fig. 4(b)). For this implementation, only four modulation expressions needed to be calculated, and this was easily done within 300 μs, including all software housekeeping required to load the hardware counter/timers. (The output of these counter/timers directly control the bridge switching elements.)

B. Switching Requirements for Bidirectional Switching Elements

A fundamental constraint for the new algorithm (and indeed for matrix converters in general) is that output current continuity is maintained at all times. To achieve this, as each switch in the bridge turns off, the next switch in sequence must immediately turn on. In practice, if the switches are bidirectional, there will generally be a brief input short circuit as the switches cross over, and this is potentially hazardous. For example, as switch S_1 turns off, switch S_2 turns on, and a momentary short circuit develops between input phases a and b. Although it is possible to minimize the effects of this short circuit by extremely careful switch timing, a more robust approach is to be preferred.

One solution to the problem is to stagger the switching of the forward and the reverse conduction elements of the incoming and the outgoing bidirectional switch elements to avoid the short circuit condition. The approach presented here is adapted from other researchers [9], [10], and has been extended to suit the general case of a three-phase to three-phase matrix converter.

Conceptually, the proposed switch crossover process can be viewed as turning on the appropriate switch element in the incoming bidirectional switch early to act as a short-term antiparallel diode and delaying the incoming switch element that could cause a momentary shortcircuit until the outgoing bidirectional switch is fully off. Unfortunately, the required switching sequence differs depending on the direction of current flow through the bridge leg before the crossover commences. Fig. 11 identifies the current-carrying devices for the two cases of load current flowing in the forward and in the reverse direction through the bridge. The required switching sequences for these devices are summarized as follows:

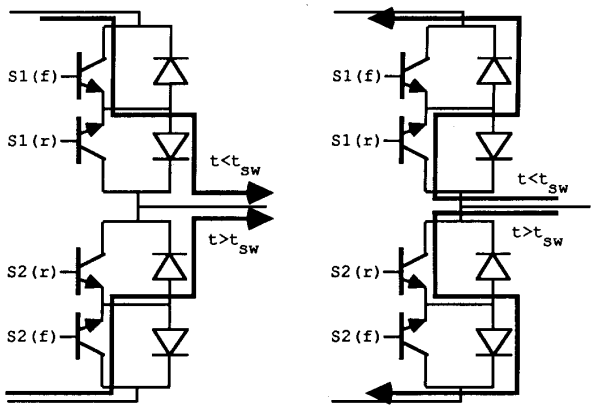


Fig. 11. Forward and reverse current carrying switch elements in a bidirectional switch. (a) Current in forward direction. (b) Current in reverse direction.

1) *For a forward current flowing through switch S1(f)*
Turn off Switch $S_1(r)$ and wait until fully off (t_1).
Turn on switch $S_2(f)$ and wait until fully on (t_2).
Turn off switch $S_1(f)$ and wait until fully off (t_3).
Turn on switch $S_2(r)$.
2) *For a reverse current flowing through switch S1(r)*
Turn off switch $S_1(f)$ and wait until fully off (t_1).
Turn on switch $S_2(r)$ and wait until fully on (t_2).
Turn off switch $S_1(r)$ and wait until fully off (t_3).
Turn on switch $S_2(f)$.

These switch sequences are independent of the applied input voltage across the bridge, assuming an inductive load to maintain the load current during the crossover. Hence, the sequences for switching from the lower half of the bridge leg to the upper half are mirror images of the above. Also, for some type of switches, delays t_1 and t_2 may be trivial.

One possible difficulty with the staggered switching concept is that the load current may reverse during the commutation process (e.g., when changing to regeneration after a change in the output voltage). However, under these conditions, the load current will settle at zero until the switching sequence completes, as the reverse current path through the incoming switch is established last. The error introduced because of this discontinuity in load current is trivial.

The complete ac–ac matrix converter has nine bidirectional switches, of which three sets of three switches must be sequenced together. This makes the staggered switching sequence more complex, as there are two possible incoming bridge switches for each outgoing switch. Fig. 12 shows the circuit arrangement for one phase of a matrix

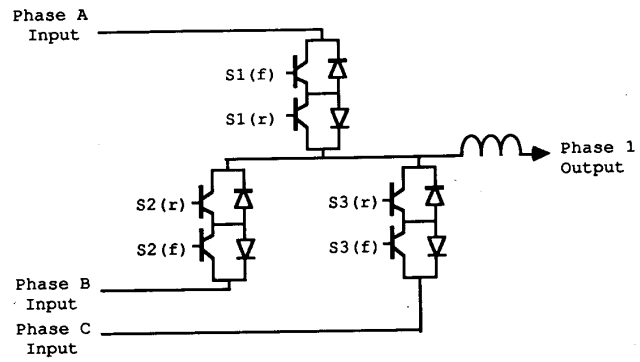


Fig. 12. Bidirectional switch arrangement of a matrix converter (one phase leg only).

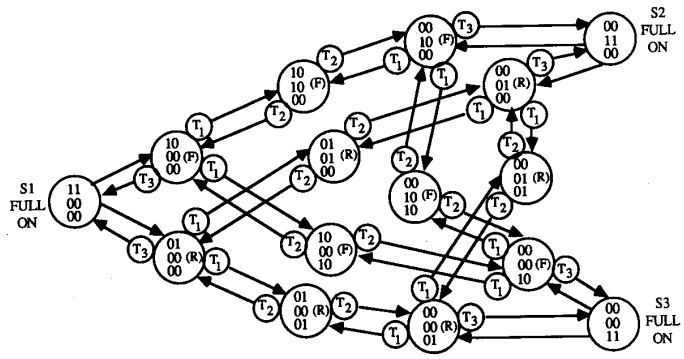


Fig. 13. Bidirectional switching sequence for one phase leg of a matrix converter.

converter (three bidirectional switches), and Fig. 13 shows the required crossover sequence logic as a constrained state diagram (the constraint is that state propagation must complete to a state of one composite switch fully on before another state transition sequence can be initiated). This logic is presently being implemented as a clocked state machine, using programmable logic chips, and will be reported as part of a future paper. To date, the staggered switching concept has been successfully verified experimentally for a two-switch bridge leg using back-to-back bipolar transistors.

IX. Conclusions

Controlled rectifiers using PWM switching strategies are currently attracting considerable interest because of their ability to minimize low-order harmonics and to present unity power factor loads to the ac supply. However, many of the modulation techniques proposed are difficult to implement on-line, or do not extend to regeneration or center tapped operation. These limitations can be overcome by using ac–ac matrix converter theory, without any additional hardware penalty.

There are four main benefits of the proposed modulation stragegy:

1) The algorithm is readily implemented in real time, unlike most other optimal PWM strategies.
2) The input current is implicitly sinusoidal with unity power factor (except for high-order switching harmonics).
3) Regenerative operation is implicit by constructing the converter using bidirectional switches (no dead time going from forward to reverse power flow).
4) Operation as a center-tapped dc supply, with regeneration, is also implicit and is easily implemented with three additional bidirectional switches.

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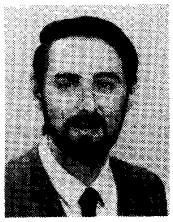

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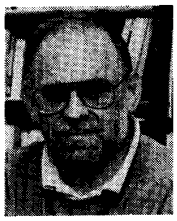

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