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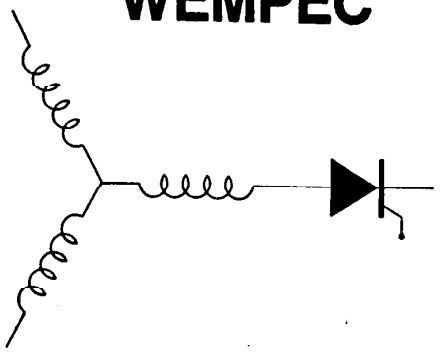

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ABSTRACT

The matrix converter Prof. Venturini proposed is very simple in structure and has powerful controllability. But, there are few applications especially in power electronics fields. This seems being mainly caused by the fact that we didn't have such power devices that were fast enough to suppress ringing oscillations in the supply lines and big enough to pay for more devices and more complicated control circuits than in conventional DC-link converter-inverter systems.

Now we've static induction thyristors(SITs) and a new possibility for the matrix converter is opened for us. This paper proposes a new control strategy which is more simple and allows to generate the output voltage of 0.866 times the supply voltage. This paper also discuss about how to eliminate voltage and current spikes inevitable in normal switching operations. The system operation is examined and confirmed by experiments.

1. INTRODUCTION

The matrix converter proposed by Prof. Venturini [1][2] is very simple in structure and is characterized as follow;

(a) A large capacity and compact converter system can be designed because the system doesn't have any DC-link circuit and, as a result, doesn't need any energy storage componen such as a smoothing inductor or a smoothing capacitor.
(b)The system has high efficiency, because the number of devices connected in series is less in this system than in the conventional rectifier-inverter system.
(c) Four-quadrant operation is very easy. What is more, by controlling switching patterns appropriately, both of output voltages and input currents become sinusoidal.

Many theoretical studies have been done on the matrix converter mainly in Europe [3][4], but there are few practical applications especially in power electronics fields. One of the reasons is that we didn't have suitable power switching devices. The matrix converter demands large-power , high-speed switching devices with bi-directional voltage blocking ability and self-turn off capability. Higher speed switching devices are desirable because the size of the input filters decreases with increased carrier frequency. The second reason is that the switches are subjected to current spikes and voltage spikes during commutation interval. The spikes increase as the current increases and the inductance of the load increases and eventually destroy the devices. The third reason is that the high voltage devices with the blocking voltage ability of 2 2 times the output voltage are required, since the output voltage is limited to 0.5 times the supply voltage under the control method proposed by Prof. Venturini.

This paper proposes a new control strategy for the matrix converter which allows to generate the output voltage of 0.866 times the supply voltage. This paper also discuss about how to eliminate voltage and current spikes in the commutation. The system operation is examined and confirmed by experiments using the matrix converter with anti-parallel-connected SITs.

2. CONTROL STRATEGY FOR VOLTAGE-SOURCE MATRIX CONVERTER

2.1 Circuit Diagram of Matrix Converter

The circuit diagram of a matrix converter is illustrated in Fig. 1. In the figure S_a, S_b, S_c are bi-directional switches and, in our project, anti-parallel-connected SITs are used. SITs switch the circuit at the switching frequency from 5 to 10kHz. Inductances L_1 and capacitors C_1 are for filtering the carrier frequency components. Each of switches in the matrix converter is PWM controlled by both of output voltage commands v_a^*, v_b^*, v_c^* and three phase supply voltages e_u, e_v, e_w.

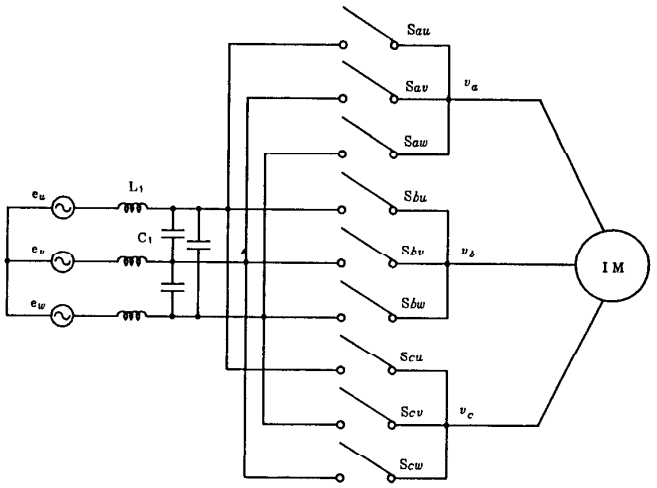


Fig. 1 Circuit diagram.

2.2 Novel Control Strategy for Matrix Converter

Prof. Venturini proposed to control the output voltage v of the converter according to the following equation.

$$v=(T_U/T)e_U+(T_V/T)e_V+(T_W/T)e_W \quad (1)$$

Where, T: a period of the carrier, T_U, T_V, T_W: time intervals in which the output terminals are connected to the phase-u, v, w, respectively, during one period of the carrier.

The output voltage depends on the supply phase voltage during the period of the carrier. The maximum value of the output voltage is therefore the half of the supply voltage, as shown in Fig. 2.

Fig. 3 and Fig. 4 explain the proposed new control strategy of the matrix converter. Fig. 3 shows a wave form of the output voltage commands and how switches are controlled according to the commands. The switches in the phase with the lowest command are always controlled to connect the output terminal to the lowest supply voltage e_{min}. The switches in another two phases are switched between the highest voltage e_{max} and the lowest voltage e_{min} of the three phase power supply and PWM controlled by output voltage command.

Here,
e_{max} = MAX [e_U, e_V, e_W]
e_{min} = MI N [e_U, e_V, e_W]

Fig. 4 shows the switching pattern for switch groups S_b and S_c during interval I. Switches in the S_c group are controlled such that the phase c terminal of the load is always connected to the lowest voltage e_{min}. The switching pattern of the S_b group is decided by the cross points between the output voltage command V_{bc}* and the triangular wave form signal whose amplitude is equal to the maximum value of the supply line voltage, e_{max} e_{min}.

With the proposed control strategy, the maximum value of the output line voltage is equal to the minimum of the e_{max} e_{min}. The output voltage is hence 0.866 times the supply voltage.

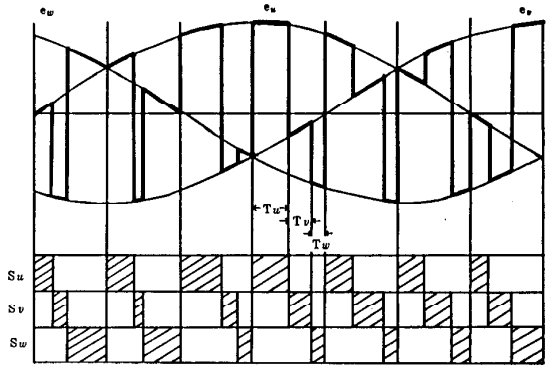


Fig. 2 Switching pattern under Venturini's method.

Prof. Venturini shows that not only the output voltages but also input currents can be controlled to be sinusoidal by selecting proper intervals T_U, T_V, T_W in the equation (1). The input currents i_U, i_V, i_W are given by,

$$i_U=(T_U/T)i,\ i_V=(T_V/T)i,\ i_W=(T_W/T)i \qquad (2)$$

Where, i: the output current.

In this paper, we only use e_{max} and e_{min} for voltage control. But, we've another freedom in controlling switching patterns. By making use of the other phase voltages and controlling switching patterns appropriately, we can control input current wave form and, as a result, the power factor of the system.

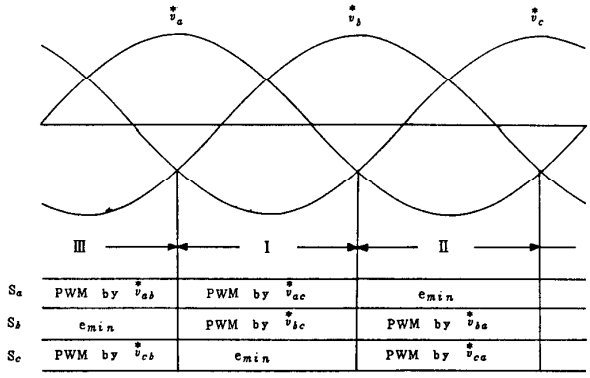


Fig. 3 Control strategy.

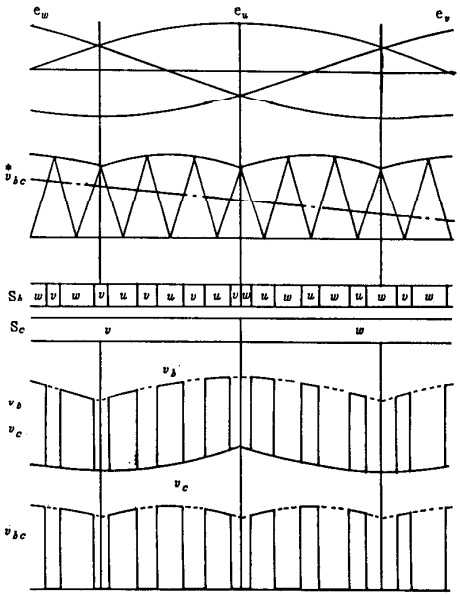


Fig. 4 SIT switching pattern.

3.EXPERIMENTAL CIRCUIT OF MATRIX CONVERTERS

3.1 SI Thyristors

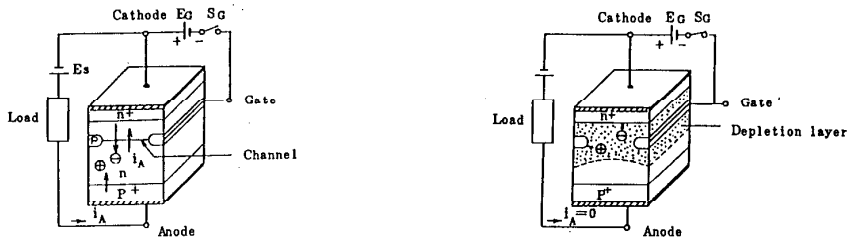
Fig. 5 shows the cross-sectional structure and functional principle of SIT [5].

When a reverse bias voltage is applied between gate and cathode as shown in Fig. 5(b), depletion layer containing no carriers grows up around the channels, and blocks the forward voltage between anode and cathode.

The removal of this reverse voltage causes the depletion larger around the channel disappear and current starts to flow through the channels like a diode, as shown in Fig. 5(a). This means that the turn-on mechanism of SIT differs from the conventional thyristors and current can sharply rise. A slight positive gate voltage should be applied to the gate to shorten the turn-on period.

By a reverse bias voltage applied between a gate and cathode, the carriers inside the n-layer are swept out to the gate and cathode electrodes, causing depletion layer to be produced around the channels. The cathode current attenuates accordingly and the thyristor is switched over to the forward blocking state. The few carriers remaining inside the n-type layer flows out to the gate electrode as a tailing current.

Table 1 shows characteristics of the SITs which have been developed up to now.



(a) ON state.

(b) OFF state.

Fig. 5 Schematic view of SIT.

Table 1 Characteristics of the SIT

Item	Symbol	Unit	Value	Condition
Off voltage	V_{DRM}	V	1200	
On current	I_{TRMS}	A	300	
Peak turn-off current	I_{TGQ}	A	> 800	V_D=600V C_s =1μF
On current rising ratio	di/dt	A/μs	> 900	V_D=800V I_{FGP}=5A
Off voltage rising ratio	dv/dt	V/μs	>2000	
Gate reverse voltage	V_{RGM}	V	160	
On voltage	V_{TM}	V	2.7	I_T =300A
Turn-on time	t_{gt}	μs	2	I_T =600A
Turn-off time	t_{gq}	μs	2	I_T =600A

3.2 Firing sequence of the SITs

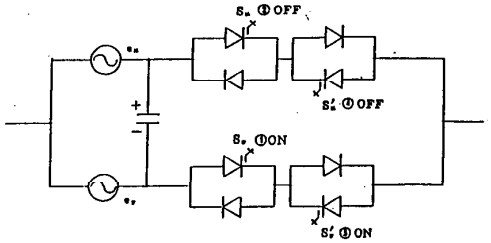
Switches S_{au}, S_{bu},...,S_{cw} in Fig.1 are bi-directional and the SITs are adopted in our project.

A diode is connected anti-parallelly with each SIT as shown in Fig.6, since the SITs on the market is without a reverse voltage blocking ability.

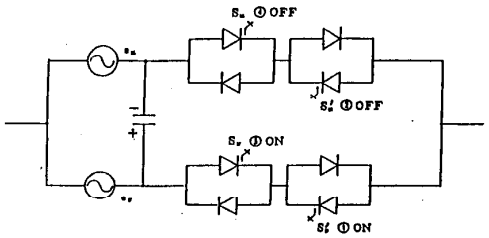
Fig. 6 illustrates the firing sequence when the commutation from phase-u to phase-v is made. In order to protect the cut of the load circuit, as well as the short circuit of the supply, it's necessary to change the firing sequence according to the polarity of the source voltage.

(i) When $e_u > e_v$ [see Fig. 6(a)]
- (1) Turn on S_v
  But, S_v doesn't conduct because it's reverse biased.
- (2) Turn off S_u
  The current flowing S_u is switched to S_v.
- (3) Turn on S_v'
  The current flowing S_u' is switched to S_v' and S_u' is reverse biased.
- (4) Turn off S_u'

(ii) When $e_u < e_v$ [see Fig. 6(b)]
- (1) Turn on S_v'
  But, S_v' doesn't conduct because it's reverse biased.
- (2) Turn off S_u'
  The current flowing S_u' is switched to S_v'.
- (3) Turn on S_v
  The current flowing S_u is switched to S_v and S_u is reverse biased.
- (4) Turn off S_u



(a) $e_u > e_v$



(b) $e_u < e_v$

Fig. 6 Firing sequence of SIT.

3.3 Configuration of Gate Control Circuit

Fig. 7 shows the configuration of the matrix converter gate control circuit. According to the frequency command and the amplitude command of the three phase output voltage, a micro CPU produces the output voltage references [Fig. 8(a)]. These references are compared with the triangular wave form signal [Fig. 8(b)] phase-locked to the supply voltage and amplitude-modulated by the e_{max}- e_{min}, and generates the switching patterns [Fig. 8(c)] which instructs on switching groups S_a, S_b,S_c in the converter to connect the load terminal High(e_{max}) or Low(e_{min}). A gate logical circuit produces the firing pulse signal of Fig.8(d) using the phase informations of the highest voltage e_{max} and the lowest voltage e_{min} given by the voltage detector.

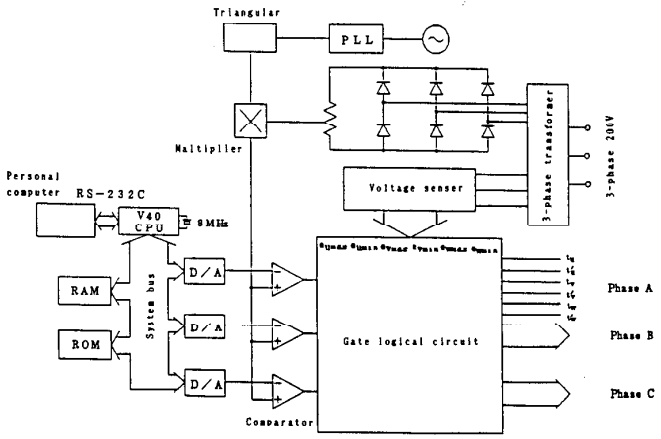
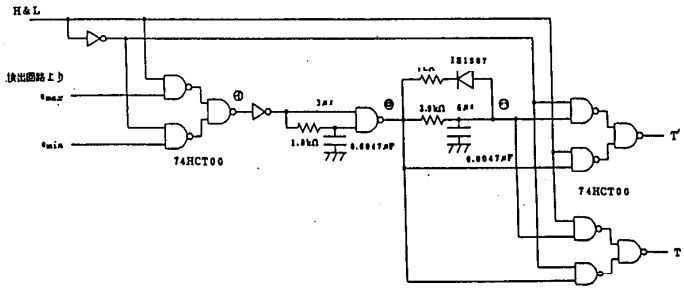
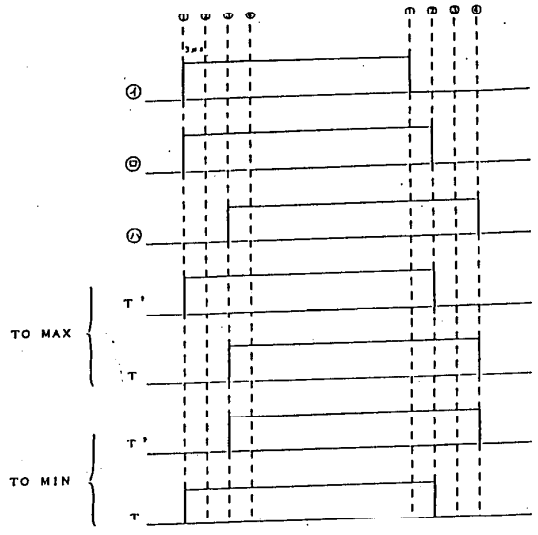


Fig. 7 Gate control circuit.

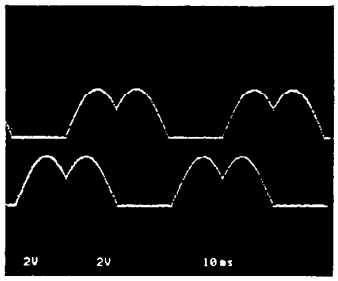


(a)

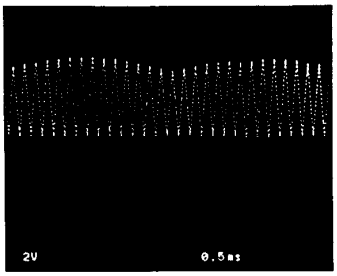


(b)

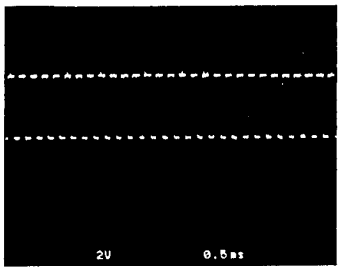
Fig. 9 Gate logic circuit.
(a) Gate logic circuit.
(b) ON, OFF signal for SIT.



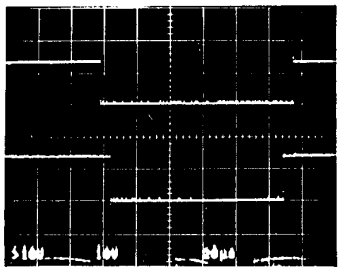
(a)



(b)



(c)



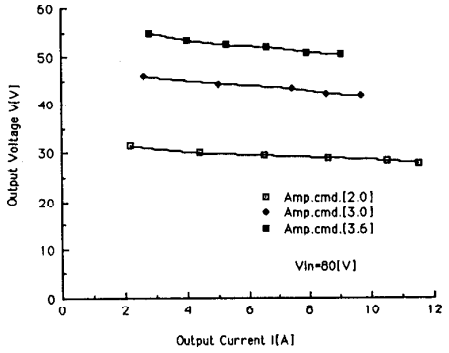
(d)

Fig. 8 Wave forms in gate control circuit.
(a) Output voltage reference
(b) Amplitude modulated triangular wave signal.
(c) Output signal at comparator.
(d) Output command of gate logical circuit.

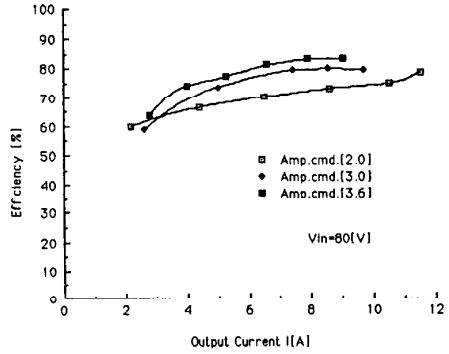
3.4 Gate Logical Circuit

Fig. 9(a) shows the gate logical circuit which generates the gate signals for a pair of SITs T, T'. This circuit generates an ON signal, when (1) both the "H"&"L" signal is 1 and the e_{max} signal is 1 or (2) the "H"&"L" signal is 0 and the e_{min} signal is 1. The signals applied to each of the anti parallel connected SITs are alternated with each other according to the polarity of the source voltage, as shown in Fig. 9(b).

4. EXPERIMENTAL RESULTS



(a)



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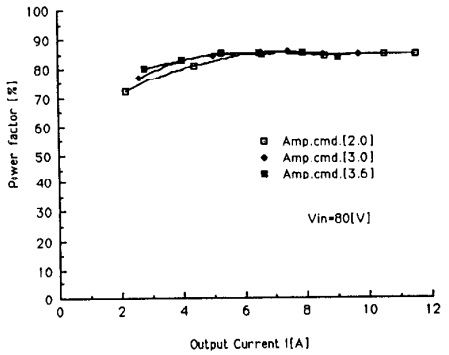


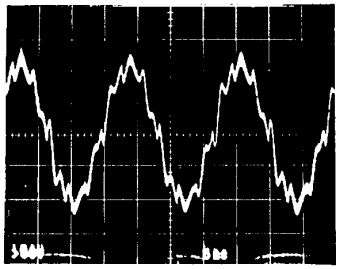
(c)

Fig. 10 Steady state characteristics.
(a) Output voltage.
(b) Efficiency.
(c) Power factor.

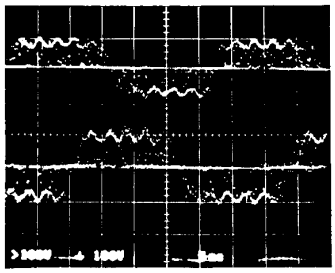
4.1 Resistive Load

Fig. 10(a) shows the output voltage and output current for various output voltage commands. As supply voltage is 80V, the theoretical maximum value of the output voltage is 69.2V. However, the experimental value is about 60V because of a voltage drop in the SITs and the diodes. Fig. 10(b), (c) shows the efficiency and the power factor, respectively. In spite of having serial diodes, the efficiency is larger than 80%. The efficiency will be improved by development of SITs with a reverse voltage blocking ability. The input fundamental power factor is always 1, and the apparent power factor is lager than 80%.

Fig. 11 shows the input and output voltage wave forms. The output voltage wave form is PWM controlled almost sinusoidally. The disorder of the input voltage wave form is relatively small. The wave form can be improved by introducing the input current wave form control by making use of the other phase voltage.



(a)



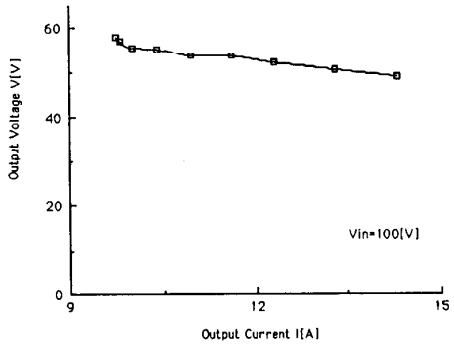
(b)

Fig. 11 Experimental wave forms.
(a) Input voltage.
(b) Output voltage.

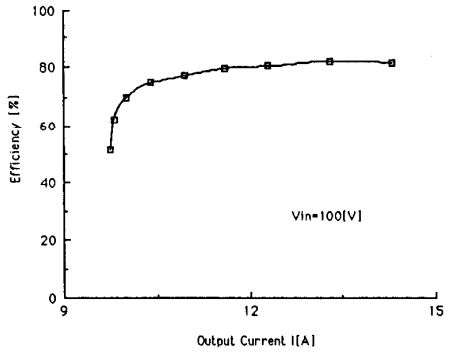
4.2 Induction Motor

Fig. 12 summarizes the experimental results under operation of an induction motor. It is shown that the converter operation is stable and has good performance. The efficiency is larger than 80%.

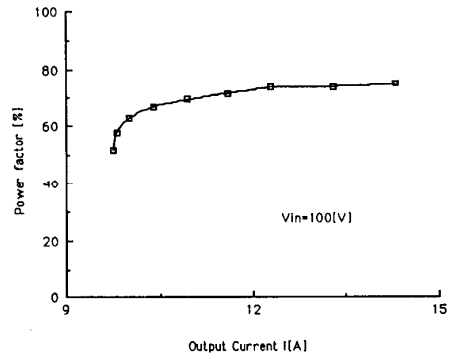
Fig. 13 shows the input and output voltage wave forms. There is no voltage spikes, as shown in Fig. 14.



(a)

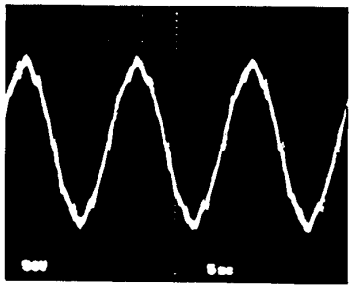


(b)

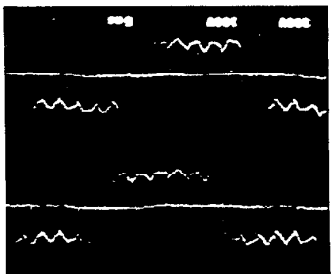


(c)

Fig. 12 Steady state characteristics.
(a) Output voltage.
(b) Efficiency.
(c) Power factor.



(a)



(b)

Fig. 13 Experimental wave forms.
(a) Input voltage.
(b) Output voltage.

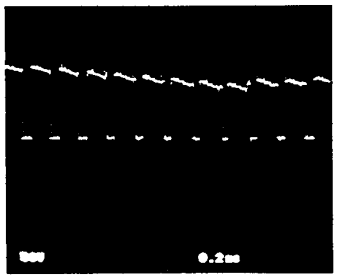


Fig. 14 Experimental wave form.

5.CONCLUSION

A new control strategy for the matrix converter is proposed and the system operation is examined and confirmed by experiments. SITs are used for the system. The followings are the conclusions of the study.

(1) The proposed new control strategy allows to generate the output voltage of 0.866 times the supply voltage, and the fundamental power factor is always 1.

(2) The proposed firing sequences eliminate the voltage and current spikes which are inevitable in the Prof. Venturini's system.

(3) The SITs, high-voltage high-power high-speed switching devices, make it possible to design the small-size large-power matrix converter system.

(4) This system has high efficiency better than 80% despite the series diode. The efficiency can be increased by development of SITs with a reverse voltage blocking ability.

We can control output current wave form also [6]. Furthermore, we can control input current wave form and the power factor by making use of the other phase voltage. We'll report next time about these in detail.

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