The College of Engineering
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RESEARCH REPORT
91-15

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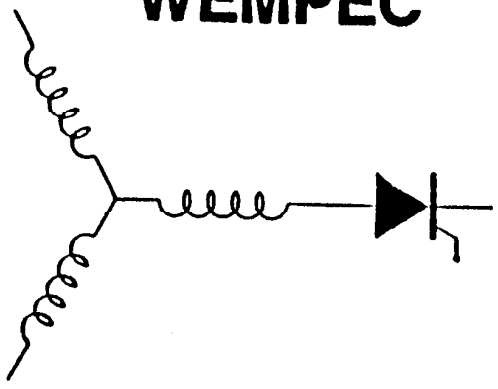

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Abstract Three phase simultaneous current pulse control for a high frequency series resonant DC link converter has been achieved by modifying a previously developed pulse trimming method. In this paper a method of implementing simultaneous flow of current in all phases is described by which excellent current waveforms and low torque-ripple performance can be obtained for an induction motor load.

Introduction

Soft switched high frequency resonant-link power conversion utilizing zero-volt or zero-current switching has been rapidly developed in recent years. The method features the possibility of having not only a high power density, but also very low switching losses. Previously, the authors presented a series resonant dc link type ac to ac power conversion scheme in 1988 [1]. The scheme was the dual of the parallel resonant dc-link type [2] and the switching is accomplished at zero current instants. The converter involves such problems as output current fluctuations and even system instability that appears to be due to the inability to perform rapid control of individual current pulses. Although the problem was basically solved by the pulse trimming method presented in 1989 [3], the trimming method was not enough to obtain sufficiently smooth output current to drive induction motors. The pulse trimming ability of the converter is enormously improved in this paper by using a dual-flow resonant pulse concept. That is, the trimming is done on two phases at a time, dividing the original pulses in an optimal ratio such that a smooth current flow is available on the three output phases.

Concept of Dual-Flow

Single-flow Trimming

Figure 1 shows a prototype of a series resonant dc link converter with the trimming circuit shown in dotted lines. Series inductances L_{01} and L_{02} and a capacitance C_0 form the high frequency resonant circuit and both the three capacitors at the output and at the input are the filters for high frequency components to maintain the resonant frequency. Parallel inductance L_d superimposes the dc current I_d to the high frequency resonating current. The resonating current starts by triggering four thyristors as shown in black. As the average value of the current pulse is equal to the dc current I_d, the adjustment can be done by the input converter although rapid adjustment is difficult because of the large inductance L_d.

The extra thyristor T_{trim} shown as a dotted line, is utilized to trim the resonating current i_s and the basic process of trimming is shown in Fig. 2. In Fig. 2(a) when the current i_s increases and reaches the threshold I_{trim}, T_{trim} is triggered and the current i_s decreases to i_s' (= $i_s - i_{trim}$), i.e., the current i_s becomes fully adjustable by adjusting I_{trim}. An example of currents i_{sa}, i_{sb} and i_{sc} is also shown in Fig. 2(b) for a linear variation of the references i_a^*, i_b^* and i_c^* shown in dotted lines. Although this trimming method allows the system to possess flexible adjustability of the current, the dead zone between the pulses is wide and it causes pulsation in the output current and voltage. Therefore, a relatively large torque ripple still remains if this system is applied to drive an induction motor.

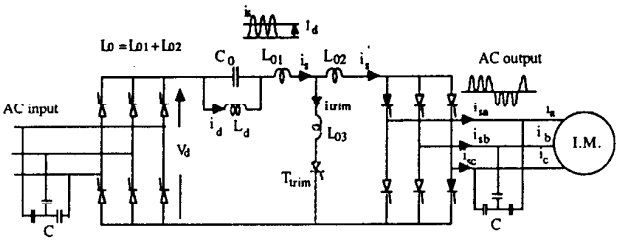


Fig. 1. High frequency series resonant DC link ac/ac converter with conventional pulse-trimming control.

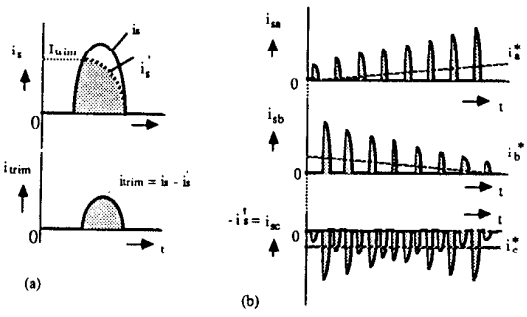


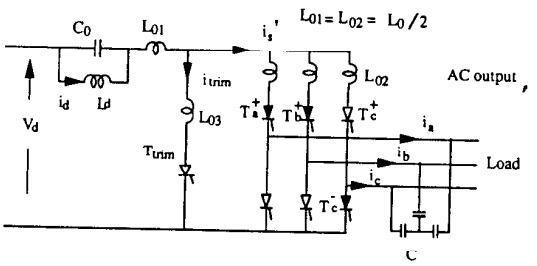
Fig. 2. Principle of pulse-trimming control of the conventional circuit.

Dual-Flow Scheme

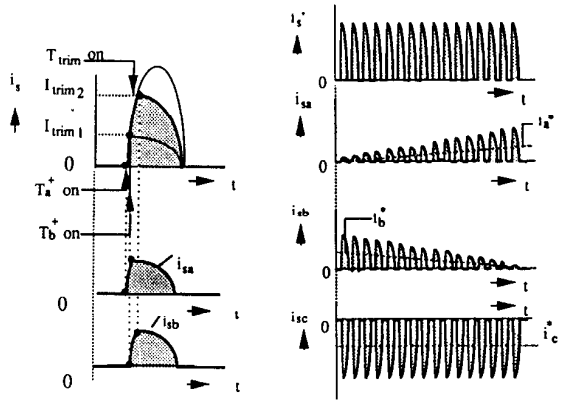
To increase the ability of current adjustment to achieve even less ripple and also increase stable operation of the system, a dual-flow current trimming concept is introduced in this paper. Figure 3(a) illustrates the basic concept of dual-flow trimming in which three inductors denoted by L_{02} are added in series to main thyristors T_a^+, T_b^+ and T_c^+ instead of the single inductance L_{02} in Fig. 1. When T_a^+, shown in Fig. 3(b), is triggered, the current i_s begins to flow to i_{sa}. After a short period during which time i_s reaches threshold I_{trim1}, T_b^+ is triggered causing current i_{sb} to flow. When trimming thyristor T_{trim} is triggered at the threshold I_{trim2}, the final currents i_{sa} and i_{sb} become as shown in Fig. 3(b). These currents are adjusted by changing the threshold values I_{trim1} and I_{trim2}. The adjustment in the two phases results in simultaneous control of all three phases since the remaining phase current is automatically decided from the two other currents. Current references as in Fig. 2(b) are used and the currents i_{sa}, i_{sb} and i_{sc} become uniform and smooth pulse trains result as shown in Fig. 3(c).

Circuit Modifications

Figure 4 illustrates the necessary modification of the circuit shown in Fig. 3(a). In Fig. 4(a), the trimming thyristor T_{trim} and inductance L_{03} are removed and thyristor T_c^+ is triggered instead of T_{trim} and the currents in the upper thyristors flow in the order ①, ② and ③. For negative current flow, the bottom inductance L_{02}'s are required as shown in Fig. 4(b) and the inductance L_{01} in Fig. 4(a) was removed because the inductance L_{02} of the trimming phase can play the same role as L_{01}. When i_a and i_b become negative, T_a^-, T_b^- and T_c^+ are used instead of T_a^+, T_b^+ and T_c^-. The trimming is done by T_c^- and the current flow becomes as shown. As this system includes six inductors a further simplification was introduced as shown in Fig. 4(c) and the current flow corresponding to Fig. 4(a) is also shown. Figure 5 shows the overall three phase circuit configuration and the input converter has also capacitors to pass high frequency current pulses.



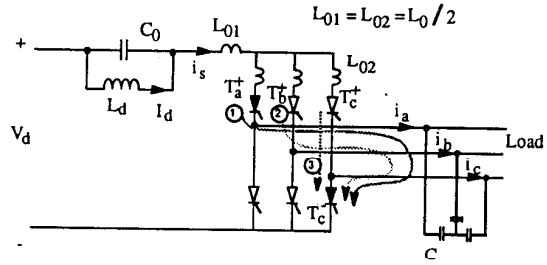
(a) Basic dual flow circuit



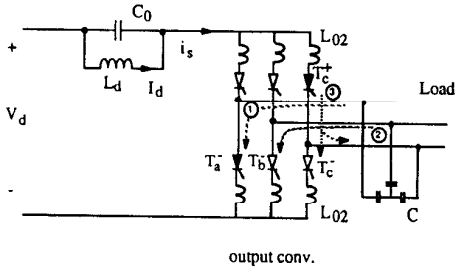
(b) Principle of triming

(c) Output waveforms

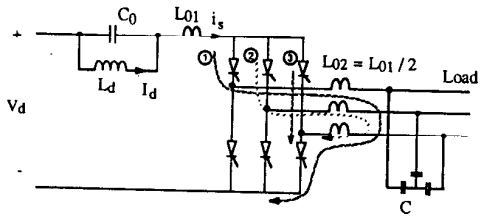
Fig.3. Principle of dual flow pulse trimming.



(a) Eliminating Ttrim



(b) For negative currents.



(c) Reducing inductors.

Fig.4 circuit modifications

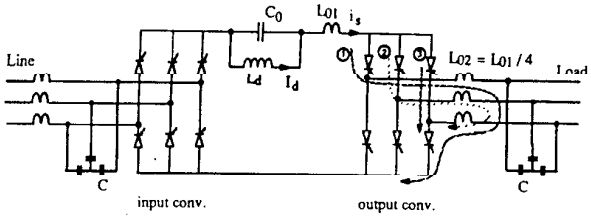


Fig. 5. Three phase ac/ac configuration.

$$E - v_{CL} = L_0 \frac{di_s}{dt} + \frac{1}{C_0}\int (i_s - I_d)\, dt \qquad (1)$$

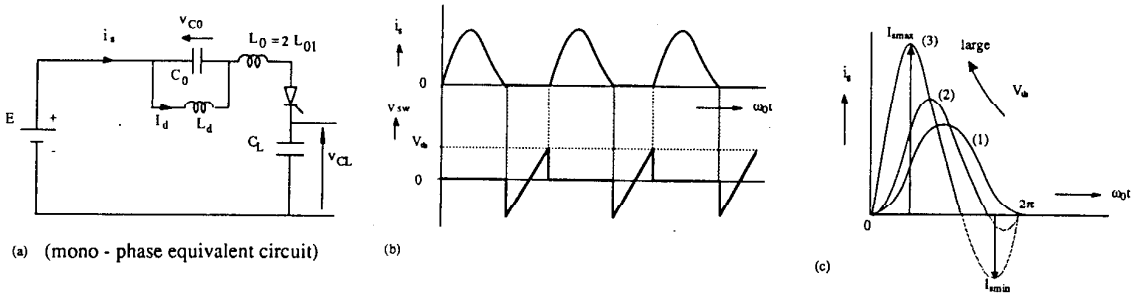
and the resulting current i_s becomes as follows,

$$i_s = I_d (1 - \cos \omega_0 t) + \sqrt{\frac{C_0}{L_0}} V_{th} \sin \omega_0 t \qquad (2)$$

where,

$$\omega_0 = \sqrt{\frac{1}{L_0 C_0}}$$

$$V_{th} = E - V_0 - V_{CL} \quad ; \; V_0 : \text{initial voltage across } C_0. \qquad (2')$$



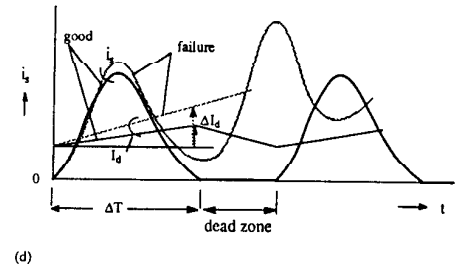


Fig. 6. Illustrations for steady operation of the resonant system

Accordingly, the peak value of i_s is dominated by the dc bias I_d and the threshold voltage V_{th}. For this system, the resonant current i_s should again reach zero to extinguish the conducting thyristors T_h, and a certain amount of reverse bias interval is required for this purpose. From Eq. (2), the maximum current I_{smax} and the minimum current I_{smin} result in the expressions,

$$I_{smax} = I_d + \sqrt{I_d^2 + \frac{C_0}{L_0} V_{th}^2}$$

$$I_{smin} = I_d - \sqrt{I_d^2 + \frac{C_0}{L_0} V_{th}^2} \qquad (3)$$

Figure 6 (c) shows the variations of i_s according to the increase of V_{th}. Obviously, from the figure or from Eq. (3), the resonant current i_s reaches zero even at $V_{th} = 0$, however, the thyristors need a certain reverse voltage to be turned off and positive V_{th} is inevitable. Furthermore, the biasing current I_d is practically not constant because of the finite value of L_d. That is, I_d increases by ΔI_d according to the dc voltage difference $E - V_{CL}$,

$$\Delta I_d = (E_d - V_{CL})\, \Delta T / L_d \text{ , (if } V_{CL} \text{ is assumed constant)} \qquad (4)$$

where ΔT is the period of current flow.

As illustrated in Fig. 6(d), although this rise of ΔI_d is cancelled during the off period by discharging the magnetic energy to charge up the resonant capacitor C_0, the ripple ΔI_d causes commutation failure of T_h if ΔI_d exceeds the limit $|I_{smin}|$. The condition is,

$$\Delta I_d = -I_{smin} . \qquad (5)$$

Basic Considerations of Resonance

The converter with resonating components L_{01}, L_{02} and C_0 is simply represented by the mono-phase equivalent circuit in Fig. 6. (a). The voltage E is the output voltage of the input converter and the capacitors denoted as C are placed both at the input and output and are expressed as a single equivalent capacitor C_L and the thyristor T_h corresponds to four thyristors in conduction in series. In this circuit, when T_h is triggered, the resonant current i_s starts to flow as shown in Fig. 6(b) and again reaches zero. At this point T_h turns off and charging of the capacitor C_0 by the biasing I_d makes the voltage V_{sw} across T_h rise linearly until a specified threshold voltage V_{th} is reached, whereupon the next triggering occurs.

As the inductance L_d and the capacitor C_L are sufficiently large, the dc bias current I_d and voltage V_{CL} across the capacitor C_L can be assumed constant. At this instant, the circuit equation becomes,

By using Eq. (3) and normalizing by I_d,

$$\Delta \bar{I}_d = \Delta I_d / I_d$$

$$= \sqrt{(V_{th}/ z_0 I_d)^2+1} - 1 \; ; \; z_0 = \sqrt{L_0 / C_0}. \qquad (6)$$

Hence, the condition for V_{th} to maintain a stable resonance is approximately obtained as

$$V_{th} \geq \sqrt{2 \Delta \bar{I}_d}\, I_d\, z_0$$

or

$$\bar{V}_{th} \geq \sqrt{2 \Delta \bar{I}_d} \; ; \; \bar{V}_{th} = V_{th} / z_0 I_d. \qquad (7)$$

For the actual dual-flow system, these conditions are adopted to enable each phase to trigger and sometimes can not be satisfied. Dual-flow control then degrades to simple single-flow trimming. Hence, the actual operation becomes amalgamated with dual-flow and single-flow. However, the system works far better than solely single-flow operation.

The maximum capacitor voltage V_{C0max} is one of the limiting factors of loading in this system. Hence, differentiating Eq. (2) and multiplying by L_0, the resonant component of the capacitor voltage is derived as follows.

$$v_{c0} = Z_0 I_d \sin \omega_0 t + V_{th} \cos \omega_0 t$$

$$\bar{V}_{C0max} = \sqrt{1 + \bar{V}_{th}^2} \; ; \; \bar{V}_{C0max} = V_{C0max} / z_0 I_d \qquad (8)$$

The actual maximum capacitor voltage is the sum of above voltage and the initial voltage. The variation in peak voltage stress across the resonant capacitor C_0 for different values of biasing current has been investigated and ploted in Fig.7. The resonant-link frequency has been kept constant at 25 kHz. It could be observed that the falling value of characteristic impeadance resulted in a lower voltage peak at the capacitor C_0. But consequently L_0 starts reducing and set a limit for practical realization of the inductance. Therefore reasonable value for L_0 has to be selected.

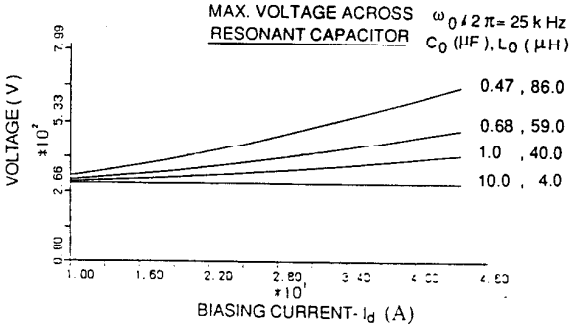


Fig. 7. voltage stresses of the resonant capacitor.

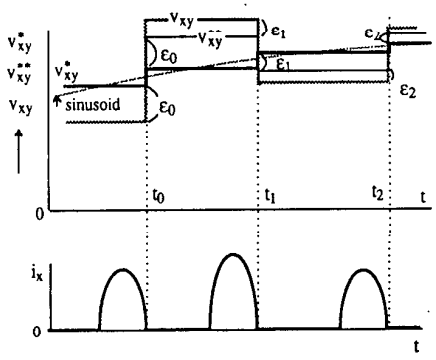
Control Scheme

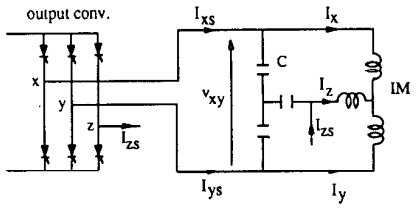
In general, the output control must be concerned with two types of cases. That is,

(1) Output current control with sinusoidal voltage reference. This method is convenient for the case in which the parameters of the load are known such as with field orientation control.

(2) Output voltage control with sinusoidal voltage reference. This method is suitable for general purpose use because it requires only the rated voltages.

The system described in this paper utilizes the latter control method. As shown in Fig. 8, the sinusoidal output voltage reference v_{xy}^* and the actual line voltage v_{xy} (averaged value in a per-pulse period) are assumed to have a stepwise variation over each pulse and both are compared to decide which thyristors in the output bridge should be fired. This system has another reference v_{xy}^{**} (modified reference) to compare with v_{xy}. For example, in the figure, if the deviation $\varepsilon_0 = v_{xy}^* - v_{xy}$ exists at $t = t_0^-$, the modified reference during $t_0 < t < t_1$ is set as $v_{xy}^{**} = v_{xy}^* + \varepsilon_0$, then the required charge to boost up the next average voltage v_{xy} to the reference v_{xy}^{**} is performed. After this decision, if a deviation $\varepsilon_1 = v_{xy}^{**} - v_{xy}$ results at $t = t_1^-$, the deviation will be used for the next modified reference as $v_{xy}^{**} = v_{xy}^* + \varepsilon_1$ as illustrated in the figure. This method of control is fundamentally an integral compensator and it significantly improves the output torque ripple performance for induction motor drives.

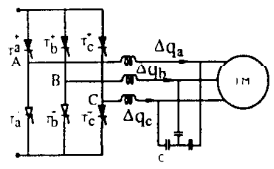




(definition of voltages and currents)

Fig. 8. out-put voltage error compensation

To select the triggering thyristors and the triggering timing, the charges required for the next period to cancel the voltage deviation ε's are estimated at the output capacitors. The detailed estimation about the required charges will be explained in the Appendix. Six possibilities for selecting the thyristors of the output bridge are defined in Table 1. The Δq's with suffixes represent the charge demand by each phase to correct voltage errors at the output.



definition of charges

MODE	Δq_a	Δq_b	Δq_c
1	+	+	−
2	+	−	+
3	−	+	+
4	−	−	+
5	−	+	−
6	+	−	−

polarities of required charges

Table 1. Required charge and polarity.

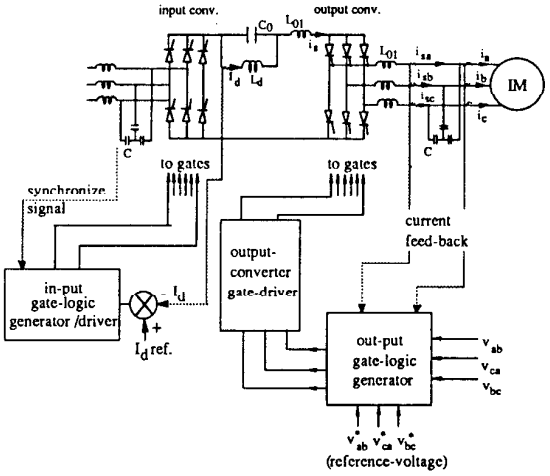


Fig.9. Control diagram of overall system

Positive signs in the table indicate the thyristors with a positive sign in Fig. 4 (top three thyristors) and the negative signs indicate the thyristors with a negative sign (bottom three thyristors). Having decided the mode based on the polarity of the demanding charge, firing order is established. The thyristor fired first is the one connected to the phase with the largest charge demand out of two phases with the same charge polarity.

In general, there will be a waiting interval until both thyristors reach the threshold voltage V_{th} to ensure the conduction of both of devices. When the first firing phase is decided, the required charge starts to reduce and reaches the same amount as that of the second phase. At this moment the next phase also triggered provided that the forward biasing V_{th} is still satisfied. Then the dual-flow starts and charges are pumped into the system, obtained by real time integration (using simple R-C circuits with reset) of the current pulse. When the initial charge demand is satisfied, the trimming phase thyristor is activated which diverts the current back. For instance, if the selected mode is '1' and the phase 'a' has the higher charge demand, then T_a^+ and T_c^- become the first thyristors to be triggered and trimming is done using T_c^+. Considering the fact that even after the trimming, charges may flow into phases 'a' and 'b', trimming is done in a little advance of this instant.

Figure 9 shows the overall system including the control diagram. Output gate logic decides which thyristors to be turned on by using above method. The input logic-generator is used both for control I_d and for unity power factor with sinusoidal current waveforms using the same PDM control method as used in [4].

Discussion

It has already been noted that the firing order of the thyristors are decided based on the magnitude of charge demanded by each phase. By extensive simulation studies, this criterion was found to be effective in reducing torque ripple and in improving stability. It is important to note that this scheme achieves the maximum benefit if the forward bias voltages are kept over V_{th} until both devices are turned on.

Accordingly, dual-flow scheme naturally features the optimum use of energy constituting a fast acting power converter. But, since all three thyristors are not fired at the same time there may be occasions where the second and trimming thyristors are not operable due to the lack of forward bias. Therefore, to assure the conduction of all thyristors dead zone is extended until all the selected thyristors have reached V_{th}. This may cause, however, a higher voltage V_{th} over the two switches to be fired later. Therefore, the peak current (Eq. 3) of the resonant pulse has to be calculated considering the worst case of output voltage combinations. Since a finite value of C_L is used, output voltage fluctuations are typically observed. However, accurate control of charges delivered to each phase, proper selection criterion based on the charge demand of thyristors and an increase of the link frequency result in low harmonic content at the output voltage and current together with low torque ripple. Since the calculation of the charge demand for each phase involves simple linear equations it can be easily performed within the dead-zone. The control does not use instantaneous quantities of current or voltage which would make the system non-realizable. Since the control does not involve any characterization curves based on the system parameters, better adaptability to different loading conditions and different I_d values are important features of the control scheme.

The results obtained by digital simulation are shown in Fig 10 and 11, and depict improvements in performance obtained by the dual-flow scheme. Figure 10(b) shows the synthesized output voltage waveform v_{ab} and the superimposed reference voltage. It should be seen that the synthesized voltage satisfactorily produces the reference voltage resulting a smoother motor current wave which is given in Fig. 10(c). It can be seen that torque ripple produced by the dual-flow in Fig. 11(a) and (b) have been drastically reduced as compared to the torque wave obtained in single flow scheme in Fig. 11(c).

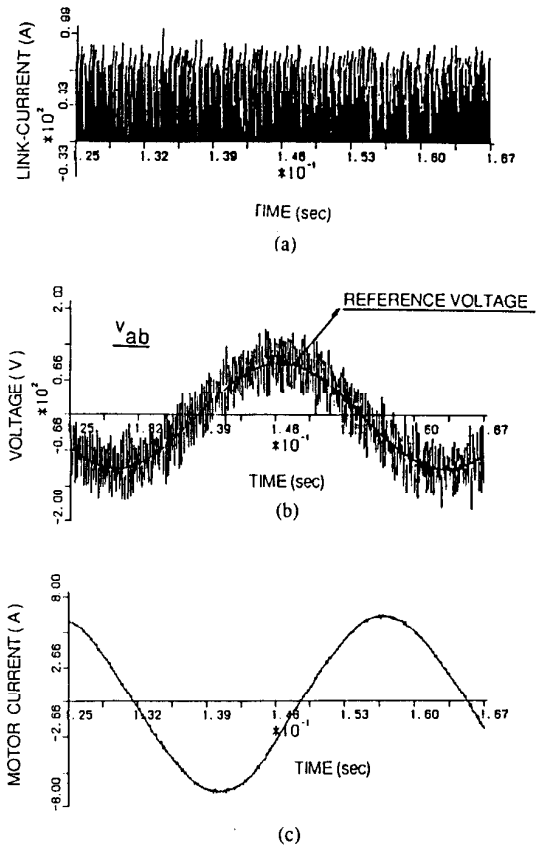


Fig. 10. Performances of the dual - flow DC link inverter

Conclusion

Dual-flow pulse-trimming has been illustrated for high frequency resonant DC link power conversion and it has been shown to enable the system to achieve more stable operation with less induction motor torque ripple. This system achieves good output waveform and is very suitable for general purpose ac/ac converters. At this moment, this system works up to 30 kHz of resonant frequency by using high speed thyristors (900v, 50A, 10μs turn-off-time of ratings). The primary drawback is the size of the output capacitors and dc inductance L_d. A corresponding rise in the resonant frequency when using faster devices such as MCT's, SI thyristors or IGBT's will be one of solutions for this problem in the future.

References

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[3] Y. Murai, S. Mochizuki, P. Caldeira, T. A. Lipo," Current pulse control of High Frequency Series Resonant DC Link Converter," IEEE-IAS Conference Record, 1989, pp. 1023-1030.

[4] P. Caldeira, K. W. Marschke, M. T. Aydemir, T. A. Lipo and Y. Murai," Utilization of the Series Resonant DC Link as a DC Motor Drive," IEEE-IAS Conference Record, 1990, pp. 813-819.

Appendix

Required Charges

As in Fig. 8, assuming average currents to flow in all phases simultaneously,

$$I_{xs} + I_{ys} + I_{zs} = 0$$

$$\Delta V_{xy} = (I_{xs} - I_x - I_{ys} + I_y)\,\Delta t / C_L$$

$$\Delta V_{zy} = (-I_{ys} + I_y + I_{zs} - I_z)\,\Delta t / C_L$$

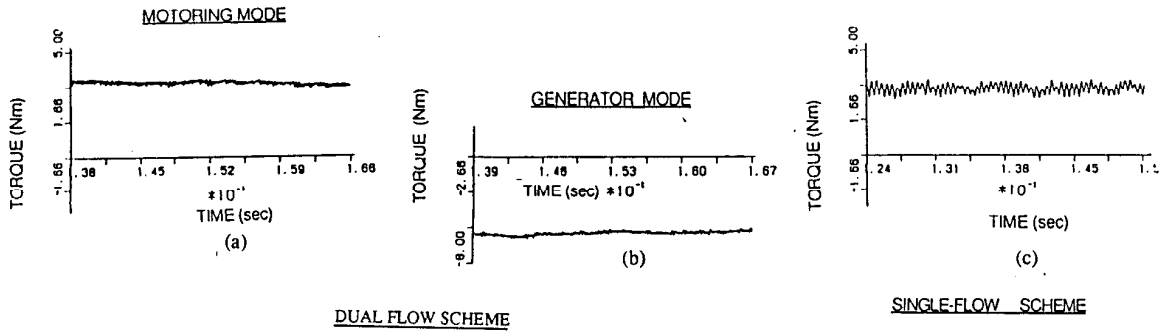

Fig. 11. Comparison of torque characteristics (dual-flow / single -flow)

$$\Delta V_{xz} = (- I_{zs} + I_z + I_{xs} - I_x)\, \Delta t / C_L \qquad (9)$$

Defining,

$$\begin{aligned} I_x\, \Delta t &= \Delta q_x \\ I_{xs}\, \Delta t &= \Delta q_{xs} \\ \Delta V_{xy}\, C_L &= \Delta q_{xy} \end{aligned} \qquad (10)$$

(similar notations are adopted for other phases)

Substituting these values in Eqs. (2), (3), (4) and solving for Δq_{xs}, Δq_{ys}, Δq_{zs} it can be proven that,

$$\begin{aligned} \Delta q_{xs} &= (\Delta q_{xy} + \Delta q_{xz} - \Delta q_y - \Delta q_z + 2\, \Delta q_x) / 3 \\ \Delta q_{ys} &= (- \Delta q_{xy} - \Delta q_{zy} - \Delta q_x - \Delta q_z + 2\, \Delta q_y) / 3 \\ \Delta q_{zs} &= (\Delta q_{zy} - \Delta q_{xz} + 2\, \Delta q_z - \Delta q_x - \Delta q_y) / 3 \end{aligned} \qquad (11)$$

In particular, it should be noted that,

$$\Delta q_{xs} + \Delta q_{ys} + \Delta q_{zs} = 0 \qquad (12)$$

These equations give the necessary and sufficient condition for correcting errors in all three phases, provided that the dual flow is occurring. Further, from Eq. (7), since the required charges follow the relation $\Delta q_{xs} + \Delta q_{ys} + \Delta q_{zs} = 0$, triggering thyristors can be uniquely defined as shown in the Table 1.