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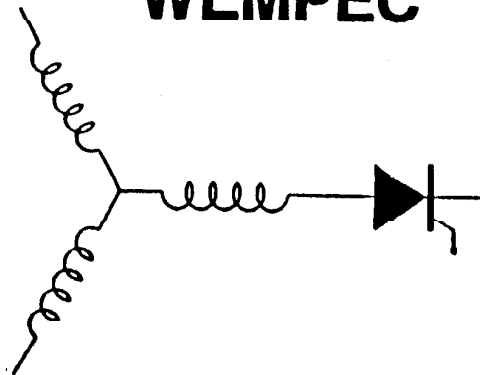# Wisconsin Electric Machines and Power Electronics Consortium

RESEARCH REPORT
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Current Peak Limiting for a Series Resonant DC Link Power Conversion Using a Saturable Core

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Abstract. High frequency resonant dc link power conversion circuits often experience irregular high peak current pulses during three phase operation and the pulses rise to over twice the regular pulse amplitude giving rise to current or voltage fluctuations at the output side. This high peak current/voltage problem appears to be common to both series/parallel resonant types respectively because of duality of the systems. In this paper current peak limiting has been performed by means of a saturable core inserted in the DC link as the resonant inductance. A simplified circuit limiting peak current is proposed and the resulting performance of the system is investigated by digital simulation.

Keywords. Series resonant dc link, Resonant link converter, Zero current switching, High density power conversion.

INTRODUCTION

Power conversion schemes with an ac or dc resonant link, featuring zero voltage or zero current switching have expanded enormously recently. The method involves the possibility of having not only very low switching losses but also a higher power density. In a previous paper several of the authors proposed a series resonant dc link type ac to ac power conversion scheme [1]. This converter is the dual of the parallel resonant dc link type and the switching occurs at zero current instants. In addition, the system utilizes only twelve thyristors for full double bridges at the input and at the output. Thus it features a minimum number of devices as well as high current and high voltage withstand margins because of the use of thyristors.

However, this system experiences very high peak currents depending upon the voltage difference when the conducting phase changes. The pulse amplitude occasionally becomes two or three times larger than that of the normal pulse height and disturbs the output current as well as the voltage regulation. In the case of the parallel resonant dc link converter, the problem encountered is not the occurrence of high current peaks but high voltage peaks that arise when the switching of conducting transistors occurs between phases. This situation is expected since the two schemes are duals of each other. A method of voltage clipping for that system was presented by utilizing an extra transistor, diode and a capacitor [2].

It is shown in this paper, that to realize current clipping, a simple saturable ferrite core can be employed in place of the resonant inductance. The principles of the pulse limiting and the simplification of the circuit are explained in detail and the control strategies adopted are discussed. A new method for establishing the switching function and a feed back method for selecting the optimum biasing current, are also presented. Since the trimming or circulating current mode is not used, this system allows a simple control method for operation while still maintaining stability accompanied by good motor torque characteristics.

PRINCIPLE OF OPERATION

Prototype System
Figure 1 shows a prototype of a series resonant dc link converter. The inductance L_0 and the capacitance C_0 form the high frequency series
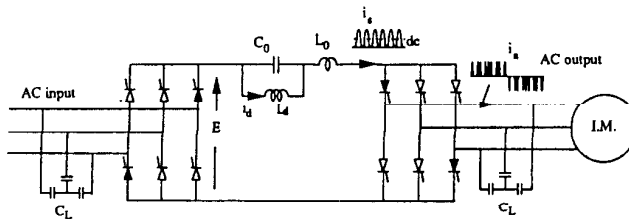
resonant circuit and the capacitor banks at the output and input are simple low-pass filters needed to maintain the resonant frequency and to obtain better output and input current waveforms. The resonating current i_s is shown in the figure. The dc current I_d is superimposed on the resonant current by the inductance L_d which is very large and is considered as a constant current source.

The resonating current i_s begins by triggering the four thyristors shown in black. After the occurrence of each current pulse, all the thyristors are extinguished and bias current I_d begins charging the resonant capacitor C_0 linearly so that the forward bias is reached for the next pair of thyristors to be triggered. When the forward bias has reached a settled threshold voltage, the next set of four thyristors are triggered to obtain a new current pulse.

The switching of main thyristors is done only at zero current instants of i_s resulting in very low switching losses. The current pulses are distributed to each phase by the method of Pulse Density Modulation (PDM)[1].

Resonant Pulses
A mono-phase equivalent circuit of the three phase converter topology is shown in Fig. 2 (a). The voltage E is the output voltage of the input converter and V_{CL} is the line line voltage of the output capacitor bank. The capacitor C_L represents the effective lumped capacitance of the filter capacitors at the input and output bridges. Thyristor T_h represents the effect of the conducting four thyristors in series and the selector switch shows the possibility of selecting different output phases.

Due to the fact that the inductance L_d is sufficiently large, the DC off-set given by the current I_d is almost constant. Since the output frequency is low compared with the resonant frequency and the capacitor C_L is also relatively large, the voltage V_{CL} across the capacitor C_L can be assumed constant over the period of each current pulse. Under these assumptions, the circuit equation is simplified as,

$$E - V_{CL} = L_0 \frac{di_s}{dt} + \frac{1}{C_0} \int (i_s - I_d) \, dt \tag{1}$$

and the resulting current i_s becomes

$$i_s = I_d (1 - \cos \omega_0 t) + \sqrt{\frac{C_0}{L_0}} V_{th} \sin \omega_0 t \tag{2}$$

where,

$$\omega_0 = \sqrt{\frac{1}{L_0 C_0}}$$

$V_{th} = E - V_0 - V_{CL}$; V_0 : initial voltage across C_0.

$$\tag{2'}$$

Fig. 1. Conventional high frequency series resonant DC link ac/ac converter.

Therefore, the peak value of i_s is dominated by the DC off-set I_d and the *threshold voltage* V_{th}. From equation (2), the maximum current I_{smax} can be expressed as

$$I_{smax} = I_d + \sqrt{I_d^2 + \frac{C_0}{L_0} V_{th}^2}$$

(3)

Therefore I_{smax} becomes constant provided that V_{th} and I_d are kept constant as shown in Fig. 2 (b).

Irregular Current Peaks
When the output thyristors are switched between different output phases, triggering at V_{th} is not always available. As a result, irregular current peaks appear as shown in Fig. 2 (c). In Fig. 2 (a), if the thyristor T_h stops conducting at time t_1, the following equations are possible with reference to the circuit in Fig. 2 (a).
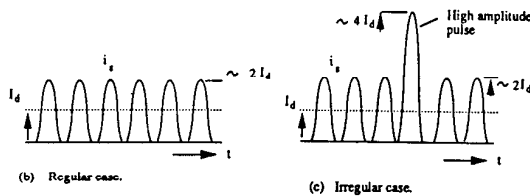
$$E - \left(V_{C0} + L_0 \frac{d\{i_s(t)\}}{dt}\right)_{t = t_1^-} - V_{01} = 0$$

(4)

where the phase selected has an output voltage of V_{01}. As the capacitor voltage V_{C0} does not change instantaneously, the voltage of inductance L_0 just before t_1 moves to the voltage V_{swt} across thyristor T_h at the moment just after t_1; that is,

$$\left(V_{swt}\right)_{t = t_1^+} = \left(L_0 \frac{d[i_s(t)]}{dt}\right)_{t = t_1^-}$$

$$= E - \left(V_{C0}\right)_{t = t_1^-} - V_{01}.$$
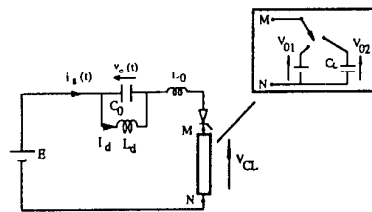
(5)
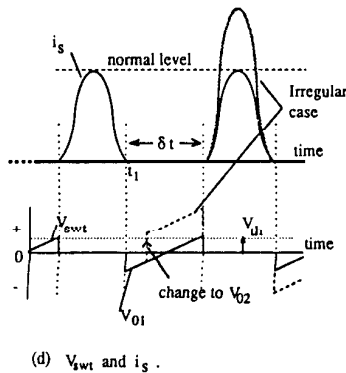
When thyristors stop conducting at time t_1, the calculation for selecting the next mode is accomplished during the interval given by δt and the capacitor charges up linearly by the constant biasing current I_d. The voltage V_{swt} goes up to V_{th} where the next triggering is scheduled as shown in Fig. 2 (d);

$$\left(V_{swt}\right)_{t = t_1 + \delta t} = V_{th}$$

$$= \left(V_{swt}\right)_{t = t_1^+} + I_d \frac{\delta t}{C_0}$$

$$= E - \left(V_{C0}\right)_{t = t_1} - V_{01}.$$

(6)

However, when V_{02} is selected for the next current pulse, V_{swt} changes to

$$\left(V_{swt}\right)_{t = t_1 + \delta t} = E - \left(V_{C0}\right)_{t = t_1^-} - V_{02}$$

(7)

This case is equivalent to the case where the selector switches move from V_{01} to V_{02} in Fig. 2 (a) during the period $t_1 < t < t_1 + \delta t$. If the voltage V_{02} is much larger than V_{01}, V_{swt} at $t = t+\delta t$ rises far beyond V_{th} and a high peak current pulse results as shown in dotted line in Fig. 2 (d). As a result the system becomes disturbed. Since the biasing current I_d varies because of finite inductance L_d, I_d control, carried out by switching the input thyristors to other input phase voltages according to the error ε in I_d ($= I_{dref} - I_d$), is difficult. Since the voltage E also changes, it exaggerates the above phenomena.

CURRENT PEAK LIMITING

Current peak limiting is proposed to eliminate undesirable high pulses from occurring and to assure uniform pulse height. Figure 3 illustrates the basic idea of current peak limiting. The system shown in Fig. 3(a) illustrates a simplified mono-phase equivalent circuit for current peak limiting. In this circuit, the resonant inductance L_0 is replaced by a saturable inductance with a biasing current I_m and the dc inductance L_d is expressed by a constant current source I_d.

The principle of the current pulse limiting is illustrated in Fig. 3(b). In the characteristic of the saturable reactor, i.e., existing current $i_s + I_m$ vs. magnetic flux linkage λ, the current I_m biases the core in the negative direction. The gradient of the slope in the saturated region is equal to the resonant inductance L_0 and the non-saturated region offers a very high inductance. In the circuit in Figure 3(a), when the thyristor T_h is triggered the current pulse starts flowing and the flux λ begins to increase toward point 2 and then to 3 and the current reaches almost a plateau, suppressed by the high inductance and returns to zero passing through points 3, 4 and 5 in that order and the corresponding current wave becomes as shown in Figs. 4(a) and (b). Figure 5 shows the actual three phase configuration with current peak limiting.
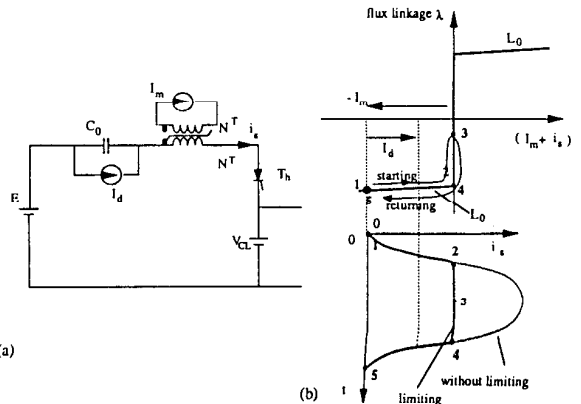

(a) Simplified mono-phase model

(b) Regular case.

(c) Irregular case.

(d) V_{swt} and i_s .

Fig. 2. Current pulse peak at conventional system.

(a)

(b)

Fig. 3. Illustration for the principle of current pulse limiting.
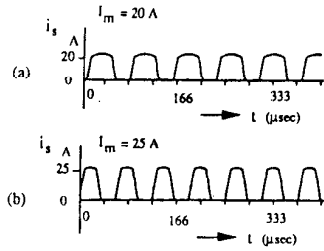
Fig. 4. Examples of current pulses i_s
for the circuit with saturable core.

SR: Saturable reactor

Fig. 5. Actual circuit configuration with current peak limiting.

In this system the biasing current is simply fed from the inductor L_d and the biasing current automatically changes according to the load current.

CONTROL SCHEME

Output Converter Control
In this scheme the output voltage of the converter has been defined and the actual output voltage is compared with the reference voltage to generate a switching function. In the implementation of the scheme, the output reference voltages are modified from pulse to pulse by which means the voltage feedback is indirectly achieved.

The output voltage feedback criterion is illustrated in Fig. 6. For example, let v_{ab}^* and v_{ab}^{**} represent the defined reference and the modified reference, respectively. When the deviation $\varepsilon_0 = v_{ab}^* - v_{ab}$ exists at $t = t_0^-$, the modified reference during $t_0 < t < t_1$ is set as $v_{ab}^{**} = v_{ab}^* + \varepsilon_0$, then the required charge to boost up the next average voltage v_{ab} to the reference v_{ab}^{**} is performed. After this procedure, if the deviation $\varepsilon_1 = v_{ab}^{**} - v_{ab}$ results at $t = t_1^-$ the deviation ε_1 will be used for the next modified reference as $v_{ab}^{**} = v_{ab}^* + \varepsilon_1$ as illustrated in the figure. This method is also particularly effective in reducing the torque ripples of induction motor drives.

The overall system diagram is given in Fig. 7. Thyristor selection for triggering is performed based on the sign of the charge demand by each phase and the estimation of charges required is done in such a manner that the errors sustained in the output voltage are canceled out with the estimated charges. A detailed derivation of charges required to correct voltage errors at the output is given in the Appendix.

Since the required charges Δq_{as}, Δq_{bs}, and Δq_{cs} follow the relation $\Delta q_{as} + \Delta q_{bs} + \Delta q_{cs} = 0$ in eq. (11), three thyristors can be uniquely defined as shown in Table 1. For a particular "MODE" in Table 1, there appear two charge quantities with the same sign as shown in Table 2. Two thyristors in the output bridge are selected for firing at a time. Therefore, having decided the mode, the two thyristors to be fired next, are selected. For this purpose, the comparison between the

(definition of voltages and currents)

Fig. 6. Output voltage control.

MODE	Δqa	Δqb	Δqc
1	+	+	-
2	+	-	+
3	-	+	+
4	-	-	+
5	-	+	-
6	+	-	-

+ : Positive charge
- : Negative charge

Table 1. Polarity combinations
of required charges.

MODE	Δqa	Δqb	Δqc
1	+		-
1		+	-
2	+	-	
2		-	+
3	-		
3		-	+
4	-		+
4		-	+
5	-	+	
5		+	
6	+	-	
6	+		-

+ : Upper thyristor
- : Lower Thyristor

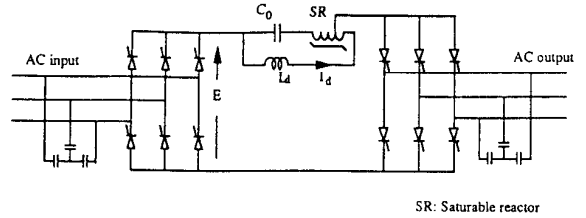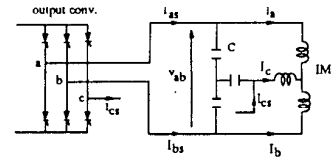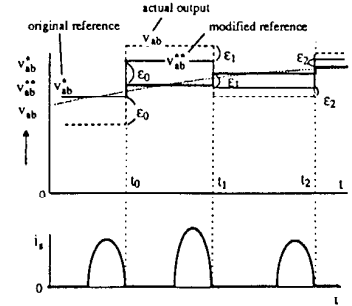Table 2. Combinations of triggering
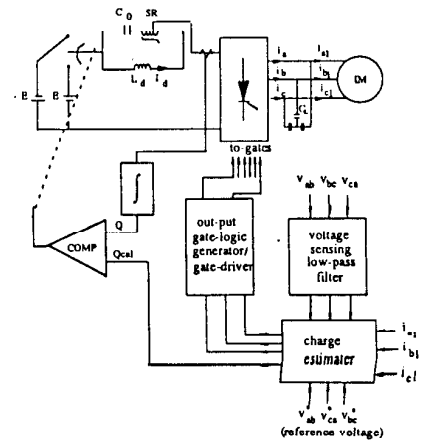thyristors for the modes of Table 1.

Fig. 7. Overall control diagram.

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magnitude of required charges is done. The phase thyristors with positive maximum and negative maximum required charges are selected.

The relevant columns in Table 1 to which the selected charge belongs gives the two lines to be selected. Positive signs in Table 1 indicate the thyristors with a positive sign (top three thyristors) and the negative signs indicate the thyristors with the negative sign. Accordingly, the thyristors shown in black in Fig. 1 and Fig. 5 represent Mode 1 and it follows from Table 2 that at this instant Δq_a is larger than Δq_b.

Input Converter Control

The input converter involves I_d control with reference I_{dref} which is determined by the required charges. Hence, this system uses a current feedback loop from the output to the input converter in addition to the voltage feedback used in the control of output converter. As the load increases, system needs a larger I_d for the energy balance.

In the implementation of the system, I_d adjustment can be achieved by a simple feedback criterion that uses comparison of charges. It should be noted that if the thyristor threshold voltage V_{th} is defined, then the charge Q afforded by a single current pulse is roughly calculated by the bias current I_d. Therefore, to maintain an energy balance between input and output, an adequate I_d should be selected to balance the required charge Q_{req}. Fig. 8 shows the tendencies of Q and Q_{req} according to biasing current I_d which is normalized by the amplitude I_0 of output motor current.

To the left of the balancing point P in Fig. 8, the possible charge Q is less than the required value Q_{req}, in which case Q is not sufficient to correct the errors and the motor currents are not smooth. When I_d is increased beyond the balance point, the system has a higher capability of correcting errors but the ripple in the output voltage increases. Hence, I_d control should be implemented so as to balance Q with Q_{req}, i.e., $I_d / I_0 \cong 2$. Therefore, the thyristors in the input converter should be switched to have the polarity of the output voltage E as,

(i) If $Q > Q_{req}$, input DC voltage is switched to +E
  to increase I_{dref}.

(ii) If $Q < Q_{req}$, input DC voltage is switched to -E
  to decrease I_{dref}.

The voltage E depends on the input three phase voltages and the selection of triggering phases is performed as the same manner as in [3] to have simultaneous unity power factor and sinusoidal input current.

Other Calculated Results
Figure 9 shows the tendency of the pulse frequency and the ripple voltage in the output. In this figure, when I_d increases, the pulse frequency increases because of less δt [the interval between pulses in Fig. 2 (d)] and the output ripple voltage V_{ripple} increases because of the increased supply of charge. It also shows that the larger filter capacitor C_L causes smaller voltage ripple in the output. In Fig. 8, it is demonstrated that as δt decreases according to the increase of I_d, the required per-pulse-charge Q_{req} with constant output current I_0 also decreases before the balancing point P, whereas the charge Q_{req} again increases after P because of excessive regulation by an excessive supply of charge.

Figure 10 shows dependencies of the peak voltage stresses across the resonant capacitor and across the thyristors. The figure also shows that V_{ripple} depends on the increase of capacitor C_L. According to the increase of C_L, smoother motor current and less voltage stresses on resonant elements and switches clearly result. In Fig. 11, simulated waveforms are shown. In Fig. 11 (a), pulses are shown with very small amplitude fluctuation compared with that of the previous prototype system [1]. Figure 11 (c) and (d) show the output voltage and current. Both are clearly well regulated and have sinusoidal waveform.

CONCLUSION

In this paper, a new current-peak limiting scheme was proposed by utilizing a simple saturable ferrite core in place of the resonant inductance. The principles of the pulse limiting and the simplification of the circuit were performed and the control strategies adopted have been discussed. A new method for establishing the switching function and a feed back method for selecting optimum biasing current, have also been presented. Although a trimming procedure or circulating mode is not used, this system provides stable and good output current regulation in straightforward, simple manner.
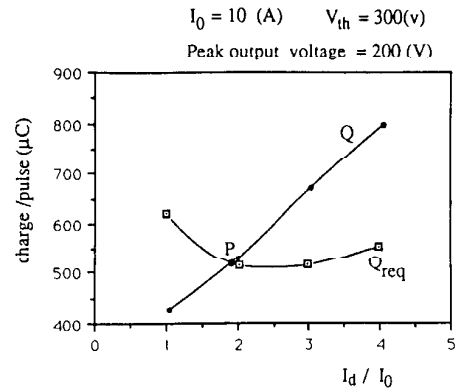
$I_0 = 10$ (A) $V_{th} = 300$(v)

Peak output voltage = 200 (V)

Fig. 8.   Dependencies of Q_{cal} and Q upon I_d.

clipping factor $\frac{I_m}{I_d} = 1.5$ $I_0 = 10$ (A)
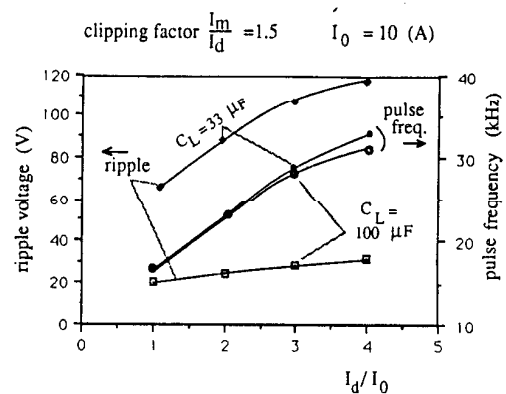
Fig. 9.   Dependencies of ripple voltage
and pulse frequency upon I_d.
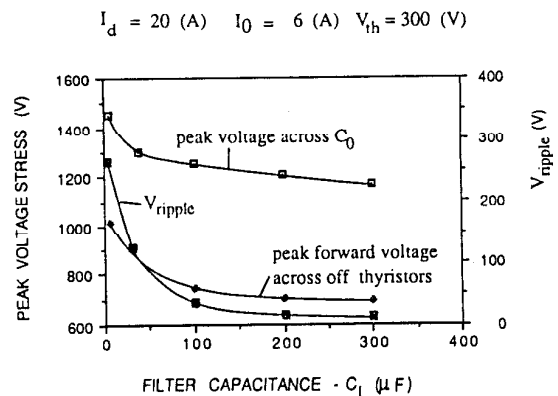
$I_d = 20$ (A) $I_0 = 6$ (A) $V_{th} = 300$ (V)

Fig. 10. Voltage stresses.

REFERENCES

[1] Y. Murai and T. A. Lipo, " High Frequency Series Resonant DC Link Power Conversion," IEEE-IAS Conference Record, 1988, pp., 648-656.

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APPENDIX

Required Charges

As shown in Fig. 6, assuming average currents to flow in all phases simultaneously,

$$I_{as} + I_{bs} + I_{cs} = 0$$

$$\Delta V_{ab} = (I_{as} - I_a - I_{bs} + I_b) \Delta t / C_L$$

$$\Delta V_{cb} = (-I_{bs} + I_b + I_{cs} - I_c) \Delta t / C_L$$

$$\Delta V_{ac} = (- I_{cs} + I_c + I_{as} - I_a) \Delta t / C_L \qquad (8)$$

Defining,

$$I_a \ \Delta t \ = \ \Delta q_a$$
$$I_{as} \ \Delta t \ = \ \Delta q_{as}$$
$$\Delta V_{ab} C_L = \Delta q_{ab} \qquad (9)$$

(similar notations were adopted for other phases)
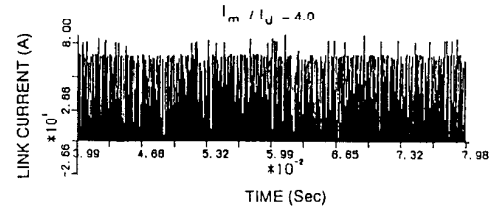
Substituting (9) into (8) and solving for Δq_{as}, Δq_{bs}, Δq_{cs} the following equations are derived.

$$\Delta q_{as} = (\Delta q_{ab} + \Delta q_{ac} - \Delta q_b - \Delta q_c + 2 \Delta q_a) / 3$$
$$\Delta q_{bs} = (- \Delta q_{ab} - \Delta q_{cb} - \Delta q_a - \Delta q_c + 2 \Delta q_b) / 3$$
$$\Delta q_{cs} = (\Delta q_{cb} - \Delta q_{ac} + 2 \Delta q_c - \Delta q_a - \Delta q_b) / 3 \qquad (10)$$
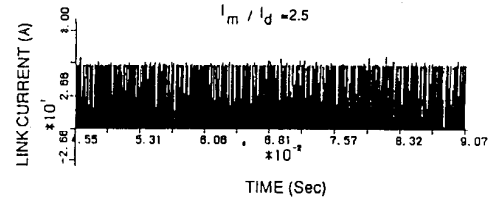
Equation (10) indicates that

$$\Delta q_{as} + \Delta q_{bs} + \Delta q_{cs} = 0 \qquad (11)$$
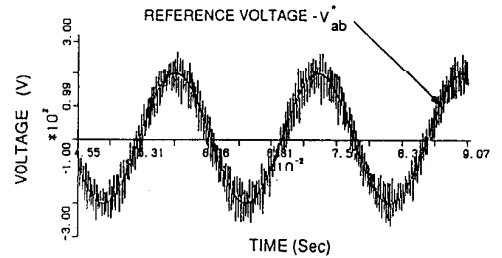
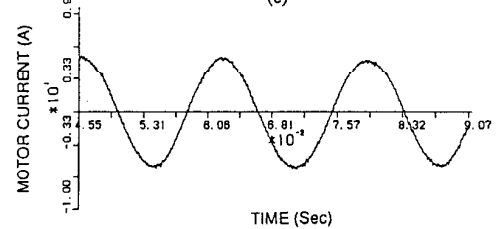and the triggering thyristors can be uniquely defined as shown in the Table 1.

(a)

(b)

(c)

(d)

Fig. 11 Simulated waveforms.