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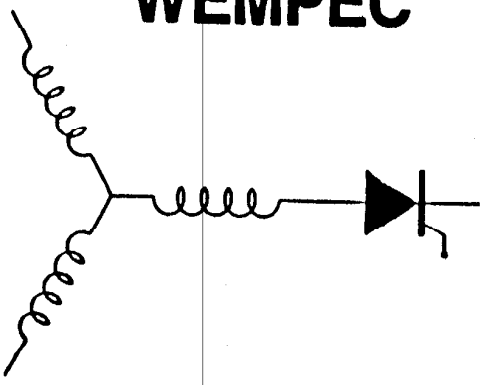

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Abstract

Three phase simultaneous current pulse control for a high frequency series resonant DC link converter was achieved by utilizing a previously developed pulse trimming method and current peak limiting with saturable core. Each resonant pulse is split to flow in three phases almost at a time so that very smooth sinusoidal output current waveform is attained. The duality of the series resonant dc link with the parallel resonant link is discussed. Simulation and the basic experiments are performed.

Introduction

Pulse Width Modulated (PWM) inverters with high frequency switchings are often utilized for driving various speed induction motors to avoid the torque ripple and the acoustic noise, keeping the efficiency high; while in contrary, the switching losses increase and the high efficiency can not be maintained even if high speed switching devices such as FETs and IGBTs are applied. High frequency resonant-link power conversion utilizing zero-volt or zero-current switching has been enormously developed recently. The method features the possibility of having not only a high power density, but also very low switching losses. In a previous paper in 1988, the authors presented a series resonant dc link type ac to ac power conversion scheme as shown in Fig. 1(a) [1]. The converter is a dual of the parallel resonant dc link type in Fig. 1 (b) and the switching occurs at zero current instants [2]. However, the method had such a problem as irregular current peak appearing when the output voltage changes suddenly, while the voltage peak problem happened for the parallel resonant type [3], the solution was an additional circuit with a capacitor and a transistor to limit the voltage [3]. Alternately, the series resonant type had the solution with a simple saturable core to limit the current peaks [4].

The current control ability of the converter is enormously improved in this paper by using pulse-split concept in addition to the current peak limiting circuit [5], the current pulse i_s is distributed to three phases almost at a time, dividing the original pulses at an optimal values such that a smooth current flow is available on the output. This flexible current control feature is essential to drive induction motors in order to reduce torque ripples as PWM inverters have.

Duality of Series Resonant DC Link

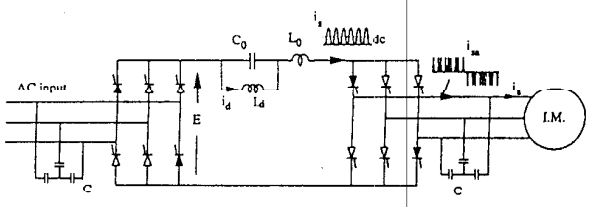
In the series resonant dc link converter in Fig. 1 (a), a series inductance L_0 and a capacitance C_0 form the high frequency resonant circuit and both the three capacitors at the output and at the input are the filters to bypass the high frequency components to maintain the resonant frequency. Parallel inductance L_d superposes the dc current I_d to the high frequency resonating current. In this circuit, for example, the resonating current starts by triggering four thyristors as shown in black; as the average value of the current pulse is equal to the dc current I_d, the adjustment can be done by the input converter although rapid adjustment is difficult because of the large inductance L_d.

Figure 1 (b) shows the parallel resonant dc link converter. The resonance happens between the inductance L_0 and the capacitance C_0, and the dc voltage E_d is superposed by the electrolytic capacitor C_d. This circuit generates high frequency voltage pulses across capacitor C_0 and the pulses are distributed to three phase load.

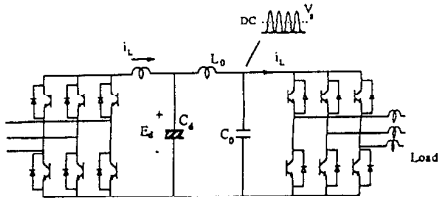
Figs. 2 (a) and (b) in solid line show the basic resonant circuits corresponding to Figs. 1 (a) and (b), respectively. In Fig. 2 (a), the voltage E is the output voltage of the input converter of Fig. 1(a), and thyristor T_h represents four thyristors conducting in series noted in black. When T_h is triggered the current starts to resonate and forms a pulsewise current as shown in Fig. 2 (c). After turning off, the inductance L_d charges up the capacitor C_0 and the thyristor voltage v_{sw} increases linearly. When v_{sw} reaches preset threshold value V_{th}, the thyristor T_h is again triggered to form the next pulse. Thus, the current pulse train is generated. The pulse train i_s is fed to the output filter capacitor C_L keeping the voltage V_L almost constant and the voltage V_L is fed to the load. For three phase load, the circuit should have three capacitors fed by distributing thyristor-bridge as shown in Fig. 1 (a).

Similarly, for the parallel resonant type in Fig. 2 (b), the resonant voltage v_s forms voltage pulse train by switching the transistor T_r. The voltage v_s is fed to flow almost constant current i_L through filter inductance L_L to the load. For three phase operation the parallel resonant circuit needs three inductances and a transistor bridge distributor as shown in Fig. 1 (b).

If the dotted lines with dual elements are drawn in Fig. 2 (b), the circuit becomes almost the same as series resonant circuit in Fig. 2 (a). The only a difference is the connecting point of capacitor C_0 noted as "P". The original connecting point "P" on the ground "G" was changed to "P'" on the source voltage E_{in}; the voltage across the capacitor becomes lower than the case of "P".

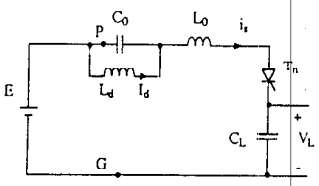


(a) Series resonant dc link converter.

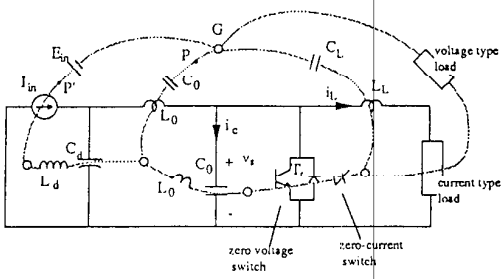


(b) Parallel resonant dc link converter.

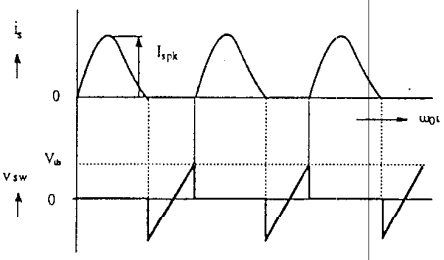
Fig. 1. High frequency resonant dc link ac/ac converter.



(a) series resonant dc link



(b) Parallel resonant dc link



(c) Current pulses of the series resonant dc link.

Fig. 2. Mono-phase equivalent circuits.

Dual-Flow with Current-Peak Limiting

Irregular Current Peaks

In Fig. 2 (a), if both the inductance L_d and the capacitor C_L are assumed sufficiently large and the dc bias current I_d and voltage V_L across the capacitor C_L are constant, the circuit equation becomes,

$$E - v_L = L_0 \frac{di_s}{dt} + \frac{1}{C_0}\int (i_s - I_d)\, dt \qquad (1)$$

and the resulting current i_s is obtained as follows,

$$i_s = I_d (1 - \cos \omega_0 t) + \sqrt{\frac{C_0}{L_0}} V_{sw0} \sin \omega_0 t \qquad (2)$$

where,

$$\omega_0 = \sqrt{\frac{1}{L_0 C_0}}$$

$$V_{sw0} = E - V_{C0} - V_L \ ; \ V_{C0} : \text{initial voltage across } C_0. \qquad (2')$$

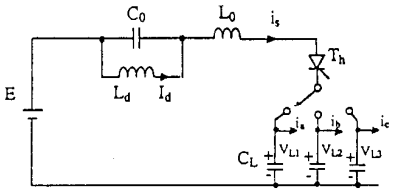
Hence, the peak-value (I_{spk}) of i_s becomes,

$$I_{spk} = I_d + \sqrt{I_d^2 + \frac{C_0}{L_0} V_{sw0}^2} \qquad (3)$$

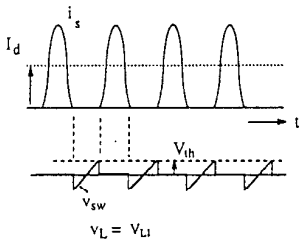
Accordingly, the peak value of i_s is dominated by the dc bias I_d and the initial thyristor voltage V_{sw0}; I_d feeds the main power to the load through i_s, while V_{sw0} feeds the exciting power to the resonating circuit to insure making the thyristors turn off.

The mono-phase equivalent circuit of the series resonant type in Fig. 2 (a) is modified in Fig. 3 (a) to have the function of output distributor, i.e., the three-point selector switch with a diode and with three capacitor C_L's are placed to represent three phase output with different voltages V_{L1}, V_{L2}, and V_{L3}. Depending on the phase selection to distribute i_s, the selector switch selects the corresponding voltage V_L. In Fig. 3 (b), the voltage V_{sw} across thyristor T_h and the current pulses are shown for $V_L = V_{L1}$. During the off state the voltage V_{sw} increases linearly until it reaches the presettled threshold voltage V_{th} (= V_{sw0}). Under the normal operating condition with constant voltage V_L, V_{sw0} is always equal to threshold voltage V_{th} and the current pulses form an uniform pulse train. However, when the selector switches the voltage V_L from low voltage phase ($V_L = V_{L1}$) to higher voltage phase ($V_L = V_{L2}$) because of different phase demand, the V_{sw} often steps by the voltage difference ($V_{L2} - V_{L1}$) considerably beyond V_{th} before triggering T_h, and the resulted high V_{sw0} causes unexpectedly extraordinary high-peak pulse. This process is clearly seen in Fig. 3(c). (the stepped point is noted as P_m and v_{sw} is illustrated in dotted line.)

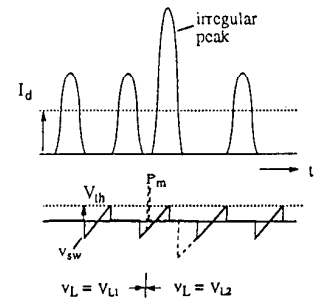
For the parallel resonant type high-peak voltage pulse occurs when the output phase changes because of load current change which is easily understood from the duality of the circuit.



(a) Modified circuit with diferent V_L's



(b) Regular pulses.



(c) Irregular current peak.

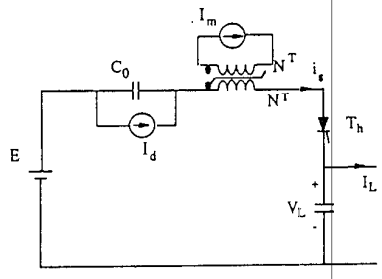
Fig. 3. Generation of irregular peak pulse.

Current peak Limiting with Saturable Core

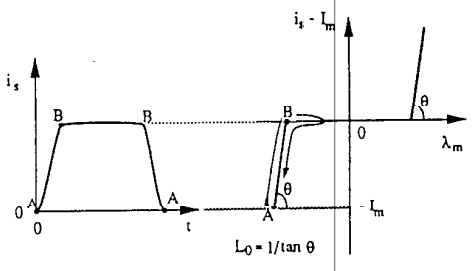
Figure 4 illustrates the basic idea of current peak limiting for this series resonant circuit. In the simplified circuit in Fig. 4 (a), the resonant inductance L_0 is replaced by a saturable reactor (SR) with a biasing current I_m and the dc inductance L_d is represented by a constant current source I_d.

The principle of the current pulse limiting is illustrated in Fig. 4 (b). In the characteristic of magnetizing current $i_s - I_m$ against flux linkage λ_m in figure (b), the gradient of the slope in the saturated region corresponds to the resonant inductance L_0 ($L_0 = 1/\tan\theta$) and the non-saturated region offers very high inductance. The current I_m biases the core of the saturable reactor (= saturable core) in the negative direction to the point "A". When thyristor T_h is triggered current i_s starts flowing and the flux λ_m begins to move from the biased point "A" in saturated region into the unsaturated high inductance zone marked as "B" and the current becomes almost a plateau, suppressed by high inductance and returns to zero again at "A"; the corresponding current wave becomes as shown in the same figure.

For the actual circuit shown in Fig. 5, the magnetizing current I_m is replaced by kI_d using tapped winding with winding ratio $k = n_1/n_2$. The circuit becomes very simple and the magnetizing current $I_m = kI_d$ is automatically adjusted according to the load variations because I_d changes in proportion to the average load current. The preferred value for k is around 2.



(a) Primitive current peak limiting circuit.



(b) Relation between flux λ_m and current i_s.

Fig. 4. Principle of current peak limiting with saturable core.

Combining with Dual-Flow

In Fig. 6 the current peak limiting circuit is combined with pulse-split concept. In figure (a) for instance, three inductances are added in series to the output capacitors to perform the pulse-split, and the resonating current i_s flows along the broken lines if positive currents are required for i_{sa} and i_{sb}. The pulse-split is done by triggering the upper thyristors in the order of phases "a", "b", and "c", while the bottom thyristor in phase "c" should be triggered at the same time as the phase "a" is triggered and being kept in conduction to flow these three currents. The resulting currents are schematically shown in figure (b). After i_{sa} carries the given required amount, i_{sb} is initiated and the required amount for i_{sb} is performed, and the circulating current i_z is initiated after i_{sb}; the required amounts are given from the output voltage errors comparing with references. For this case, phase "c" is used for the circulating purpose, whereas the amount of i_{sc} is automatically satisfied if i_{sa} and i_{sb} are of adequate amounts.

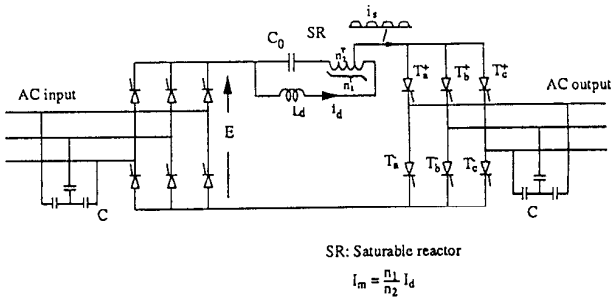
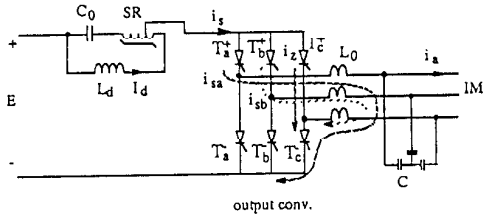
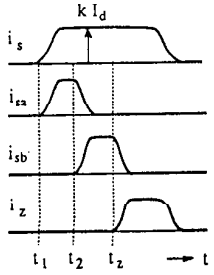


Fig. 5. Circuit configuration with current peak limiting.



(a) Current flow.



(b) Current pulses.

Fig. 6. Principles of pulse splitting.

System Control

Overall system diagram

Fig. 7 shows the overall system diagram. The sensor block samples the output voltages v_{ab}, v_{bc}, v_{ca} and the output control block compares them with sinusoidal reference voltages v_{ab}^*, v_{bc}^*, v_{ca}^*, then decides which thyristors correspond to the first triggering, the second triggering, and the last triggering thyristors as explained in Fig. 6. The delaying angle between the first and the second thyristors is also decided in the control block by using the actual currents sensed by the same block. The control block outputs the timing signals to output converter gate-drive circuit which sends the firing signals to thyristors.

The input converter has the role of controlling both the dc biasing current I_d and the unity power factor in the input at the same time; I_d control is done by using I_d reference I_d^* which is set around twice of the peak output line current, while the unity power factor in the input is done by selecting the thyristors to flow the current pulses to form the sinusoidal current waveforms synchronizing with the signal from the input phases. The sinusoidal current waveform in the input is performed by using Pulse Density Modulation (PDM) technique by synchronizing the waveform with the input phase voltage.

Selection of triggering phase thyristors

In Fig. 8 the selecting procedure of firing thyristor is again illustrated in detail. The selection begins by sensing output line-line voltages v_{ab}, v_{bc}, v_{ca}. Comparing them with reference values v_{ab}^*, v_{bc}^*, and v_{ca}^* the resulted errors ε_{ab}, ε_{bc}, ε_{ca} are compared with each other. The results of comparison are classified into following two cases depending on the polarity of the maximum error phases.

(i) Maximum error is positive:

The bottom thyristor of lower potential phase in maximum error phases and the upper thyristor of second potential phase are selected to be triggered first. For the second triggering thyristor the upper thyristor of the highest potential phase is selected. The opposite side of the bottom thyristor first triggered is triggered last as a circulating mode thyristor.

(ii) Maximum error is negative:

The upper thyristor of higher potential phase in maximum error phases and the bottom thyristor of second potential phase are selected to be triggered first. For the second triggering thyristor the bottom thyristor of the lowest potential phase is selected. The opposite side of the upper thyristor first triggered is triggered last as a circulating mode thyristor.

An example of the selection is schematically shown in Fig. 8 (a) and (b); the negative maximum error case is in figure (a) and the positive maximum error case is in Fig. 8 (b). The corresponding triggering order of the thyristors are shown in the right.

Above selection strictly depends upon the voltages appearing across the selected thyristors; positive polarity voltage is mandatory for the thyristors to be turned on. Fig. 8 contains both two cases in triggering orders of thyristors classified by line voltage relations.

For numerical examples of voltages shown in the parentheses, the current flows for the first and second triggering are noted in dotted line in the order of I and II. (Circulating modes III are not shown.) For other voltage combinations, dual-flow will be degraded to single flow trimming or to non-trimming primitive method.

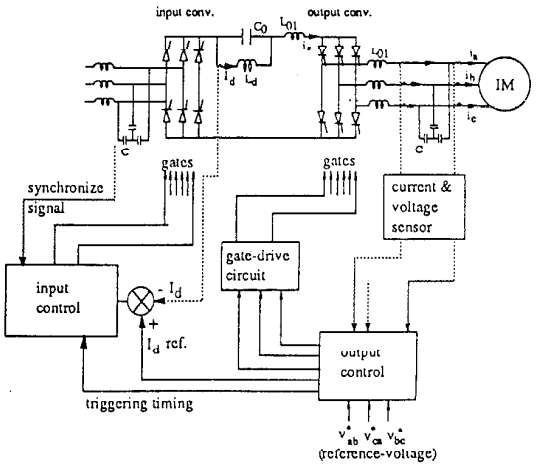
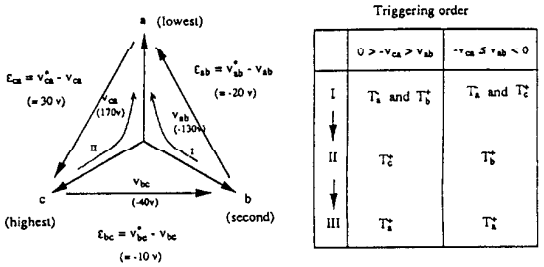
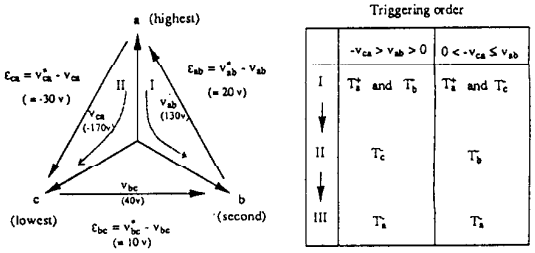


Fig. 7. Control diagram of overall system



(a) Maximum error is positive.



(b) Maximum error is negative.

Fig. 8. Examples of selection of triggering phase thyristors for output converter.

Results and Discussions

Fig. 9 (a) and (b) shows an example of simulated voltage and current waveforms for induction motor drive with the ratings of 60 Hz, 200v, 0.75kw at a operating condition of 60Hz, 160v, slip s = 3.3%. The waveforms in (a) and (b) are satisfactorily sinusoidal and the resulted torque waveform in figure (c) has almost no fluctuations.

Fig. 10 shows a short interval characteristics; currents i_s, i_{sa}, i_{sb}, i_z, and flux linkage λ_m are shown in (a), (b), (c), (d) and (e) respectively. Figure (e) shows the output voltages v_{ab}, v_{bc}, and v_{ca}. Each waveform has regular small ripple and shows smooth variations.

Fig. 11 explains the experimental mono-phase resonant circuit with simple triggering circuit. The triggering pulse is obtained from the opt-coupler when the current i_{op} becomes enough to light LED to activate the photo-transistor. In that figure, when the thyristor T_h is triggered, the current pulse i_s forms resonant waveform. During the off state of the thyristor, the dc inductance charges up the capacitor C_0 and the voltage v_{sw} across T_h also increases. The voltage v_{sw} to light LED is the threshold voltage V_{th}; the adjustment of V_{th} is done by simply adjusting the series resistor R_{op}.

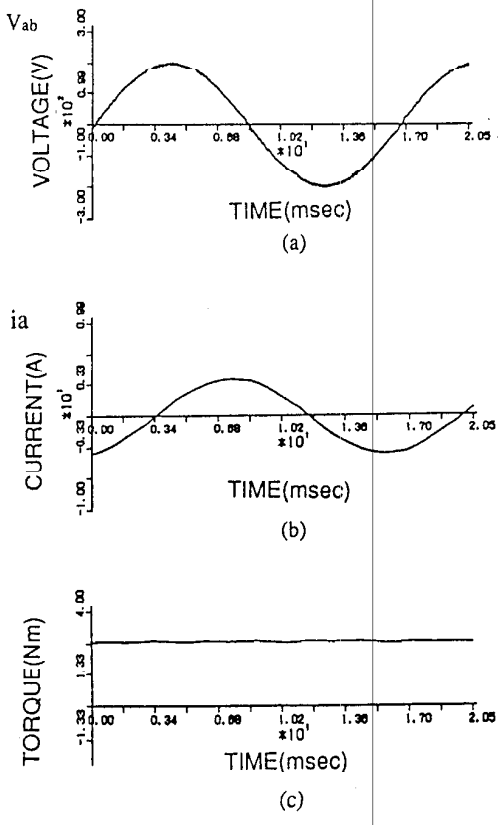


Fig. 9. Simulated output voltages, currents, and torque for three phase operation.

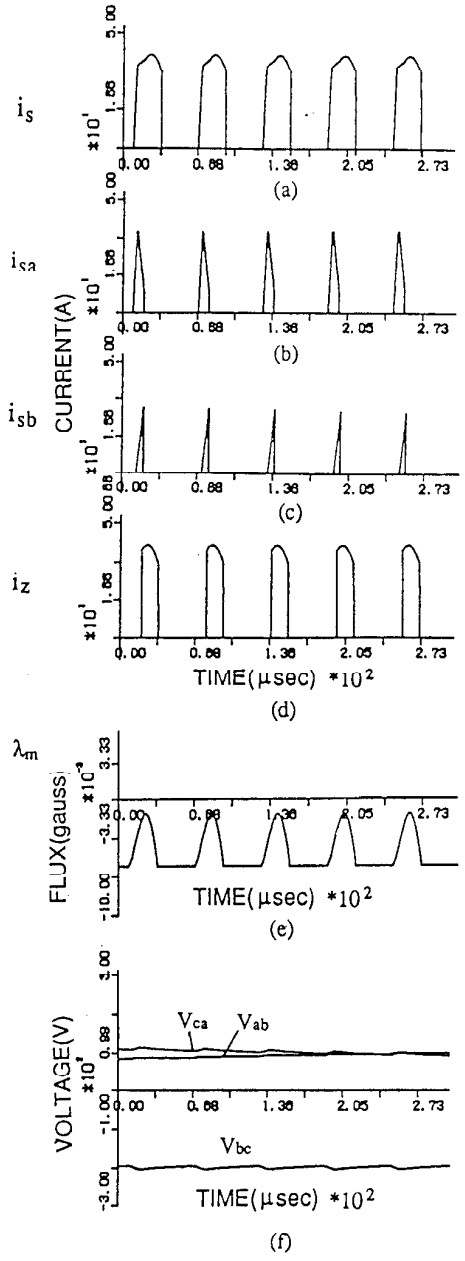


Fig. 10. Current pulses and voltages for Fig. 9.

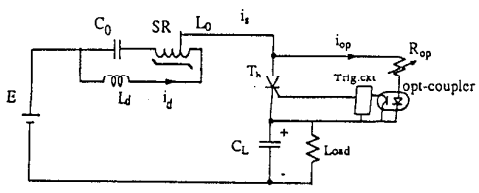


Fig. 11. Experimental circuit and v_{sw} detection.

The experimentally obtained current pulses at winding factor k = 1.2 and 2.2 are shown in Figs. 12 (a) and (b), respectively. For k =1.2, the clamping level is very low and the pulse frequency f_s is as low as 2.1 kHz, whereas for k= 2.2 the clipping level increases and f_s = 13.5 kHz results. As the average current is equal to I_d, the duration interval of zero current becomes less than the case of low clipping level. The waveform involves small overshoot at the beginning of the flat-topped region marked "A" because of parasitic oscillations. The reason why the flat-topped region descends to the right seems to arise from partial saturation of the core.

To apply the triggering circuit to the actual three phase ac/ac circuit in Fig. 7, the resistors and the opto-couplers are only placed at the bottom thyristors of output converter in Fig. 13. After the triggering thyristors are selected as shown in black, all of the thyristors except bottom one are triggered.(T_1, T_2, T_3)are triggered.) Then the total across voltage which is equivalent to v_{sw} at the mono-phase circuit in Fig. 11 appears at the bottom thyristor T_4. When v_{sw} reaches V_{th} the signal from opt-coupler is used to trigger thyristors to perform dual-flow trimming.

For the dual-flow trimming utilized, the condition for the trimming is not always possible to be satisfied. During the actual operation, only 50 percent of the pulses are potential to be dual-flow although the result was better than the case without using dual-flow. For the cases not potential with dual-flow, single flow trimming which utilize the current mode 1 and 3 in Fig. 4(a) was utilized.

For this series resonant circuit the dc biasing inductance and the filter capacitors C_L's should have future consideration for reducing the sizes especially for motor drive in competing with PWM inverters. Higher frequency over 100 kHz seems to be necessary in reducing the sizes and to compete with PWM inverters.

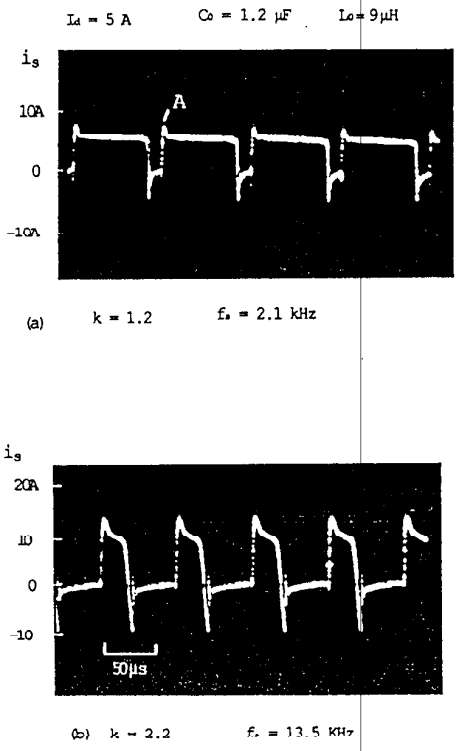


Fig. 12. Experimental results for Fig. 11.
(Tyristor: 600v, 50A, recovery 10μs)

Conclusion

The series resonant dc link converter with dual-flow trimming and current peak limiting function was developed. The performance was satisfactory and the current limiting circuit became very simple and the clamping level is automatically adjusted by the load current.

By using the output voltage reference the series resonant dc link can be easily applicable for induction motor drives and the pulse-split with current limiting scheme seems to be extremely useful to the general purpose ac/ac converters in which the output voltage rating is specified and the current reference is not available. Although the feature is the dual of the parallel resonant type [4] with sinusoidal current reference, the series resonant-type seems to posses pretty wide feasibility for the future industrial use such as PWM general purpose inverters have.

References

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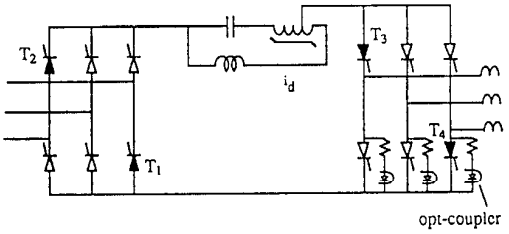

Fig. 13. v_{sw} detection for three phase practical system.