Pulse-Split Concept in Series Resonant DC Link Power Conversion for Induction Motor Drives

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Abstract—**Three phase simultaneous current pulse control for a high frequency series resonant DC link converter was achieved by utilizing a previously developed pulse trimming method and current peak limiting with saturable core. Each resonant pulse is split to flow in three phases almost at the same time so that very smooth sinusoidal output current waveform is attained. The duality of the series resonant dc link with the parallel resonant dc link is discussed. Simulation and the basic experimental results are presented.**

I. Introduction

PULSE Width Modulated (PWM) inverters with high frequency switching are often utilized for driving variable speed induction motors to avoid torque ripple and acoustic noise, and to keep the efficiency high. Unfortunately, on the contrary, the inverter switching losses increase and high system efficiency can not be maintained even if high speed switching devices such as FETs and IGBTs are used. High frequency resonant-link power conversion utilizing zero-voltage or zero-current switching has been enormously developed recently to address this problem. The method features the possibility of having not only a high power density, but also very low switching losses. Previously, the authors presented a series resonant dc link type ac to ac power conversion scheme as shown in Fig. 1(a) [1]. The converter is a dual of the parallel resonant dc link type converter seen in Fig. 1(b), and switching occurs at zero current instants. However, irregular current peaks appear when the output voltage changes suddenly, as similar to voltage peak problem of the parallel resonant converter [2]. The solution for the voltage peak problem was an additional circuit with a capacitor and a transistor to limit the voltage [3]. Alternately, the difficulty with the series resonant type was solved with a simple saturable core to limit the current peaks [4].

The current control ability of the converter is considerably improved in this paper by using pulse-split concept in addition to the current peak limiting circuit [5]. The current pulse is is distributed to three phases almost at the same time, dividing the original pulses at optimal values so that a smooth current flow is available at the output. This flexible current control feature is essential for induction motor drives such as PWM inverters in order to reduce torque ripples.

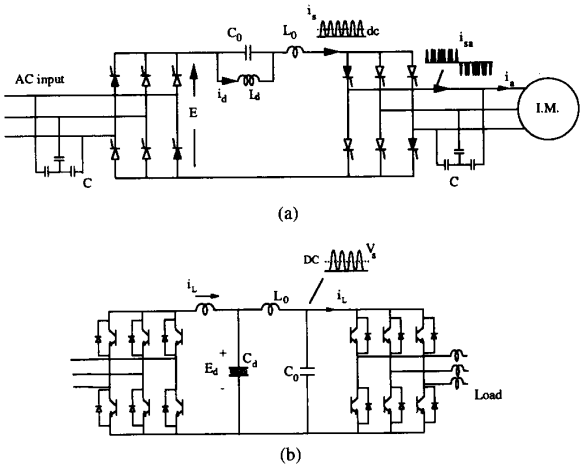

Fig. 1.

II. Duality of Series Resonant DC Link

In the series resonant dc link converter shown in Fig. 1(a), a series inductance L_0 and a capacitance C_0 form the high frequency resonant circuit and the three capacitors both at the output and at the input are the filters to bypass the high frequency components to maintain the resonant frequency. Parallel inductance L_d superposes the dc current I_d to the high frequency resonance current. In this circuit, for example, the resonance current pulse is started by triggering four thyristors as shown in black. As the average value of the current pulse is equal to the dc current I_d, the adjustment can be done by the input converter although rapid adjustment is difficult because of the large inductance L_d.

Figure 1(b) shows the parallel resonant dc link converter. Resonance occurs between the inductance L_0 and the capacitance C_0, and the dc voltage E_d is superposed by the electrolytic capacitor C_d. This circuit generates high frequency voltage pulses across capacitor C_0 and the pulses are distributed to a three phase load.

The solid lines in Figs. 2(a) and (b) show the basic resonant circuits corresponding to Figs. 1(a) and (b), respectively. In Fig. 2(a), the voltage E is the output voltage of the input converter of Fig. 1(a), and thyristor T_h represents four

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thyristors conducting in series noted in black. When T_h is triggered the current starts to resonate and forms a current pulse as shown in Fig. 2(c). After the turn-off of the switches, the inductance L_d starts charging up the capacitor C_0 and the thyristor voltage v_{sw} increases linearly. When v_{sw} reaches preset threshold value V_{th}, the thyristor T_h is again triggered to form the next pulse. Thus, a current pulse train is generated. The pulse train i_s is fed to the output filter capacitor C_L keeping the voltage V_L almost constant, and the voltage V_L is fed to the load. For a three phase load, the circuit should have three capacitors fed by a distributing thyristor-bridge as shown in Fig. 1(a).

Similarly, for the parallel resonant type in Fig. 2(b), the resonant voltage v_s forms a voltage pulse train by switching the transistor T_r. The voltage v_s allows almost constant current i_L through filter inductance L_L to the load. For three phase operation the parallel resonant circuit needs three inductances and a transistor bridge distributor as shown in Fig. 1(b).

If the dotted lines with dual elements are drawn in Fig. 2 (b), the circuit becomes almost the same as the series resonant circuit in Fig. 2(a). The only difference is the connecting point of capacitor C_0 noted as P. The original connecting point P on the ground G was changed to P' on the source voltage E_{in}, and the voltage across the capacitor becomes lower than that in the case of P.

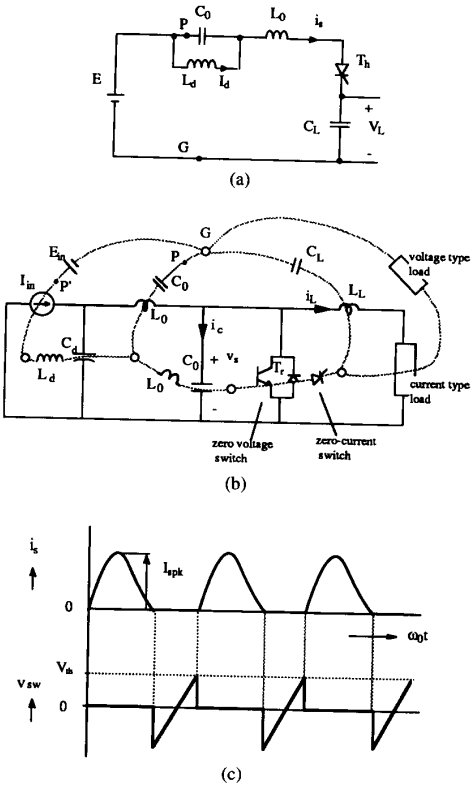

Fig. 2.

III. Dual-Flow with Current-Peak Limiting

A. Irregular Current Peaks

If it is assumed that the inductance L_d and the capacitor C_L seen in Fig. 2(a) are sufficiently large, and that the dc bias current I_d and voltage V_L across the capacitor C_L are constant during one resonant pulse, the circuit equation becomes,

$$E - V_L = L_0 \frac{di_s}{dt} + \frac{1}{C_0} \int (i_s - I_d)\, dt \tag{1}$$

and the resulting current is i_s obtained as follows,

$$i_s = I_d(1 - \cos \omega_0 t) + \sqrt{\frac{C_0}{L_0}} V_{sw0} \sin \omega_0 t \tag{2a}$$

where,

$$\omega_0 = \sqrt{\frac{1}{L_0 C_0}}$$
$$V_{sw0} = E - V_{C0} - V_L; V_{C0}\text{: initial voltage across } C_0. \tag{2b}$$

Hence, the peak-value (I_{spk}) of i_s becomes,

$$I_{spk} = I_d + \sqrt{I_d^2 + \frac{C_0}{L_0} V_{sw}^2 0}. \tag{3}$$

Accordingly, the peak value of i_s is determined by the dc bias current I_d and the initial thyristor voltage V_{sw0}. I_d feeds the main power to the load through i_s, while V_{sw0} feeds the exciting power to the resonating circuit to insure the thyristors turn off.

The monophase equivalent circuit of the series resonant converter in Fig. 2(a) is modified in Fig. 3(a) to include the function of output distributor, i.e., the three-point selector switch with a diode and with three capacitors placed to represent three phase output with different voltages V_{L1}, V_{L2}, and V_{L3}. Depending on the phase selection to distribute i_s, the selector switch selects the corresponding voltage V_L. In Fig. 3(b), the voltage V_{sw} across thyristor T_h and the current pulses are shown for $V_L = V_{L1}$. During the off state, the voltage V_{sw} increases linearly until it reaches the preset threshold voltage $V_{th}(= V_{sw0})$. Under the normal operating condition with constant voltage V_L, V_{sw0} is always equal to threshold voltage V_{th} and the current pulses form a uniform pulse train. However, when the selector switches the voltage V_L from low voltage phase ($V_L = V_{L1}$) to higher voltage phase ($V_L = V_{L2}$) because of different phase demand, the V_{sw} often steps up by the voltage difference ($V_{L2} - V_{L1}$) considerably beyond V_{th} before triggering T_h, and this high V_{sw0} causes an extraordinary high-peak pulse. This process is clearly seen in Fig. 3(c). (The steping point is noted as P_m and v_{sw} is illustrated in dotted line.)

For the parallel resonant type, a high-peak voltage pulse occurs when the output phase changes because of load current change which can be easily understood from the duality of the circuit.

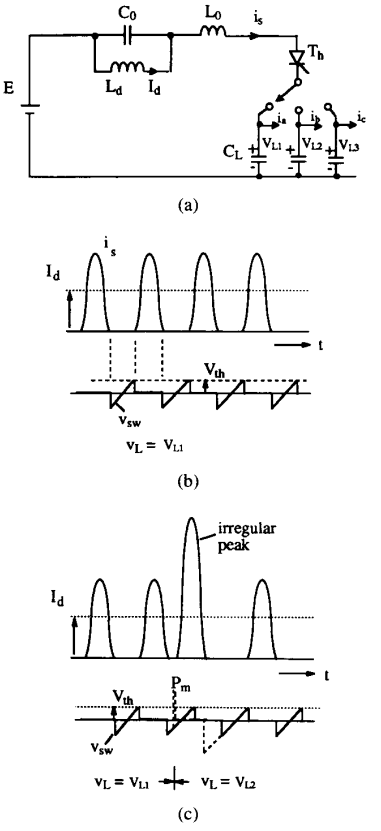

Fig. 3.

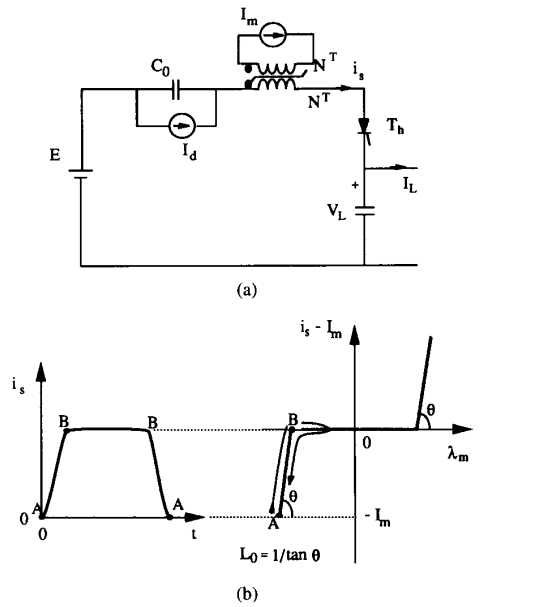

Fig. 4.

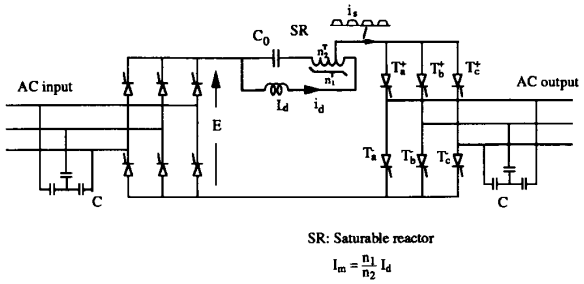

Fig. 5.

B. Current Peak Limiting with Saturable Core

Figure 4 illustrates the basic idea of current peak limiting for this series resonant circuit. In the simplified circuit in Fig. 4(a), the resonant inductance L_0 is replaced by a saturable reactor (SR) with a biasing current I_m, and the dc inductance L_d is represented by a constant current source I_d.

The principle of the current pulse limiting is illustrated in Fig. 4(b). In the characteristic of magnetizing current $i_s - I_m$ versus flux linkage λ_m in Fig. 4(b), the slope in the saturated region corresponds to the resonant inductance $L_0(L_0 = 1/\tan\theta)$ and the non-saturated region offers very high inductance. The current I_m biases the core of the saturable reactor (saturable core) in the negative direction to the point "A". When thyristor Th is triggered current i_s starts flowing and the flux λ_m begins to move from the biased point "A" in saturated region into the unsaturated high inductance zone marked as "B" and the current becomes almost a plateau, suppressed by high inductance and returns to zero again at "A". The corresponding current waveform is also shown in the same figure.

For the actual circuit shown in Fig. 5, the magnetizing current I_m is replaced by kI_d using a tapped winding with winding ratio $k = n_1/n_2$. The circuit becomes very simple and the magnetizing current $I_m = kI_d$ is automatically adjusted according to the load variations since I_d changes in proportion to the average load current. The preferred value for k is around 2.

C. Combining with Dual-Flow

In Fig. 6 the current peak limiting circuit is combined with pulse-split concept. In Fig. 6(a) for instance, three inductances are added in series to the output capacitors to perform the pulse-split, and the resonating current i_s flows along the broken lines if positive currents are required for i_{sa} and i_{sb}. The pulse-split is done by triggering the upper thyristors in the order of phases "a", "b", and "c", while the bottom thyristor in phase "c" should be triggered at the same time as the phase "a" is triggered, and kept in conduction to flow these three currents. The resulting currents are schematically shown in Fig. 6(b). After phase "a" carries the current (i_{sa}) for required time, i_{sb} is initiated and carried for required amount of time. Finally, the circulating current i_z is initiated after i_{sb}. The required time amounts for phase currents are calculated by comparing the output voltages with references. For the given case, phase "c" is used for the circulating purpose, and the

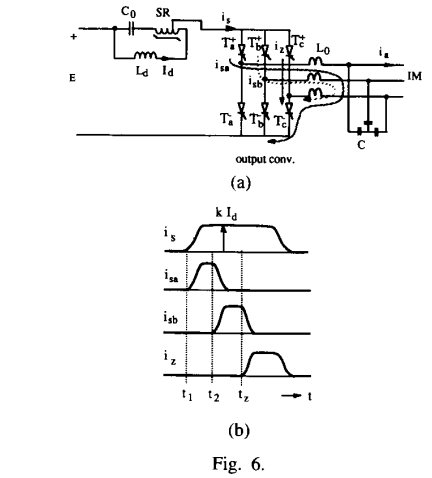

Fig. 6.

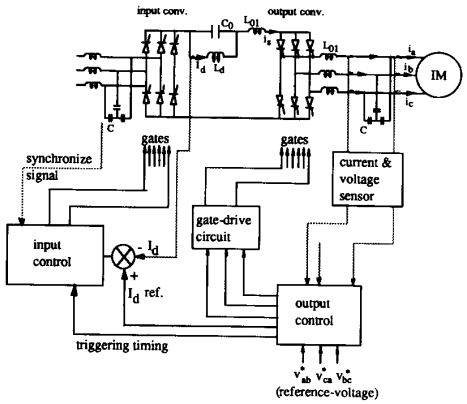

Fig. 7.

pulse width of i_{sc} is automatically satisfied if i_{sa} and i_{sb} are of adequate length.

IV. System Control

A. Overall System Diagram

Fig. 7 shows the overall system diagram. The sensor block samples the output voltages v_{ab}, v_{bc}, v_{ca} and the output control block compares them with sinusoidal reference voltages $v^*_{ab}, v^*_{bc}, v^*_{ca}$, then decides which thyristors correspond to the first triggering, the second triggering, and the last triggering thyristors as explained in Fig. 6. The delay angle between the first and the second thyristors is also decided in the control block by using the actual currents sensed by the same block. The control block outputs the timing signals to output converter gate-drive circuit which sends the firing signals to thyristors.

The input converter has the role of controlling the dc bias current I_d and achieving unity power factor in the input at the same time. I_d control is done by using an I_d reference I^*_d which is set to around twice of the peak output line current, while the unity power factor in the input is achieved

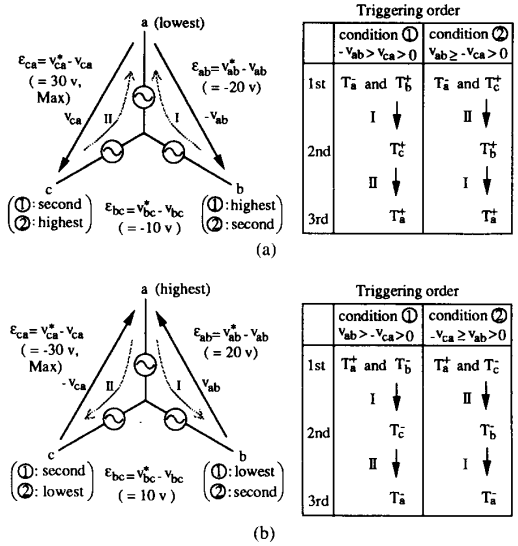

Fig. 8.

by selecting the thyristors to flow the current pulses to form sinusoidal current waveforms synchronized with the input voltage waveforms. The selection of the input side thyristors for unity power factor operation is done by using the Pulse Density Modulation (PDM) technique.

B. Selection of Triggering Phase Thyristors

In Fig. 8 the selection procedure for the firing thyristor is again illustrated in detail. The selection begins by sensing output line-line voltages v_{ab}, v_{bc}, v_{ca}. Three phase voltage errors $\varepsilon_{ab}, \varepsilon_{bc}, \varepsilon_{ca}$ are computed by comparing these voltages with teh reference values v^*_{ab}, v^*_{bc}, and v^*_{ca}, and then these errors are compared with each other. The results of the comparison are classified into the following two cases depending on the polarity of the maximum error phases.

(i) Maximum error is positive: The bottom thyristor of lowest potential phase in the maximum error phases and the upper thyristor of second highest potential phase are selected to be triggered first. The upper thyristor of the highest potential phase is selected to be turned on next. The opposite side of the bottom thyristor that was turned on first is triggered last as a circulating mode thyristor.

(ii) Maximum error is negative: The upper thyristor of higher potential phase in the maximum error phases and the bottom thyristor of second lowest potential phase are selected to be triggered first. The bottom thyristor of the lowest potential phase is selected to be turned on next. The opposite side of the upper thyristor that was turned on first is triggered last as a circulating mode thyristor.

An example of the selection is schematically shown in Fig. 8. Fig. 8(a) shows the positive maximum error case and Fig. 8(b) shows the negative maximum error case. The corresponding triggering order of the thyristors are also given.

The selection mentioned above strictly depends upon the voltages appearing across the selected thyristors to be turned

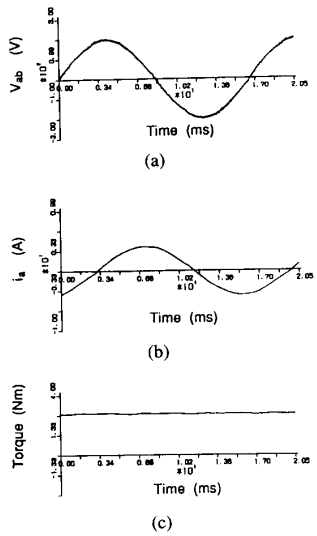

Fig. 9.

on. Fig. 8 demonstrates both cases that are possible in triggering orders of thyristors classified by line voltage relations.

For the numerical voltage values shown in the parentheses, the current flows for the first and second triggerings are noted in dotted line in the order of I and II. (circulating mode III is not shown.) For other voltage combinations, dual-flow will be degraded to single flow trimming or to primitive non-trimming method.

V. Results and Discussions

Figs. 9(a) and 9(b) show an example of simulated voltage and current waveforms for induction motor drive with the ratings of 60 Hz, 200 V, 0.75 kW at an operating condition of 60 Hz, 160 V, slip $s = 3.3\%$. The waveforms in (a) and (b) are satisfactorily sinusoidal and the resulted torque waveform in Fig. 9(c) has almost no fluctuations.

Fig. 10 shows a short interval of characteristics. Currents i_s, i_{sa}, i_{sb}, i_z, and flux linkage λ_m are shown in (a), (b), (c), (d) and (e) respectively. Figure 10(e) shows the output voltages v_{ab}, v_{bc}, and v_{ca}. Each waveform has regular small ripple and shows smooth variations.

Fig. 11 explains the experimental mono-phase resonant circuit with simple triggering circuit. The triggering pulse is obtained from the opto-coupler when the current $i_{\rm op}$ becomes big enough to light the LED that activates the photo-transistor. In that figure, when the thyristor T_h is triggered, the resonant current pulse i_s is formed. During the off state of the thyristor, the dc inductance charges up the capacitor C_0, and the voltage $v_{\rm sw}$ across T_h also increases. The voltage $v_{\rm sw}$ to light the LED is the threshold voltage $V_{\rm th}$, and the adjustment of $V_{\rm th}$ is done by simply adjusting the series resistor $R_{\rm op}$.

The experimentally obtained current pulses for winding factors k = 1.2 and 2.2 are shown in Figs. 12 (a) and (b), respectively. For k =1.2, the clamping level is very low and the pulse frequency f_s is as low as 2.1 kHz, whereas for k = 2.2 the clipping level increases and f_s = 13.5 kHz is obtained.

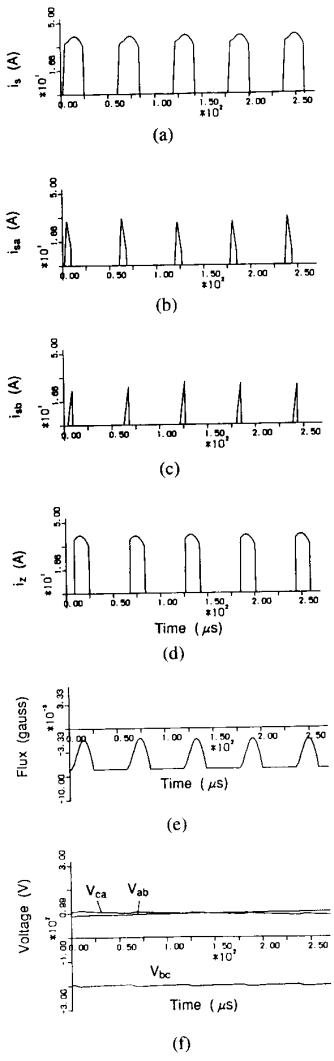

Fig. 10.

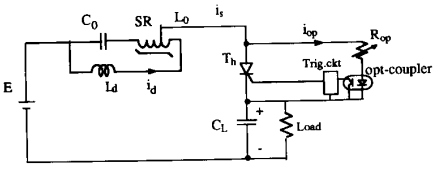

Fig. 11.

As the average value of the resonant current is equal to I_d, the zero current interval becomes less than the case of low clipping level. The waveform involves a small overshoot at the beginning of the flat-topped region marked "A" because of parasitic oscillations. The reason why the flat-topped region descends to the right and seems to arise from partial saturation of the core.

To apply the triggering circuit to the actual three phase ac/ac circuit in Fig. 7, the resistors and the opto-couplers are only

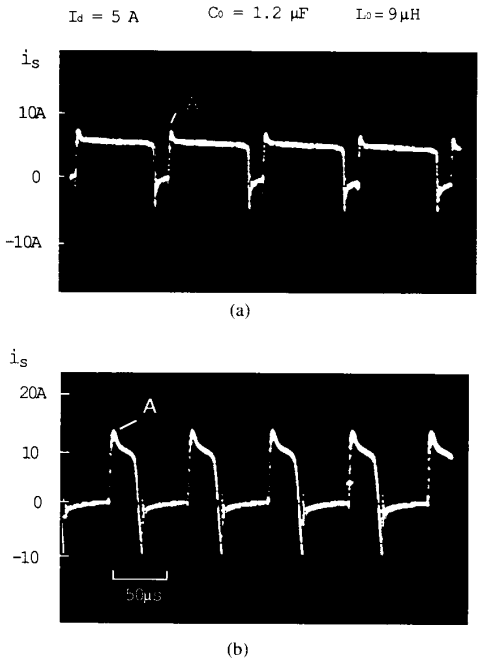

Fig. 12.

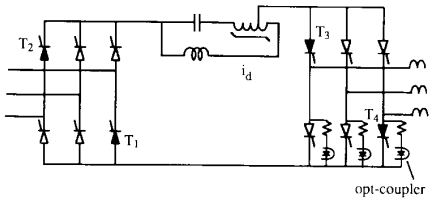

Fig. 13.

placed at the bottom thyristors of output converter in Fig. 13. After the triggering thyristors are selected as shown in black, all of the thyristors except the bottom one are triggered. (T_1, T_2, T_3 are triggered.) Then the total voltage which is equivalent to vsw at the mono-phase circuit in Fig. 11 appears across the bottom thyristor T_4. When v_{sw} reaches V_{th}, the signal from an opto-coupler is used to trigger thyristors to perform dual-flow trimming.

For the dual-flow trimming utilized, the condition for the trimming is not always possible to be satisfied. During the actual operation, only 50 percent of the pulses are potentially capable of dual-flow although the result was still much better than the case without using the dual-flow technique. For the cases where dual-flow is not possible, single flow trimming which utilizes the current mode 1 and 3 in Fig. 4(a) can be used.

For this series resonant circuit the dc biasing inductance and the filter capacitor C_L should have future consideration for size reduction, especially for motor drives to compete with PWM inverters. Higher frequency over 100 kHz seems to be necessary in reducing the filter sizes and to compete with cpnventional PWM inverters.

VI. Conclusion

The series resonant dc link converter with dual-flow trimming and current peak limiting function was developed. The performance was satisfactory and the current limiting circuit became was shown to be very simple. Automatic adjustment of the clamping level by the load current was achieved.

By using the output voltage reference, the series resonant dc link can be readily applied to induction motor drives. The pulse-split with current limiting scheme seems to be extremely useful to for general purpose ac/ac converters in which the output voltage rating is specified and the current reference is not available. Although the feature is the dual of the parallel resonant type [4] with sinusoidal current reference, the series resonant-type also appears to be promising for future industrial use.

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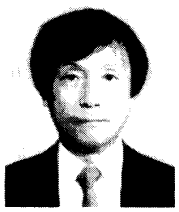

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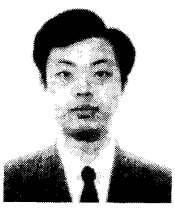

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