The College of Engineering
University of Wisconsin-Madison

Wisconsin Electric Machines and Power Electronics Consortium

RESEARCH REPORT
92-6

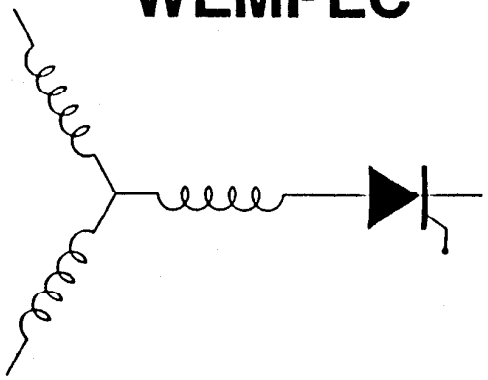
Soft Switched Notching Current Source Inverters

T. A. Lipo
Dept. of Elec. and Comp. Engr.
University of Wisconsin-Madison
1415 Johnson Drive
Madison, WI 53706

E. da Silva
Fed. University of Paraiba
Caixa Postal 15
51800 Campina Grande
PB Brazil

G. Ledwich
Univ. of Queensland
Brisbane, Australia
4072

WEMPEC



Department of Electrical and Computer Engineering
1415 Johnson Drive
Madison, Wisconsin 53706

SOFT SWITCHED NOTCHING CURRENT SOURCE INVERTERS

G. Ledwich
University of Queensland
Brisbane Australia 4072

E. Da Silva
Federal University of Paraiba
Caixa Postal 15
51800 Campina Grande PB Brazil

T.A. Lipo
University of Wisconsin-Madison
1415 Johnson Drive
Madison WI 53706

ABSTRACT

An improved soft switched current source converter structure is reported in this paper. An evolution of possible forms is presented and the operation of the circuit explained. A simulation study illustrates the quality of closed loop modulation in synthesizing a three phase sinusoidal voltage under the soft switching constraints. An evaluation of the loss mechanisms in this structure is performed and the relative loss terms compared for a particular high power thyristor. The primary disadvantage of the circuit are the voltage stresses which are appreciably higher than line to line voltage but are roughly the same as that of current proposed soft switched CSI systems.

INTRODUCTION

The use of GTO based hard switched current source inverters such as in [1] has extended PWM modulation to the current source field, removing most of the limitations of auto-sequential current source inverters. However, since such converters switches must turn-off a substantial current, switching losses of the devices limit the frequencies at which such converters can be modulated. For GTO based inverters, this switch loss can be comparable to its significant conduction losses. Recently, soft switching techniques have been demonstrated to be helpful in reducing the switching losses of such inverters [2]. The resonant link DC converter as in [3] periodically produces a zero current in the inverter; at this time the switch configuration can be changed arbitrarily with little switching loss. The CSI system in [4] also produces the soft PWM transfer but at the overhead of 24 extra devices in the total converter . In this paper a circuit is examined which has only 4 extra switches over the hard switched version and can be implemented using thyristors or GTOs. The switching commutation time and voltage ratings are roughly half that of the resonant DC link in [2].

NOTCHING INVERTER EVOLUTION

Basic operation

The basic operating features of the proposed circuit can be explained by reference to Fig. 1. In Fig. 1 the left hand series resonant circuit diverts the link current from the output inverter by firing T_{a1}. If the peak line to line voltage on the input and output is denoted as V_p, the commutation voltage can be expressed as $(1+k)V_p$. The capacitor C_{a1} is initially charged to $-(1+k)V_p$. This voltage will reverse bias any possible conducting pair in the output. The link current I_d now diverts to the notching circuit and the voltage ramps until $(1+k)V_p$ which is higher than any possible incoming switch pair voltage. When the inverter thyristors fire, T_{a1} is reverse biased and turns off. Thyristor T_{a2} is used to reverse the voltage on C_{a1} to its initial value. In addition to resonating with the capacitor C_{a1} to reverse its voltage, the series inductor L_{c1} is also necessary to limit di/dt when the incoming switches are in a NULL state. That is, if both a+ and a- switches are fired, the only loop inductance is L_{c1}.

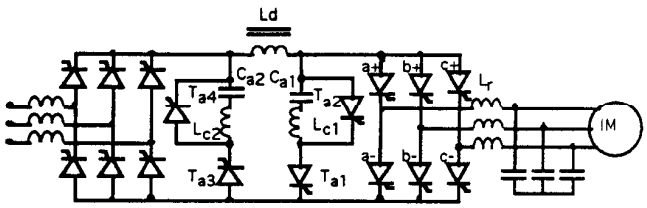


Figure 1. Self resonant notching converter.

Commutation of the input bridge is possible in an equivalent manner by firing T_{a3}, with C_{a2} initially charged to $(1+k)V_p$.

Natural Commutation

It is important to note that it is not necessary to use the previously described mode of resonant commutation if the sequence of required output phases e.g.. AB AC AA, constitute a monotonic increasing voltage sequence. Here, the notation AB refers to current flow into the a+ switch and returning via b-. For the conversion from state AB to AC if C phase voltage is sufficiently lower than B, firing of c- will reverse bias b- and inherently turn it off, thus completing the transfer. For each switching cycle the required duration for each state must be computed at the beginning of the switch cycle and then the states are ordered as a decreasing sequence. Any state of zero duration is simply eliminated from the sequence. In general each cycle

will have one resonant transfer to commence the cycle and two natural transfers between each resonant transfer. In the case where the line voltages are too close to guarantee reliable natural commutation within a reasonable time, an additional resonant transfer is required for that cycle. As in [2] the zero current "lossless" transfer can be achieved using only three output line inductors sized to give an acceptable di/dt.

Modulation Pattern

The modulation pattern for the current source structure is based on the same space vector modulation hexagon as previously given in [5]. If it is desired to synthesize three currents comprising I_{ra}, I_{rb}, I_{rc} in the sector bounded by AB AC and the center NULL state the appropriate duty ratio is given in [5] as I_{rb}/I_d and I_{rc}/I_d for states AB and AC respectively. The NULL state AA is then of duty ratio $1-I_{rb}/I_d-I_{rc}/I_d$. If the desired current changes sector, the new switch pattern can be established during the resonant state when no current is flowing in the inverter.

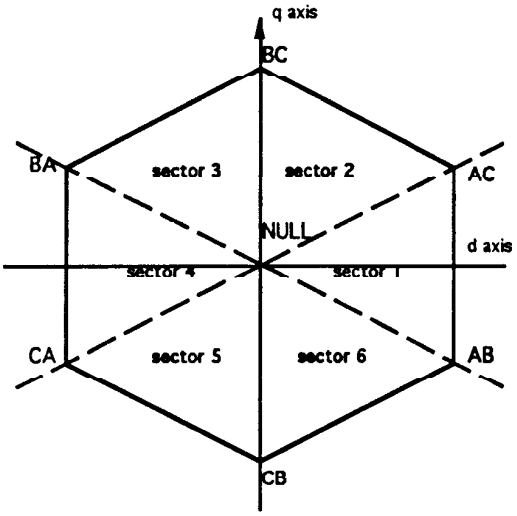


Figure 2 Space vector description for CSI. modulation.

Circuit Simplifications

Since the commutation circuit is used only once per switch cycle it should be observed that it is possible to have the one circuit alternately commutating the input and output bridge. In this case the thyristor controls appear as before but the passive components are shared. If there is complete alternation between the converter side commutations there is no need to have a reversal circuit and thyristors T_{a1} and T_{a2} can be eliminated.

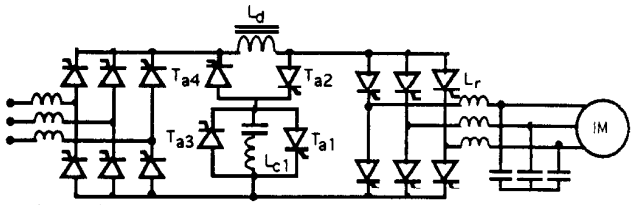


Figure 3 Notching converter with shared notching circuit.

The occasional additional resonant transfer to accommodate low voltage differences will made it difficult to ensure that the commutating voltage is of the correct polarity at the required time when one of the two bridges requests a transfer. For this reason thyristors T_{a1} and T_{a2} are retained but need only used when a low voltage transfer is anticipated.

One of the limitations of the circuit is that a large capacitor is required in the commutation circuit to achieve the necessary reverse bias time T_q, but a small value is preferred for the time to slew between $-(1+k)V_p$ and $(1+k)V_p$. For an overvoltage factor k=0.7 the slew time is, for example, $5T_q$. As there is effectively no output current during this interval it is desirable to reduce this time as much as possible. In Fig. 4 the commutation components have been rearranged for this purpose. In this case, once the inverter is commutated off and the capacitor is at $-V_p$, the slewing thyristor T_{a2} is fired to create more current in the capacitor thereby greatly speeding the transfer of current to about $2.5T_q$.

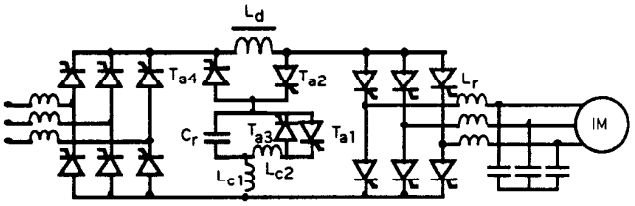


Figure 4 Fast slewing notching converter.

The long reverse recovery time and fast slew time of the commutating capacitor voltage C_r (V(4)), the corresponding current I_{Cr} (ICAPR) and the resulting input current (I0 - dc link side current) are shown in Fig. 5. One can observe the fast commutation turn-off and slower turn-on commutation of I_o. This feature is due to the fact that, at this particular point of the sine wave during which commutation occurs, the inverter voltage being commutated off is zero giving a commutation voltage of $[(1+k)V_p]$, and the voltage of the phases being turned on is close to V_p

giving a commutation voltage of kV_p and a longer transition.

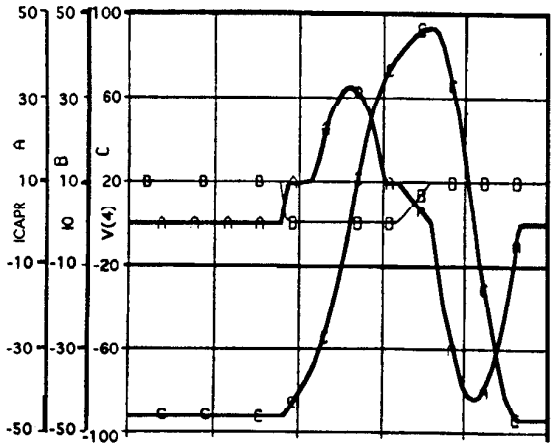


Fig. 5 Current link commutation waveforms.

SIMULATION RESULTS

In order to demonstrate how ordering and notching can produce useful PWM output from a CSI inverter, the output side inverter was simulated with the computer language ACSL. The line current and output voltage for the proportional closed loop voltage controlled inverter are shown in Figs. 6 and 7 respectively. The initial transient is due to the need for establishing the desired voltage and persists for 2mS.

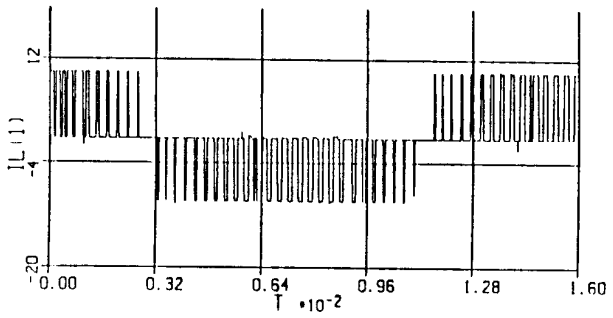


Figure 6 Line current of notching inverter.

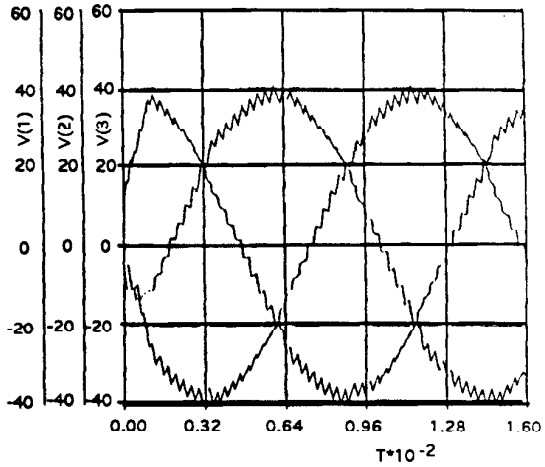


Figure 7 Output voltage of notching inverter.

EXPERIMENTAL RESULTS

The circuit shown in Fig. 8 was used to test the concept of notching with thyristor switching elements. The devices chosen for the test had a reverse recovery time of 11 μs but were operated as if the devices had a reverse recovery time in the range of 20 to 30 μs. The link current was controlled by a dc power supply and series inductor. The thyristor T1 in Fig. 8 and the load with freewheeling diode represent the main inverter elements. The notch was initiated by firing T2. The firing of the slew assist thyristor T4 and reset thyristor T3 are controlled by voltage comparators. The current to T1, voltage across T1 and the capacitor voltage are plotted in Fig. 9 for the case of no slew assist. The corresponding slew assist results are given in Fig. 10. It can be noted that the resonant losses for this test circuit are responsible for the swing of capacitor voltage to negative voltage which does not match its positive starting point. The slew assist circuit is seen to be highly effective in significantly reducing the slew time of the converter.

LOSSES IN THE NOTCHING INVERTER

The losses in the soft switching inverter consist of conduction losses for the main devices as well as the commutating switches. In addition to these losses there is a finite dv/dt for the thyristors which requires the use of snubbers and their associated lossy elements. Reverse recovery of the switches causes losses both in resonant transfer as well as during natural commutation. The analysis proceeds by neglecting the occasional additional resonant transfer and assumes one resonant and two natural

commutations in the switching cycle at frequency f_s. In this analysis the losses for the output side of the converter are computed first and then the losses are doubled to account for both converters.

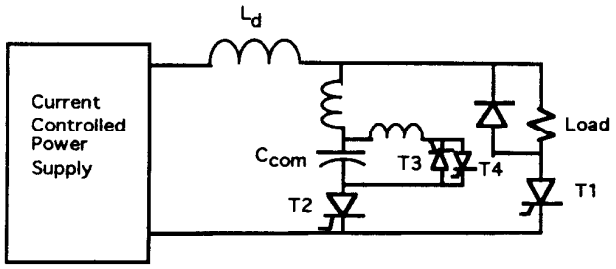


Figure 8 Test circuit for notching of DC current link.

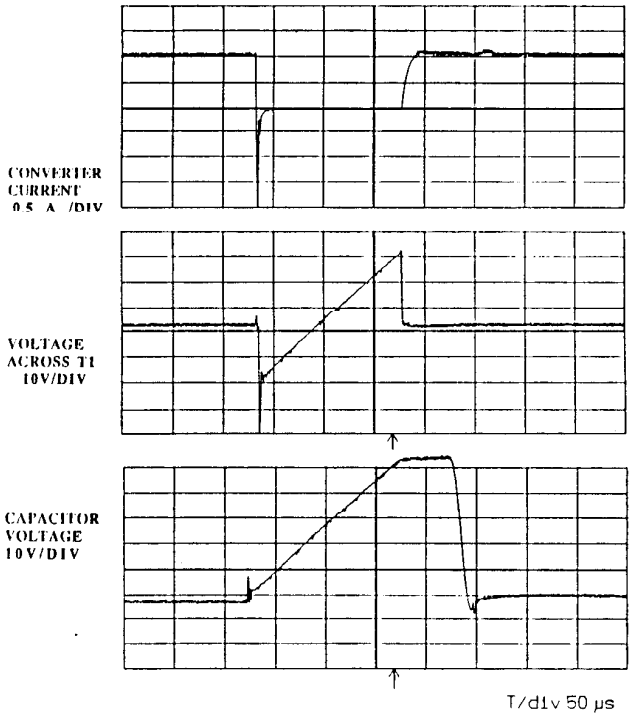


Fig. 9 Notched current, capacitor voltage and reverse voltage with basic notching circuit.

If the notch time from the turn-off commutation until the next device switches on is called T_n, the conduction loss for the main switches is found by considering two switches to be on at any one time with a link current I_d and consequent device drop of V_d for a fraction $(1 - T_n f_s)$ of the interval T_n. In addition, the link

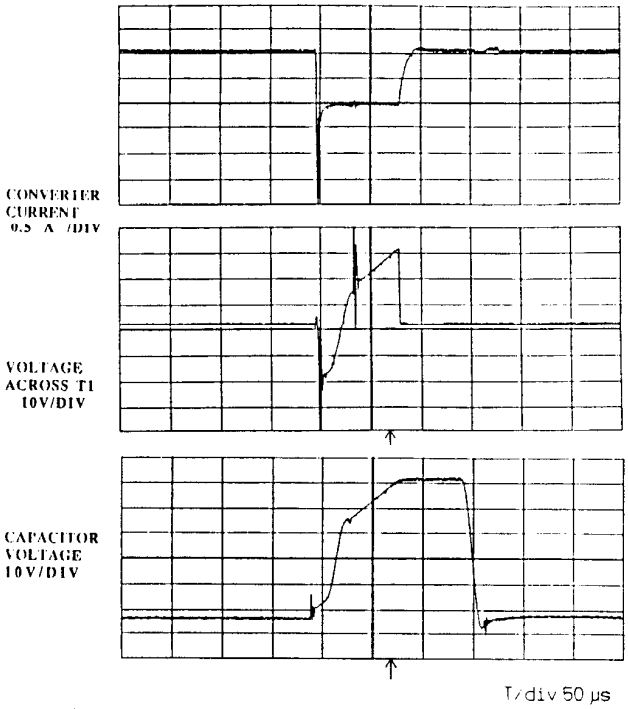


Fig. 10 Converter current, thyristor voltage and capacitor voltage waveforms with the use of slew assisted commutation.

thyristor carries I_d for the remainder of the time giving, for conduction loss,

$$\textit{Conduction Loss} = 2\,V_d\,I_d\,(1-T_{II}\,f_s) + V_d\,I_d(T_{II}\,f_s) \quad (1)$$

If the slew assist time is bT_q, then the total commutation notch time is $2T_q + bT_q$. This observation specifies that the average current in the slew assist period from V_p to $-V_p$ is

$$I_{av} = \frac{2C_T V_p}{bT_q} \quad (2)$$

Knowing the link current I_d is already flowing, the peak of the half sine wave assist current is

$$I_{peak\ res} = \frac{\pi}{2}(I_{av} - I_d) \quad (3)$$

The loss per switch cycle in the assist thyristor is therefore,

$$\textit{Slew Loss Energy} = V_d\,I_{av}\,(b\,T_q) \quad (4)$$

When the resonant transfer occurs the link voltage is taken as the value $(1+k)V_p$. However, the line to line voltage for the incoming phases could be anything from 0 to

V_p. If the voltage is evenly divided between the snubbers of both incoming phases the capacitor energy loss is $1/2C_sV_S^2$. The capacitance C_s is specified for a specified rated I_d giving the worst case dv/dt. One third of the time the commutation will be from a link voltage of $(1+k)V_p$ to the null state or to a line to line voltage of zero. For simplicity the voltage is assumed to be evenly distributed from 0 to V_p for the remainder of the time. The uniform distribution assumption gives an average value for V_S^2 as $(7/36 +k/2+k^2/2)V_P^2$. With two switches the loss energy is then

$$\textit{Snubber Loss Energy Resonant} = C_S V_P^2 (\frac{7}{36} + \frac{k}{2} + \frac{k^2}{2}) \quad (5)$$

The natural commutations will also produce snubber losses. The commutation could be from B to A and then to C. It can be assumed that these commutations have voltage differences of $V_p(1-x)$ and V_px respectively. The middle phase is assumed to be uniformly distributed between the other two phases (x uniform between 0 and 1). This simplification yields the snubber energy loss during the natural commutation intervals as

$$\textit{Snubber Loss Energy Natural} = C_s{*}V_P^{2/3} \quad (6)$$

The reverse recovery at rated dv/dt and di/dt can be found from manufacturers data as R joules per switching. Taking the worst case of the resonant turn off loss and neglecting the natural commutation reverse recovery loss

$$\textit{Recovery Loss} = R\, f_s \quad (7)$$

The resistive losses of the link and phase inductors also clearly need to be taken into account. It is assumed that the resistive impedance is 5% of the mains frequency impedance and determine that the phase current is conducting I_d for 1/3 of the time giving an rms of $I_d/\sqrt{3}$. Knowing the commutation times the rms value for those currents are found giving a total loss of

$$\textit{Inductor Loss} = 3\, r_{ph} (\frac{I_d}{\sqrt{3}})^2 + r_{com}(I_d \sqrt{t_{res}\, f})^2 + r_{slew}(I_{slewpeak} \frac{\sqrt{t_{res}\, f}}{2})^2 \quad (8)$$

LOSS EXAMPLE

Consider the thyristor GE C713, with a voltage limit of 2000 V and an average current suitable for a link current of 1800 A. With a safety factor of 1.3 above the worst case resonant peak and using an overvoltage factor of k=0.3, the output peak inverter voltage V_p = 615 V. For a modulation frequency of 1.2 kHz, reverse recovery of T_q = 50μS and slew factor b = 0.5, the losses for the output side become,

Conduction loss:	7003 W
Resonant loss:	1512 W
Reverse recovery:	600 W
Inductor loss:	420 W
Snubber losses:	5103 W

For this configuration the inverter output VA is 886 kVA but the filter capacitors set at 10 times the link transfer capacitors absorb 378 kVA so that the effective output power is reduced to 802 kW. The total conversion efficiency is then 96.4% including both input and output losses.

CONCLUSION

This paper has described a new type of notching current source converter suitable for high power applications. The converter can be commutated in both the rectifying and inverting mode. Since the converter thyristors are soft switched the associated losses are greatly reduced. The approach is equally suitable for single ended bridge type applications such as dc motor drives and magnet power supplies and for double ended bridge type applications such as variable speed induction motor drives.

REFERENCES

[1] S. Nonaka and Y. Neba, "A PWM Current Source Type Converter-Inverter System For Bi-directional Power Flow" IEEE IAS Annual Meeting Conf. Record, 1988, pp. 296-301.

[2] Y. Murai and T.A. Lipo, "High Frequency Series Resonant DC Link Power Conversion", 1988 IAS Annual Meeting, Oct. 2-7, Pittsburgh PA, pp. 772-779.

[3] Y. Murai, S.G. Abeyratne, T.A. Lipo and P. Caldeira, "Current Peak Limiting for a Series Resonant DC Link Power Conversion Using a Saturable Core", 1991 European Power Electronics Conference, Florence Italy, Sept. 1991, vol. 2, pp. 8-12.

[4] Y. Chung and G. Cho, "New Current Source Inverters With Dc-Side Commutation And Load Side Energy Recovery Circuit", 1991 IEEE Power Electronics Specialist Conference, June 1991, pp.

[5] G. Ledwich, "Current Source Inverter Modulation", IEEE Trans. on Power Electronics, vol. 6, No. 4, Oct. 1991, pp. 618-623.