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Pulse Width Modulated Series Resonant Converter

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PULSE WIDTH MODULATED SERIES RESONANT CONVERTER

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ABSTRACT-Pulse width modulation (PWM) has been a very powerful tool for control of power electronic systems. Series and parallel resonant converters realize PWM by using an integer number of half sine pulses of current and voltage respectively. For high power applications the reverse recovery time of the switches is the dominant factor in PWM operation since this sets the period when the converter cannot transfer power from input to output (dead time). A PWM extension of the series resonant converter is presented which reduces the dead time and improves the modulation strategy of this type of converter. With the addition of one thyristor and one diode to the 12 thyristors of a series resonant converter, pulses of link current of arbitrary width can be created. Simulations show that good waveform quality can be achieved and experimental results also show a reduction in the effective dead time.

I. INTRODUCTION

A variety of different controls, such as phase control, integral control, and chopper control [1], have been used to obtain a controllable dc voltage from a dc or ac source. Switching losses due to hard switching processes, high ripple due to low frequency of supplies, limited control of the input power factor and bad harmonic content have been cited as disadvantages of these systems.

One approach that could be used to solve these problems has been proposed in [2]. However, the proposed circuit uses an extra switch that continually conducts load current thus increasing conduction losses.

In the past few years, remarkable progress has beenmade in the development of resonant link converters. These converters are unique in that they allow devices to switch at zero voltage or zero current crossing [3-6]. Recently, one member of this family of converter, a high frequency series resonant DC link current converter, has been utilized as a conditioning system for SMES [7] and to drive a dc motor [8]. However, this converter only allows integral cycle switching and is therefore incapable of synchronizing with external PWM signals. With this type of control mode, control of input power factor is obtained at expense of resonant capacitor overvoltage during the zero current period which must occur on the link to produce zero current switching.

This paper proposes a new type of PWM series resonant DC link converter. The pulse width modulation feature can be implemented by the addition of a diode and a thyristor to a series resonant link converter as shown in Fig. 1. The concept can be used to produce arbitrary pulse width current pulses to the desired phases by simply delaying the onset of the resonance in the link tank circuit which is normally freely running in the conventional series resonant converter circuit [1].

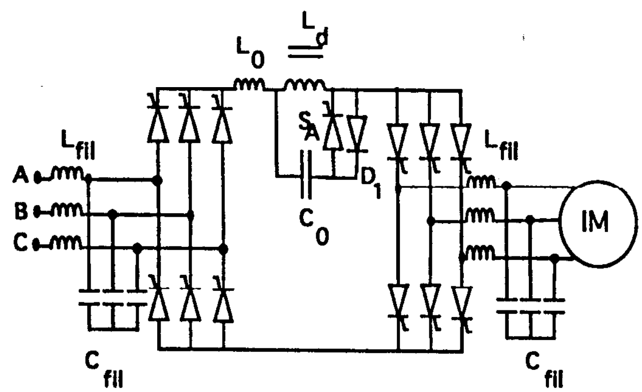

Fig 1 Pulse Width Modulated Series Resonant DC Link Converter (PWM-SRDCL)

II. CONTROL OPTIONS FOR THE PWM-SRDCL CONVERTER

The options available for controlling the pulse width in closed loop hard switched inverters include error saw-tooth, sampled error and hysteresis controllers. One aspect which differentiates the soft switched from the hard switched converter is that the initiation of resonant turn off time is to be controlled, not the edge of the pulse. In addition, one current zero is used to switch both input and output bridges. This aspect of control makes it difficult to use an error type saw-tooth current controller since only one bridge could be controlled in this manner. However, the hysteresis approach can be extended to double bridge systems by initiating turn off of the link if either bridge has an error outside a specified error bound. The implementation of the hysteresis approach gives undesirable results because the error significantly exceeds the bound by the time the resonant pulse is complete and one has to ensure that the error trajectory passes inside the error bound before attending to the bound being exceeded.

The sampled error approach was also rejected as it again quantized the turn off points that had become continuous variables through the use of the extra thyristor and diode. A reduced dead time can be achieved and a good balance of input and output errors achieved using a fixed width hold off time.

For most motor drive systems, the input harmonic spectrum is more important than the motor side harmonics. For this case a pulse width control based of the input bridge tracking error with an upper bound on the pulse width has been determined to be feasible. The upper limit on the width ensures that the output waveform achieves a definite lower limit to its switching change rate. The width is set by the criterion that the system stays in one switch configuration as long as no adjacent state on the input bridge is better than the current one (by a fixed amount). This offset in the decision making process can provide a form of hysteresis control, but for the cases examined a simple zero offset gave desirable performance.

III. PRINCIPLE OF OPERATION

Figure 2 shows the monophase equivalent of the PWM-SRDCL converter. The fact that the link resonates at a much higher frequency compared to the input and output side voltages and currents allows one to use this equivalent circuit to investigate how the converter operates. In this analysis the system is assumed to be operating at the steady state with the link current is almost constant (i_d=I_d). The output voltage of the input side converter, $v_d(t)$, can have a positive, negative or zero voltage depending on the current error. The analysis will be done for the most positive voltage available, V_d. The switch SW in Fig. 2 represents four switches, two in each bridge. These switches are either conducting altogether or are chosen to be turned on when the necessary condition is satisfied. The voltage across the switch is shown as v_{sw} and the switch is turned on when this voltage is greater than a pre-described voltage, V_{swt}. The output side capacitors are assumed to have a constant voltage across them during the interval being investigated. This voltage is represented as $v_o(t)$=V_o.

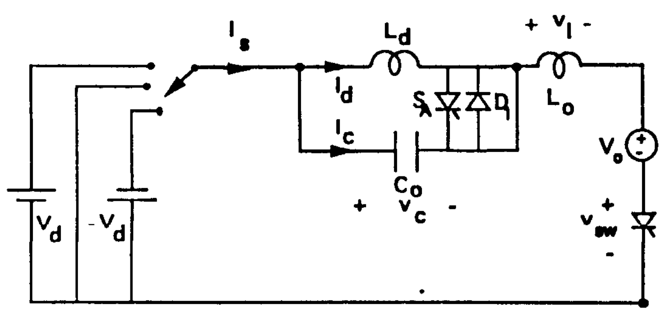

Fig 2 Monophase equivalent of the PWM-SRDCL Converter

The operation of the system can be analyzed in each of its different modes. To begin, it is assumed that all the main switches are off and the link current is less than the reference value. Therefore, two switches of the input side converter that would yield the most positive voltage (V_d) should be turned on. For the switches to be turned on, the switch voltage should be greater than V_{swt}. Therefore the resonant capacitor should discharge through the diode D_1 so that this voltage condition is satisfied. This procedure is carried out in the first interval of Mode 1.

Mode 1: During the first interval of this mode, the capacitor is discharged from an initial voltage V_{C0} (to be calculated) through D_1 with the following equation:

$$v_c(t)=-\frac{I_d}{C_0}\,t + V_{C0} \tag{1}$$

Switches S_A and SW are off and the resonant current (i_s) is zero during this interval. The first interval ends when $v_c(t)$ = V_d-V_o-V_{swt} at which moment $v_{sw}(t)$=V_{swt}, allowing one to turn on the switches. The second interval starts with turn-on of the main switches (SW). The initial conditions for this interval are given by Eqs. (2a-b).

$$i_s(0)=0 \tag{2a}$$

$$v_c(0)=E-V_{swt} \tag{2b}$$

where,

$$E=V_d- V_o \tag{3}$$

By solving the differential equations of the system with these initial conditions, Eqs. (4a-c) are obtained as the governing equations for this interval.

$$v_c(t)=E_1-V_{swt}\cos\omega_0 t - Z_0 I_d \sin\omega_0 t \tag{4a}$$

$$i_s(t)=I_d-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \tag{4b}$$

$$i_c(t)=-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \tag{4c}$$

The quantities Z_0 and ω_0 in (4) are given as:

$$Z_0=\sqrt{\frac{L_0}{C_0}}$$

$$\omega_0=\frac{1}{2\pi\sqrt{L_0C_0}} \tag{5}$$

and E_1 is defined as

$$E_1=V_d-V_o \tag{6}$$

At the instant $\omega t=\tan^{-1}(Z_0I_d/V_{swt})$ the capacitor current is zero and the diode turns off. This is the end of the second interval and beginning of the third interval. Since the diode is off, the dc current I_d flows through SW during this mode. The resonant capacitor C_0 voltage is maintained at aconstant value of

$$V_c=E_1-\sqrt{V_{swt}^2-Z_0^2I_d^2} \tag{7}$$

This condition is maintained until the dc current becomes larger than the reference current at which time the auxiliary switch S_A is turned on creating a resonant circuit. This instant is the beginning of interval 4. The equations for this interval are given by Eq. (8).

$$v_c(t)=E_1-\sqrt{V_{swt}^2+Z_0^2 I_d^2}\cos\omega_0 t \quad (8a)$$

$$i_s(t)=I_d+\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (8b)$$

$$i_c(t)=\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (8c)$$

When the resonant current reaches zero, S_A turns off and this interval ends. The value of the capacitor voltage at the end of this interval must be equal to V_{C0} given as the initial value for the first interval which can now be easily calculated as

$$V_{C0}=E_1+V_{swt} \quad (9)$$

As long as additional current required on the link, intervals 1 through 4 are repeated. If the resonant current becomes greater than the reference value then the two switches of the input side converter that would give the most negative output voltage should be gated . However, before applying a negative voltage to the link, a null state must first be utilized. This is accomplished in Mode 2.

Mode 2: During the null state, two switches on the same leg of the input side bridge will be turned on giving $v_d(t)=0$. To be able to turn these switches on, SW has to have sufficient voltage across it. Therefore, the resonant capacitor must be charged again through the diode D_1 from E_1+V_{swt} to $-V_o-V_{swt}$ so that $v_{sw}(t)$ would be equal to V_{swt}. This charging process is defined by (10).

$$v_c(t)=-\frac{I_d}{C_0}t+E_1+V_{swt} \quad (10)$$

The discharging process is the first interval of Mode 2. The null state starts with the second interval. Having $v_d(t)=0$, $V_{C0}=-V_o-V_{swt}$ and $i_s(0)=0$ conditions, the equations for this interval are given by (11).

$$v_c(t)=-V_o-V_{swt}\cos\omega_0 t-Z_0 I_d\sin\omega_0 t \quad (11a)$$

$$i_s(t)=I_d-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \quad (11b)$$

$$i_c(t)=-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \quad (11c)$$

At the time instant $\omega t=\tan^{-1}(Z_0 I_d/V_{swt})$ the capacitor current is zero and the diode turns off. As soon as the diode turns off, the S_A switch is turned on. Since there is no energy transfer in the null state, there is no use to have a constant current interval as in Mode 1. The voltage of the capacitor at the instant of switching is given by (12).

$$V_C=-V_o-\sqrt{V_{swt}^2+Z_0^2 I_d^2} \quad (12)$$

When S_A is turned on, a new resonant cycle defined by (13) begins.

$$v_c(t)=V_o-\sqrt{V_{swt}^2+Z_0^2 I_d^2}\cos\omega_0 t \quad (13a)$$

$$i_s(t)=I_d+\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (13b)$$

$$i_c(t)=\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (13c)$$

When the resonant current is zero, this mode is over and Mode 3 starts. If, during the null state, the dc current i_d again becomes smaller than the reference current then there is no need to apply a negative voltage to the link and we go back to the positive voltage stage. But, since the most general case is being investigated here, we will assume that this does not occur.

Mode 3: Mode 3 starts with a charging interval as v_d will be equal to $-V_d$ and SW switch will not have enough positive voltage across it. The charging equation is given by (14).

$$v_c(t)=-\frac{I_d}{C_0}t-V_o+V_{swt} \quad (14)$$

This interval ends when

$$v_c(t)=-E_2-V_{swt} \quad (15)$$

where E_2 is given as

$$E_2=V_d+V_o \quad (16)$$

At this point switch SW has V_{swt} across it and therefore can be turned on. Equations (17a-c) describe the operation in this second interval.

$$v_c(t)=E_2-V_{swt}\cos\omega_0 t-Z_0 I_d\sin\omega_0 t \quad (17a)$$

$$i_s(t)=I_d-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \quad (17b)$$

$$i_c(t)=-I_d\cos\omega_0 t+\frac{V_{swt}}{Z_0}\sin\omega_0 t \quad (17c)$$

Again, after i_c becomes zero, there exists an interval during which $i_s=I_d$. This interval continues until the current i_d becomes smaller than the reference current requiring a positive link voltage. During this third interval the capacitor voltage is given by (18).

$$V_C=-E_2-\sqrt{V_{swt}^2+Z_0^2 I_d^2} \quad (18)$$

At the end of the third interval S_A is turned on and the following equations are valid in the fourth interval.

$$v_c(t)=-E_2-\sqrt{V_{swt}^2+Z_0^2 I_d^2}\cos\omega_0 t \quad (19a)$$

$$i_s(t)=I_d+\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (19b)$$

$$i_c(t)=\frac{\sqrt{V_{swt}^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \quad (19c)$$

At the end of this resonant cycle Mode 3 ends leading to another null state before applying the link a positive voltage.

Equation (20) gives the capacitor voltage at the end of this mode.

$$V_C=-E_2+V_{swt} \tag{20}$$

Mode 4: Since $v_d(t)$ will be equal to zero during this mode, using (20) as initial condition, it can be seen that the switch SW has across it V_d-V_{swt} which is larger than V_{swt} if $V_{swt} \leq 0.5\ V_d$. Since this condition is normally satisfied, there is no need for a charging period and the switches can be turned on.

The equations for the first interval of Mode 4 are given by (21).

$$v_c(t)=-V_o-(V_d-V_{swt})\cos\omega_0 t-Z_0 I_d \sin\omega_0 t \tag{21a}$$

$$i_s(t)=I_d-I_d\cos\omega_0 t+\frac{(V_d-V_{swt})}{Z_0}\sin\omega_0 t \tag{21b}$$

$$i_c(t)=-I_d\cos\omega_0 t+\frac{(V_d-V_{swt})}{Z_0}\sin\omega_0 t \tag{21c}$$

When i_c=0, diode D_1 turns off. As in Mode 2, there is no need to have a constant current interval and S_A can be turned on immediately. At the time of this switching the capacitor voltage is given by (22).

$$V_C=-V_o-\sqrt{(V_d-V_{swt})^2+Z_0^2 I_d^2} \tag{22}$$

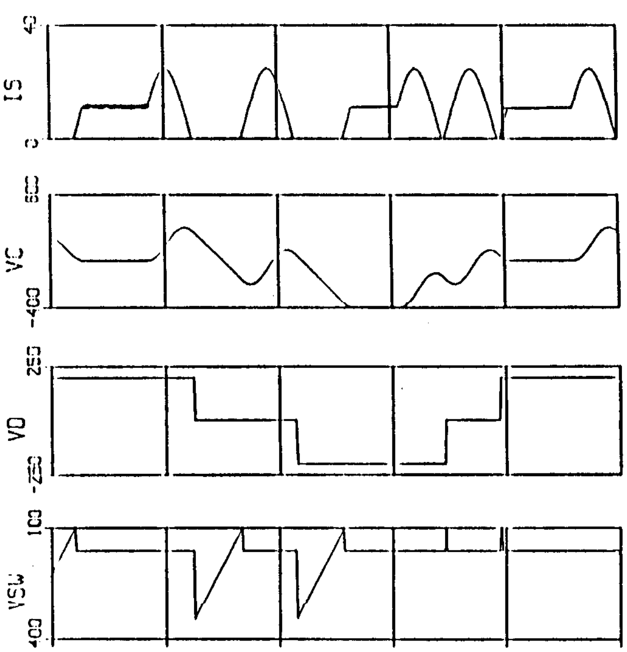

Fig.3 Ideal operating waveforms of PWM-SRDCL Converter with the adjacent states control method.

Turning S_A on starts the resonant cycle which is defined by (23).

$$v_c(t)=-V_o-\sqrt{(V_d-V_{swt})^2+Z_0^2 I_d^2}\cos\omega_0 t \\ -Z_0 I_d \sin\omega_0 t \tag{23a}$$

$$i_s(t)=I_d+\frac{\sqrt{(V_d-V_{swt})^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \tag{23b}$$

$$i_c(t)=\frac{\sqrt{(V_d-V_{swt})^2+Z_0^2 I_d^2}}{Z_0}\sin\omega_0 t \tag{23c}$$

The final value of the capacitor voltage in this mode is given by (24).

$$V_C=-V_o+V_d-V_{swt}=E_1-V_{swt} \tag{24}$$

Now that the null state has been attained, v_d will again be equal to the voltage V_d. Under these conditions the switch voltage can be calculated as V_{swt} which shows that, again, there is no need for a charging interval. Therefore, circuit operation is again placed in Mode 1.

All the related waveforms of the PWM-SRDCL converter are given in Fig. 3 based on the preceding calculations. These waveforms were drawn for the following parameters:

$$I_d=10\text{ A},\ Z_0=10\ \Omega,\ V_d=200\text{ V}, \\ V_o=50\text{ V},\ V_{swt}=100\text{ V} \tag{25}$$

A simpler control method that was used in our experiments is to change the input side converter voltage only between positive voltage and zero voltage. The equations and waveforms can be easily obtained in the same way. Figure 4 shows the waveforms for this method with the same parameters given by Eq. (25). As can be noticed, in this control scheme the constant current interval has to be utilized during the null state until the current i_d reaches the reference value.

IV. SIMULATED AND EXPERIMENTAL RESULTS

A. Simulation Results

The system shown in Fig. 1 was simulated for the case of three phase resistive load instead of induction machine. The adjacent states vector control method was used as the control algorithm. Some of the results obtained during the simulation study are given in Figs. 5 and 6. In particular, Fig. 5a shows the inverter current. The filtered inverter current is shown in Fig. 5b. A nearly sinusoidal inverter current can be obtained as seen in this trace. Figure 6 also illustrates the low harmonic content of the input current that can be attained. As shown in the figure, the largest harmonic is less than 5% of the fundamental. These simulations were run for a high rated power system.

B. Experimental Results

In order to verify the theory presented in this paper an existing 20 kHZ 5 kW series resonant converter was converted to the link structure of Fig. 1 with the output side bridge and motor replaced by either by a resistive or a DC motor load.

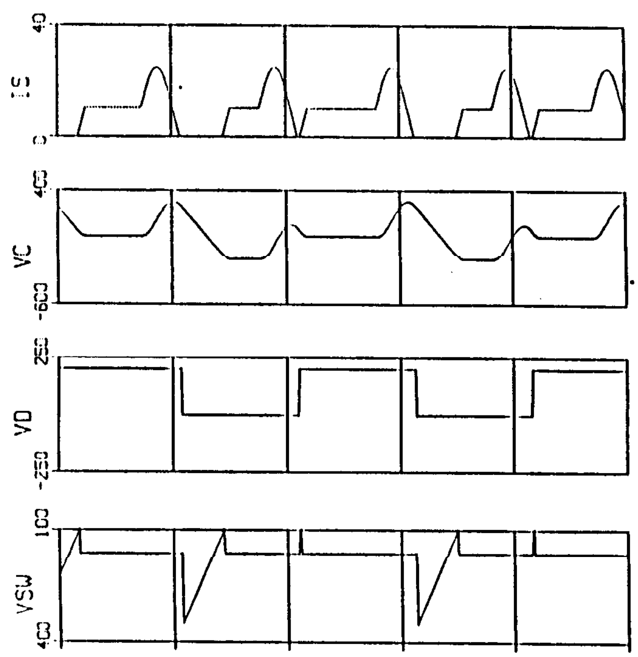

Fig.4 Ideal operating waveforms of PWM-SRDCL Converter with the simplified control method.

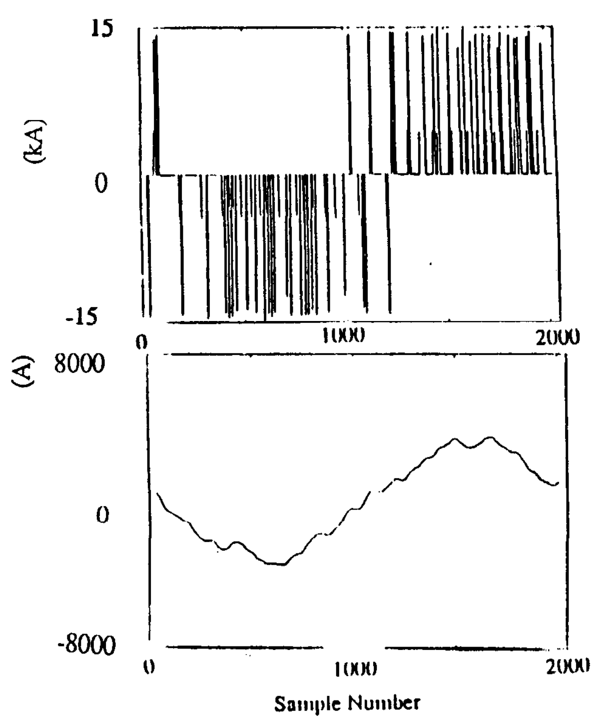

Fig.5 Simulation results by using the adjacent states method: (a) Inverter current, (b) Filtered inverter current

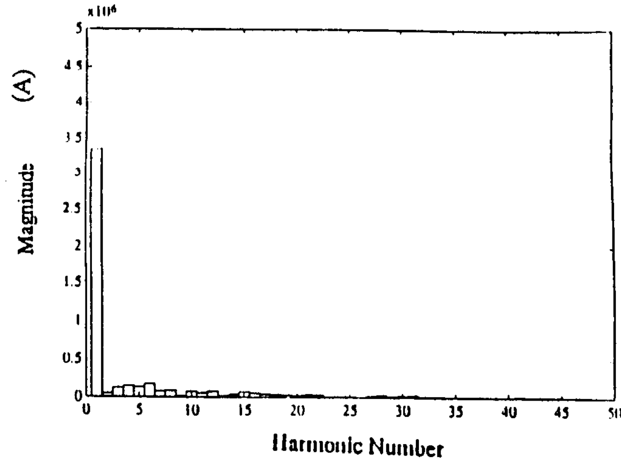

Fig.6 Simulation result: Harmonic content of the input current of the PWM-SRDCL Converter

The results of Fig. 7 show the current in L_0 (I_s), the voltage across C_0 and the ripple of the DC link current I_d. In this case it can be noted that the resonant current remains in a particular state until the error in I_d exceeded a given threshold or until the maximum width of 400 μs is reached. A corresponding trace for the former control method is shown in Fig. 8. Compared with the standard SRC performance of I_s in Fig. 8, a much lower percentage dead time for PWMSRC can be noted.

Fig.7 Waveforms from DC motor experiment: (a) Resonant current i_s 5 A/div, (b) Capacitor voltage v_c 100 V/div, (c) Ripple of the DC current I_d 0.2 A/div (0.5 msec/div)

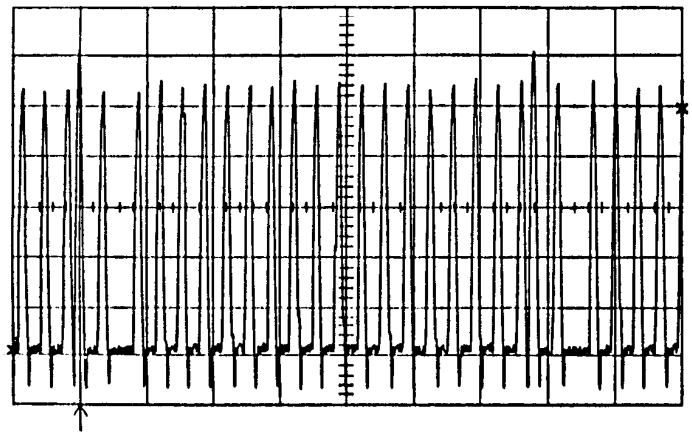

Fig.8 The resonant current waveform obtained with normal SRDCL Converter 5 A/div, 0.2 msec/div

V. CONCLUSION

In this paper an improved version of the Series Resonant DC Link Converter, PWM-SRDCL Converter was introduced. Its operation was analyzed, and simulation and experimental results were presented. From the simulation and experimental results obtained during this study it can be concluded that the proposed control scheme has the following advantages over previous methods:

-inverter switching and external PWM signals can be synchronized,

-high frequency dc link current regulation remains possible allowing line current power factor control,

-the link resonant frequency is the same as the resonant series dc link current converter,

-device stresses are typically lower than in the normal series resonant dc link converter when a PWM technique is employed.

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