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Force Commutated Three Level Boost Type Rectifier

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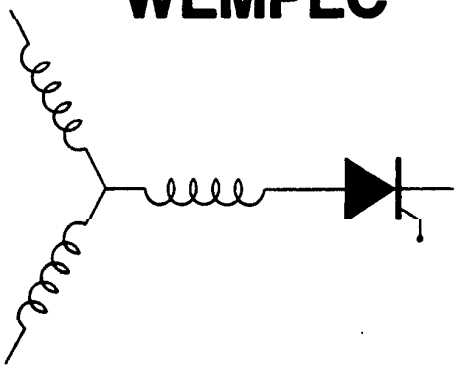

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ABSTRACT: A new force commutated three level boost type rectifier is proposed in this paper. The rectifier has the characteristics of drawing nearly sinusoidal current from utility with unity fundamental power factor. High reliability is possible due to its shoot-through free structure. Doubled DC bus voltage compared to a normal single level rectifier is also possible because of the neutral point clamping. The operating principle, steady state analysis, input current and neutral point voltage control schemes, as well as detailed experimental results are presented in this paper.

1. INTRODUCTION

The thyristor bridge rectifier is the most widely used interface between utility and power electronics systems or any other systems where DC power supplies are required. Although the thyristor bridge rectifier is very simple in structure and robust in operation, it has the disadvantages of drawing a large amount of harmonic current from utility and causing utility pollution. As more and more power electronics systems are being used in industry, it can be expected that the utility pollution problem will become increasingly intolerable. Therefore, standards such as IEEE 519 have been proposed that will eventually lead to limiting the direct use of thyristor bridge rectifier as the interface. At the same time, much effort has been made with the low harmonic current injection to utility and controllable input power factor as major goals.

In this paper, a new interface topology called a force commutated three level rectifier is proposed. The paper focuses its discussions on the operating principle, operating range, and input current control scheme of this new topology. Experimental results are presented. Voltage balancing among the series connected DC bus capacitors, a common problem with multi-level converters is also treated in this paper.

2. OPERATING PRINCIPLE AND STEADY STATE ANALYSIS

The proposed three level boost type rectifier is shown in Fig. 1. In the switching arm 1, the rectifier input terminal voltage V_{un} is clamped to the neutral point of the DC bus when switches S_{11}, and S_{12} are "on". When S_{11}, S_{12} are "off", V_{un} can be either $+V_d/2$ or $-V_d/2$ according to the polarity of the current of phase A. It can be noted that because of the existence of the DC bus neutral point, the maximum voltage stress on each device is $V_d/2$. This feature enables the rectifier output voltage to be double the DC bus voltage compared with a conventional PWM type rectifier with same switching device voltage rating. Another significant advantage of the proposed topology is that the shoot-though current is blocked by the diodes connected to the DC buses even when both the switches in a switching arm are "on". This provides for high reliability of the rectifier.

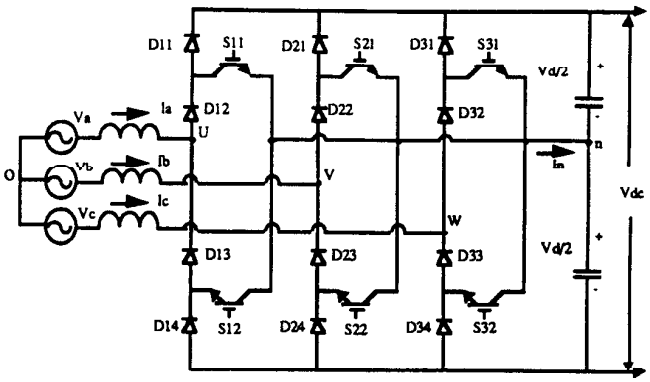
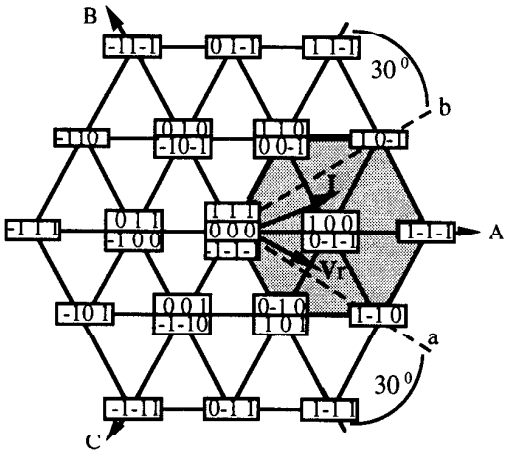


Fig. 1 Proposed Circuit Configuration

As each switching arm has three switching modes, the total number of switching modes of the rectifier is $3^3 = 27$. The number of distinguishable voltage vectors produced by the 27 switching modes is 19. The switching modes and the voltage vectors for this circuit are shown in Fig. 2.

Referring to the utility-rectifier equivalent circuit shown in Fig. 3, from fundamental circuit theory it can be determined that for the input current to be sinusoidal the rectifier input terminal voltage V_{uo}, V_{vo}, and V_{wo} must be sinusoidal as well. Although it is impossible, one can synthesize these currents using the voltage vectors in Fig. 2 in a manner that the rectifier input terminal voltage has a desired fundamental component with only high frequency harmonics. Thus the input harmonic current is small due to the low pass characteristic of the input inductors. In order to control the amplitude and the phase angle of the input current, it is also required that the amplitude and the phase angle of the rectifier input terminal voltage should be controllable. However, it should be pointed out that for the proposed circuit configuration only a portion of the 19 voltage vectors are realizable at any instant of time. Consider the case in Fig. 2, for the given current vector

position, $i_a > 0$, $i_b < 0$, and $i_c < 0$. Here, switching state " -1 " is not realizable because the positive current of phase A can not flow through D_{13} and D_{14}. For the same reason, state " +1 " is not possible in both arm 2 and arm 3 for that input current vector position. Therefore, the hexagon shaped shaded area can be determined which contains the realizable switching modes and voltage vectors. This area moves as the current vector rotates in the vector space. Because of the restricted switching mode realization, it is necessary to investigate its impact on the input current control.



D=1 rectifier input terminal is clamped to positive dc bus
D=0 rectifier input terminal is clamped to dc bus neutral point
D=-1 rectifier input terminal is clamped to negative dc bus

Fig. 2 Switching Modes and Limitations on Voltage Vector Realization

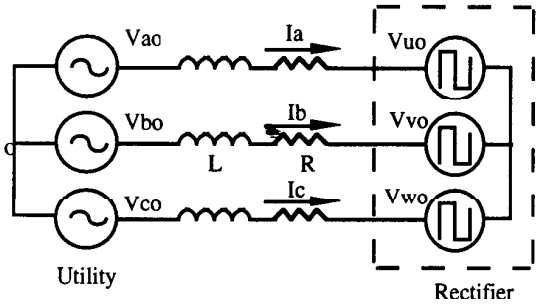


Fig. 3 Utility Rectifier Equivalent Circuit

Again referring to Fig. 2 it can be noted that if the current vector **I** stays in the region bounded by the dashed lines a and b, then the shaded area will be kept at the position shown. Also the voltage vector $\mathbf{V}_r$ corresponding to the desired rectifier input terminal voltage vector must remain in this area as well. The two worst cases occur when the current vector **I** is at the position of line a and the leading of **I** with respect to $\mathbf{V}_r$ is greater than 30°, and when **I** is at the position of line b with a 30^0 lagging condition. In both cases vector $\mathbf{V}_r$ is required outside the hexagon and thus is unrealizable. The phasor diagrams of the two critical cases are drawn in Fig. 4 (where R is neglected). From the phasor diagram in Fig. 4 a) one can derive the following equation for the input current.

$$I_{max}(p.u)=1.155 \sin(\phi+ 30^o) \qquad (2.1)$$

where ϕ is the input current displacement angle.

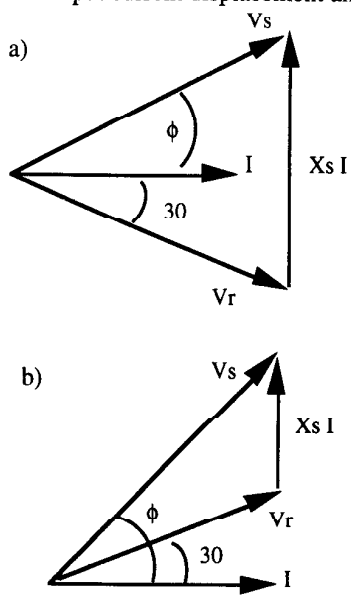


Fig. 4 Phasor Diagrams for Critical Operation
a) 30^0 lagging, V_r vs. I
b) 30^0 leading, V_r vs. I

The current I_{max} is the maximum current that the rectifier can draw from utility without low frequency harmonic distortions. It is a p.u. value with $V_b=V_s$, the rms phase voltage of utility, and $I_b=\frac{V_b}{X_s}$, the rectifier input terminal short circuit current, where $X_s=\omega L$.

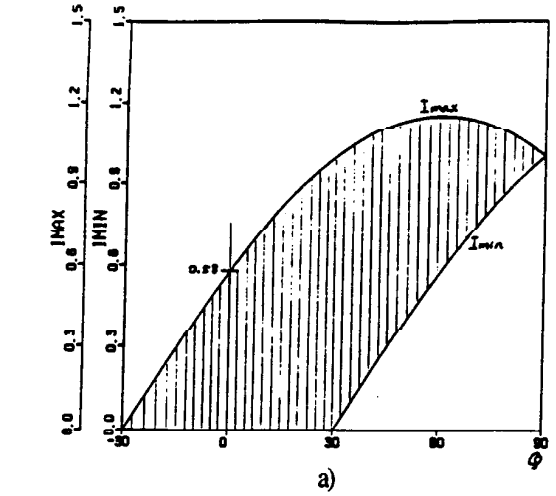
Another equation derived from Fig. 4 b) is:

$$I_{min}(p.u)=1.155 \sin(\phi - 30^o) \qquad (2.2)$$

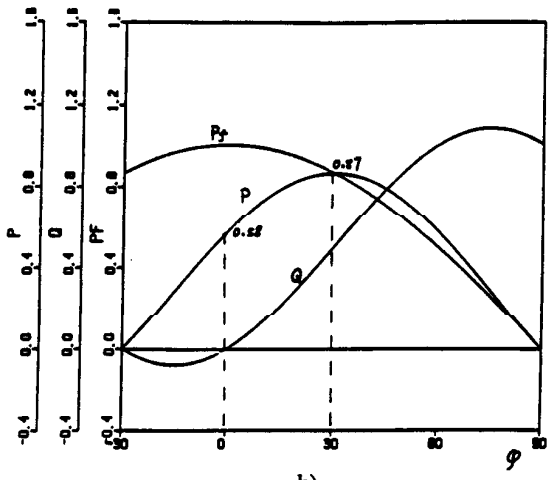
The current I_{min} is the minimum current that the rectifier must draw from utility to avoid low frequency harmonic distortions.

Equations (2.1) and (2.2) define the limits of the operation region of the proposed rectifier as shown in Fig. 5 a). The maximum input power and reactive power can be easily derived from Eq. (2.1) and are shown in Fig. 5 b) with:

$$P_{max}(p.u)=1.155 \sin(\phi+ 30^o) \cos(\phi) \qquad (2.3)$$
$$Q_{max}(p.u)=1.155 \sin(\phi+ 30^o) \sin(\phi) \qquad (2.4)$$



a)



b)

Fig. 5 Steady State Analysis Results
a) Operating region for input current
b) Maximum power and reactive power, power factor

3. INPUT CURRENT AND DC BUS NEUTRAL POINT VOLTAGE CONTROL

The steady state analysis in the previous section is based on the assumption that the voltage across the DC bus capacitors are balanced. In reality the neutral point voltage is inclined to drift due to an arbitrary unbalanced operation due to slight imperfections in circuit. Therefore, explicit control over the neutral point voltage must be exercised together with input current control to guarantee correct operation of the rectifier.

3.1 Neutral Point Voltage Control

Neutral point voltage control is achieved by using the voltage vectors in the center of each shaded hexagon. In Fig. 2, this vector is produced by switching modes 1,0,0 and 0,-1,-1. Because each of these vectors corresponds to two switching modes, and the two switching modes produce different polarities of neutral current I_n, two degrees of freedom exist to control the input current and neutral point voltage simultaneously. In particular if the voltage vector at the center of the shaded area in Fig. 2 is demanded by the current controller, one can choose either switching mode 1,0,0 or switching mode 0,-1,-1 to produce this voltage vector. When mode 1,0,0 is chosen, rectifier input terminals V and W are clamped to the neutral point. Because input current I_b and I_c are negative, neutral current I_n is forced to flow out of the neutral point. As a result, the neutral point voltage will drift towards negative DC bus. On the other hand if switching mode 0,-1,-1 is chosen, the neutral point voltage will drift toward positive DC bus since the neutral current now becomes positive.

3.2 Current Control Scheme

Theoretically almost all the control schemes developed for inverter current control can be employed for the purpose of current control of this converter. Among these schemes, the hysteresis controller is the choice for the method with greatest simplicity of implementation. When a hysteresis controller is used the voltage vectors are randomly chosen from a hexagon which contains 7 possibilities. Therefore, the chance of the voltage vector capable of controlling neutral point voltage being selected is only one in seven. This degree of control does not appear to be sufficient for the purpose of neutral point voltage control. Based on experience with the circuit it appears that the best current control scheme for the proposed rectifier should be the one with not only fast response to the input current error, but also a strong ability to handle the neutral point voltage drifting problem. For this purpose, a novel current control scheme was adopted with some modifications. The scheme utilizes current deviation vector in determining switching modes and offers great flexibility in compromising between input current and neutral point voltage control.

The principle of the current control scheme is illustrated as follows.

The voltage equation for the power supply-rectifier equivalent circuit shown in Fig. 3 can be expressed as:

$$V_S = L\frac{dI}{dt} + RI + V_r(k) \qquad (3.1)$$

where

$V_S = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$, power supply phase voltage,

$I = \begin{bmatrix} ia \\ ib \\ ic \end{bmatrix}$, rectifier input current,

$V_r(k) = \begin{bmatrix} v_{uo}(k) \\ v_{vo}(k) \\ v_{wo}(k) \end{bmatrix}$, instantaneous rectifier input terminal voltage, k=0,...,18.

Defining $\Delta \mathbf{I} = \mathbf{I}^* - \mathbf{I}$ and substituting into (3.1) yields:

$$L\frac{d(\Delta I)}{dt} = V_r(k) - E \qquad (3.2)$$

where

$$\Delta I = \begin{bmatrix} i_a^* - ia \\ i_b^* - ib \\ i_c^* - i_c \end{bmatrix}, \text{ current deviation vector,}$$

$$I^* = \begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix}, \text{ input current reference, and}$$

$$E = V_S - \left(L\frac{dI^*}{dt} + RI^*\right) = \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \qquad (3.3)$$

If unity input power factor is assumed then $\mathbf{I}^*$ is in phase with V_S. Let $v_a = V_m \sin(\omega t)$, $i_a^* = I_m^* \sin(\omega t)$. Substituting these expressions into (3.3) yields:

$$E = \begin{bmatrix} E_m \sin(\omega t - \theta) \\ E_m \sin(\omega t - \theta - 120^o) \\ E_m \sin(\omega t - \theta + 120^o) \end{bmatrix} \qquad (3.4)$$

where

$$E_m = \sqrt{(V_m - RI_m^*)^2 + (\omega L I_m^*)^2}$$

$$\theta = \tan^{-1}\left(\frac{V_m - RI_m^*}{\omega L I_m^*}\right).$$

Equation (3.4) shows that $\mathbf{E}$ can be easily determined by the current command $\mathbf{I}^*$, supply voltage V_S, and the parameters L and R. Returning to Eq. (3.2) one can find that $V_r(k)$ can be selected according to the position of vector $\mathbf{E}$ and position of the current deviation vector $\Delta \mathbf{I}$ such that the direction of $d(\Delta I)/dt$ is always trying to decrease the current deviations.

3.3 Selection of Switching Modes

For the proposed rectifier, as previously mention, the control of the input current and the control of neutral point voltage must be compromised. Another characteristic of the proposed rectifier is that for any given position of the input current vector the realizable switching modes are confined in a small hexagon around that vector. These two factors determine the rules of the switching mode selection.

Assume that the vectors $\mathbf{I}$, $\mathbf{E}$ and the corresponding realizable switching modes are at the position shown in Fig. 6 a). The hexagon in Fig. 6 a) is the same as the shaded area in Fig. 2. The $d(\Delta \mathbf{I})/dt$ vectors corresponding to $V_r(k)$ (where k=0,...,6) are also shown in Fig. 6 a). Where in Fig. 6 a) switching modes 0,-1,-1, and 1,0,0 can be used to control the neutral point voltage. Figure 6 b) shows the regions to which the current deviation vector $\Delta \mathbf{I}$ may belong.

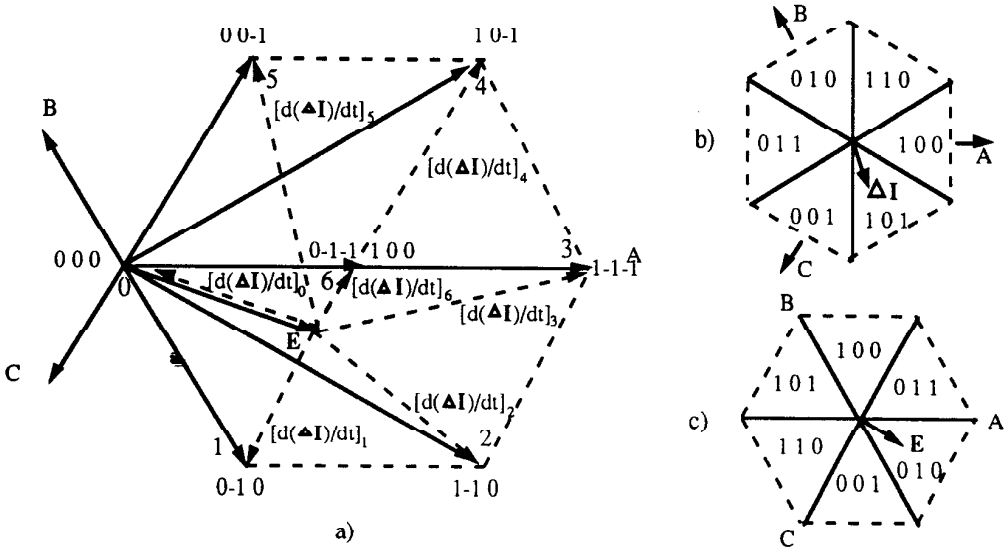


Fig. 6 Switching Modes Selection

a) Realizable switching modes for a particular position of input current vector and the derivatives of current deviation vector
b) Regions for input current vector and deviation current vector
c) Regions for Vector E

From Fig. 6 a) and Fig 6 b), if only input current control is considered, one can summarize the relations between the position of $\Delta\mathbf{I}$ and the switching modes as in Table 1. Here the rule for the selection of switching modes is to select the state that will produce vector $d(\Delta\mathbf{I})/dt$ in the direction most opposite to $\Delta\mathbf{I}$. As an example, for the $\Delta\mathbf{I}$ position in Fig. 6 b), the $d(\Delta\mathbf{I})/dt$ vector produced by switching mode 0,0,-1 (vector $\mathbf{V}_r(5)$) should be selected.

Table 2 also shows the relations between the positions of $\Delta\mathbf{I}$ and the switching modes but with the neutral point voltage control being taken into consideration. Here the rule becomes to choose vector Vr(6) (switching modes 1,0,0, or 0,- 1,-1) as many times as possible as long as the dot products of $\Delta\mathbf{I}$ and $[d(\Delta\mathbf{I})/dt]_6$ is not positive, i.e. the length of $\Delta\mathbf{I}$ does not increase.

Comparing the two tables it is possible to determine that the chances of voltage vector 6 being selected in Table 2 is three times larger than that of in Table 1. Therefore the switching mode selection method in Table 2 offers a strong control action over the neutral point voltage. The trade-off is that this method has a slower response to the current error.

Table 1. Switching Modes Selection (consider only input current control)

Position of $\Delta\mathbf{I}$	101	100	110	010	011	001
Switching modes	00-1	000	0-10	1-10	1-1-1	100 0-1-1 10-1

Table 2. Switching Modes Selection (consider both input current control and neutral point voltage control)

Position of $\Delta\mathbf{I}$	101	100	110	010	011	001
Switching modes	100 0-1-1	000	0-10	1-10	100 0-1-1	100 0-1-1

3.4 Implementation of the Switching modes Selection Scheme for Use with a Microprocessor

In a microprocessor implementation, the switching modes are stored in the memory as a look-up table with the positions of **I**, **E**, and $\Delta\mathbf{I}$ combined as its addresses. The positions of **I** and $\Delta\mathbf{I}$ are coded according to Fig. 6 b), and the position of **E** is coded according to Fig. 6 c). A neutral point voltage control bit (NPVC) is attached to the LSB of this address. When the NPVC is set to 1 by the neutral point voltage feedback control, the switching modes selected will produce a positive neutral current I_n to charge the neutral point voltage up toward the positive DC bus. On the other hand, if NPVC is set to 0, the neutral point voltage will decrease.

Table 3 shows a portion of the look-up table implemented on a microprocessor. It is translated from Table 2. The position of the hexagon in Fig. 6 a) denotes that the current vector **I** stays in the region 1,0,0 in Fig. 6 b). From Fig. 6 c) it is determined that the region code of **E** is 0,1,0.

Table 3. Switching Mode Selection Scheme Microprocessor Implementation Look-Up Table

Address				Memory
Position of **I**	Position of **E**	Position of $\Delta\mathbf{I}$	NPVC	Switching modes
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
100	010	001	0	100
100	010	001	1	0-1-1
100	010	010	*	1-10
100	010	011	0	100
100	010	011	1	0-1-1
100	010	100	*	000
100	010	101	0	100
100	010	101	1	0-1-1
100	010	110	*	0-10
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.

* don't care

4. EXPERIMENTAL RESULTS

A prototype of the proposed rectifier has been built using IGBT as the main power circuit switches and the MOTOROLA DSP56000 microprocessor as its controller. For purpose of comparison, both a hysteresis current controller and the proposed current control scheme were implemented. The waveforms of the three phase input currents i_a, i_b, i_c, and the integration of the neutral current i_n when the hysteresis controller is used are shown in Fig. 7. The reason for showing the integration of the neutral current is that it is closely related to the neutral point voltage drifting problem. The same waveforms under the control of the proposed current control scheme are shown in Fig. 8. Although the input current deviations in Fig. 7 are smaller than that in Fig. 8, the increasing neutral current integration waveform denotes the neutral point voltage drifting associated with the hysteresis current control scheme. It should be point out that the neutral point voltage was forced balanced by the use of asymmetrical loads to the two DC bus capacitors when hysteresis controller was used, otherwise the neutral point voltage would continually drift. As a result the hysteresis control was not able to function properly. On the other

hand, when the proposed control scheme was used, as can be seen from Fig. 8, although the current deviation is slightly larger due to the compromise between the input current and the neutral point voltage control, the neutral point voltage was balanced successfully and thus satisfactory operation can be guaranteed.

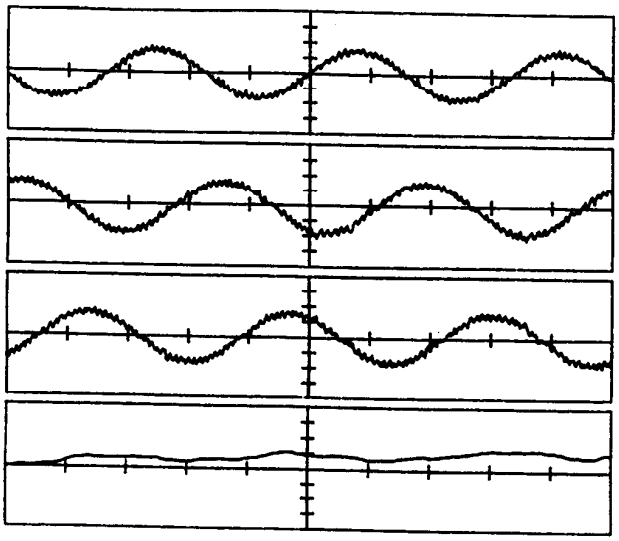


Fig. 7 Experimental Results Using Hysteresis Current Controller
(From Top to Bottom)
Traces 1, 2, 3: phase A, B, C input current, 5 A/div.
Trace 4: integration of neutral current I_n.

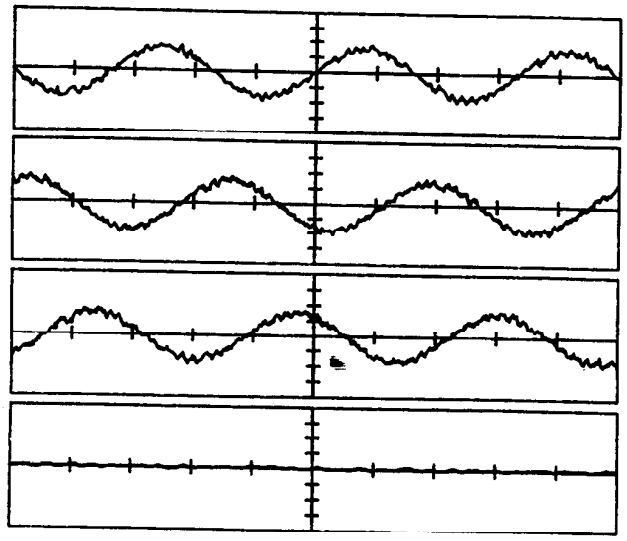


Fig. 8 Experimental Results Using Proposed Current Regulation Scheme
(From Top to Bottom)
Traces 1, 2, 3: phase A, B, C input current, 5 A/div.;
Trace 4: integration of neutral current I_n.

The AC power supply phase voltage and input current shown in Fig. 9 through Fig. 11 demonstrate feasibility of power factor adjustment. The rectifier was operated with fundamental power factors of 30° lagging in Fig. 9 , unity power factor in Fig. 10, and 30° leading in Fig. 11 respectively. Low frequency current distortions can be found in 30° leading operation as predicted in the steady state analysis.

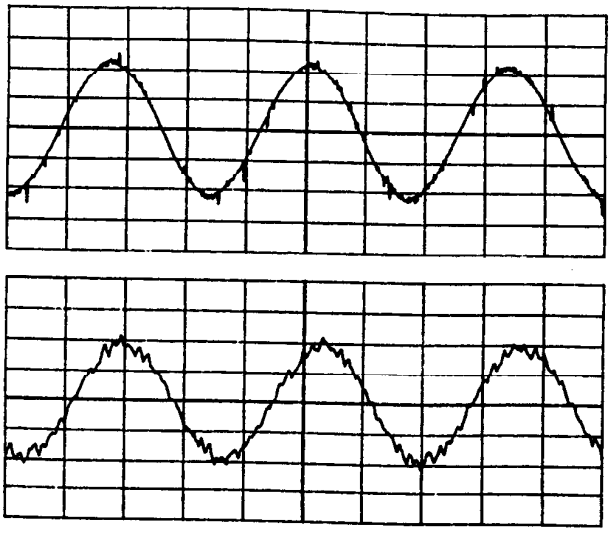


Fig. 9 Experimental Result for 30° Lagging Operation
Trace 1: phase A voltage, 50 V/div.;
Trace 2: phase A current, 5 A/div.

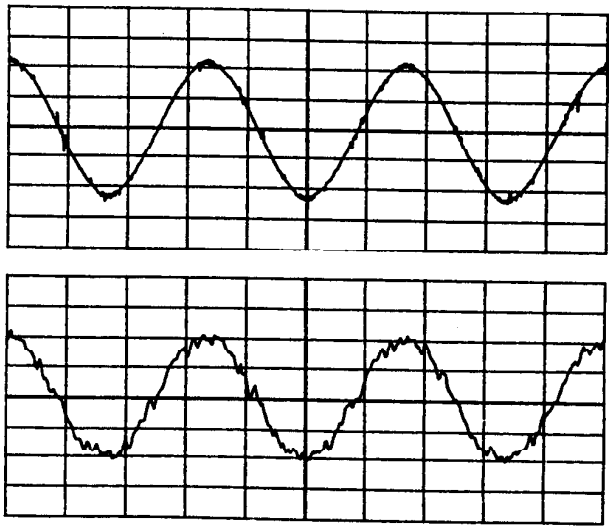


Fig. 10 Experimental Result for Unity Power Factor Operation
Trace 1: phase A voltage, 50 V/div.;
Trace 2: phase A current, 5 A/div.