Quasi Current Resonant DC Link AC/AC Converter

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Abstract— **A new quasi current resonant dc link (QCRDCL) topology has been developed in this paper. Although prototype current resonant dc link topologies for ac/ac power conversion have had such problems as irregular high current peaks, uncontrollable pulse width, etc., this new topology enables the ac/ac conversion system to have the properties wherein the current peak is limited and the pulse width is adjustable. The system begins to assume an adjustable-width flat-topped current shape, whereby the system becomes particularly suitable for high power application. With control of the pulse width a very fine load current regulation can be obtained. In this system, an open loop PWM control has been adopted and almost the same quality of output waveforms as the conventional current source inverter has been achieved.**

I. Introduction

In recent years, many types of resonant power conversion topologies have been developed for ac motor drives [1]–[6]. The basic configurations of these topologies are of the conventional VSI or CSI inverters with an additional capacitor and inductor for the resonant tank. Although such circuits can reduce the high frequency switching losses to a minimal value by means of zero-voltage or zero-current switching, they have a particular problem in that the resonant pulse peak is much higher than source voltage or current, so that the system needs much higher voltage or current rating of the switching devices than conventional hard switched inverters. Furthermore, the output waveform control is solely carried out by PDM (pulse density modulation) because of lack of pulse width adjustments. Hence they need extremely high frequency switching to achieve high quality output waveform control.

In order to solve these problems, the actively clamped resonant dc link inverter [2] and other sophisticated circuits which limit the link voltage have been presented for use with voltage resonant converters [4]–[6]. In case of current resonant converters, the authors have proposed a current peak limiting circuit for a series resonant dc link converter using a saturable core in 1991 [3]. The clamping action in this case was realized by utilizing a saturable core for a resonant inductor without using any additional active elements. Although this converter works very well with a pulse-split control principle and has some degree of current adjustment, it could not, however, easily produce wider flat-topped current waveforms.

This paper presents a new converter concept having a highly adjustable flat-topped current pulse. The system operates with partially resonant or quasi resonant topology and the pulse peak is always maintained at the dc link current value. Thus, the irregular current peak stress of the previous basic circuit is reduced and the current rating of the devices is remarkably reduced. Owing to the ability of the circuit to produce a variable current pulse width with constant pulse amplitude, open loop PWM control can be adopted and nearly the same output performance as the conventional current source GTO inverters can be achieved [7]–[9]. In the proposed system all of the switches are naturally commutated thyristors with no snubbers. Hence, the circuit is low cost concept, with great potential in high power applications.

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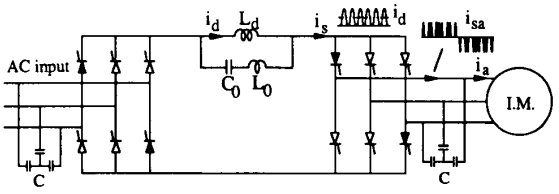

Fig. 1. Basic series resonant dc link converter.

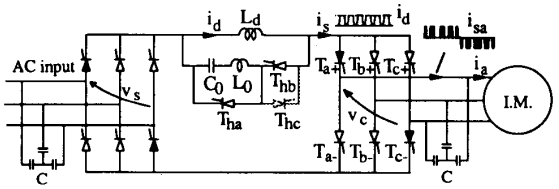

Fig. 2. Proposed quasi resonant dc link converter.

II. Principles

Fig. 1 shows the overall configuration of the basic series resonant dc link converter. The capacitance C_0 and inductance L_0 form high frequency resonant circuit and both the three capacitors at input and output are used as filters to bypass high frequency components to maintain the resonant frequency. The inductance L_d is to superimpose a dc current onto the high frequency resonant currents to allow for unidirectional switches in the converters (i.e., thyristors). Fig. 2 shows the proposed quasi resonant converter with additional three thyristors (T_{ha}, T_{hb}, and T_{hc}). These thyristors are used to control the resonance of prototype current pulses.

To explain the converter operation, the switching condition and operational waveforms are shown in Fig. 3 with a modified single phase equivalent circuit. For the equivalent circuit, the following assumptions are made. As the input and output filter capacitors are very large compared to the resonant capacitor

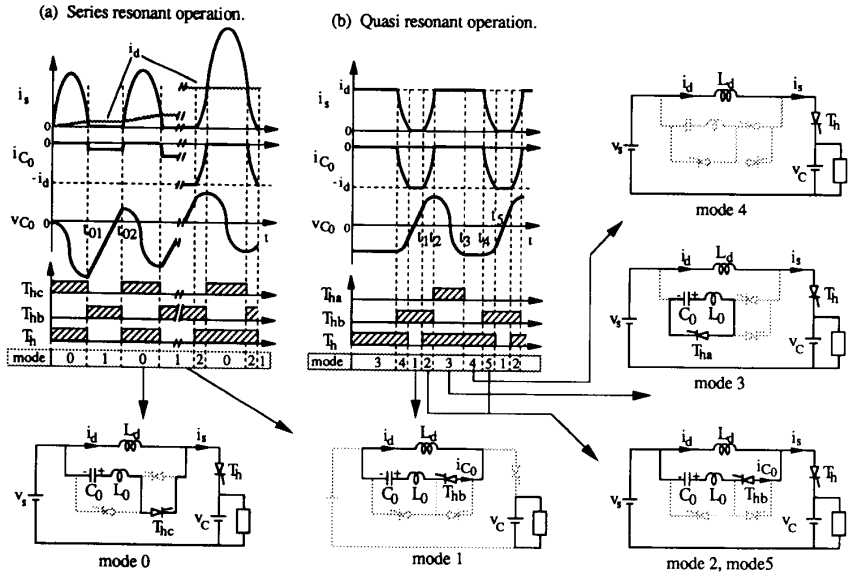

Fig. 3. Modified single phase equivalent circuit and operating waveforms.

C_0, these elements are represented as a voltage source V_s and V_C. Since the inductance L_d is large enough to work as a current source, the resonant frequency is decided by C_0 and L_0. A thyristor T_h represents the four thyristors conducting in series noted in black in Fig. 2. During starting of converter operation, the thyristors T_{hb} and T_{hc} are kept on, while T_{ha} remains off. The system operates as a prototype series resonant converter as shown in Fig. 1 and the operating waveform is shown in Fig. 3(a). After establishing a dc current I_d (= steady state value of i_d; almost constant), quasi resonant operation begins to take place as shown in Fig. 3(b).

These processes can be described as follows according to each mode.

A. Series Resonant Operation

The operation of converter divided into three modes. Waveform of i_d is depicted by the dotted line in the same area of i_s. The periods while thyristors conduct are drawn in oblique lines in the lower part of Fig. 3(a). The first and second pulses express the starting condition and the third one expresses the beginning of steady state operation.

a) Mode 0 ($0 < t < t_{01}$): Initially, C_0 is discharged and no current flows in L_d. The prototype series resonant operation is utilized by triggering thyristors T_h and T_{hc}. The resonant current i_s flows sinusoidally and i_d increases linearly.

b) Mode 1 ($t_{01} < t < t_{02}$): When current i_s reaches zero, thyristor T_h turns off. Subsequently T_{hb} is turned on so that the current i_d flows through T_{hb} and charges C_0 up to the polarity as shown in the figure (mode 1). The resonant capacitor voltage V_{C0} increases linearly. When resonance occurs, the voltage V_s is obtained as follows:

$$V_s = V_d - V_{C_0} - V_{C_L}. \tag{1}$$

When V_s reaches a certain threshold value, mode 0 operation is re-initiated. As i_{C0} has a negative polarity at this instant, mode 2 is entered between mode 1 and mode 0 until i_{C0} reaches zero.

B. Quasi Resonant Operation

After the series resonant operation imposed during starting, quasi resonant operation is ready to begin. When the quasi resonant starts after mode 1, five modes appear during normal operation.

a) Mode 2 ($t_1 < t < t_2$): If V_s reaches the threshold value in the mode 1, T_h is triggered at the beginning of mode 2. During mode 2, i_{C0} increases up to zero and i_s increases up to I_d.

b) Mode 3 ($t_2 < t < t_3$): When i_s equals to I_d, i_{C0} becomes zero and thyristor T_{hb} turns off. At the same time, upon triggering T_{ha}, resonance occurs through C_0 and L_0, and the charge of C_0 changes to the inverse polarity. The resonant current flowing through T_{ha} reaches zero and T_{ha} turns off.

c) Mode 4 ($t_3 < t < t_4$): C_0 and L_0 are separated from L_d and the current i_s flows through L_d. By varying the duration time of mode 4, an optimal current can now be supplied to the load.

d) Mode 5 ($t_4 < t < t_5$): When T_{hb} is triggered again, i_s decreases to zero as i_{C0} flows into C_0. If i_s becomes zero, thyristor T_h is turned off and one resonant process is completed.

A detailed analysis of this circuit operation is presented in the Appendix.

A modified quasi resonant dc link circuit is shown in Fig. 4 which is usable for the quasi resonant operation. A minimum

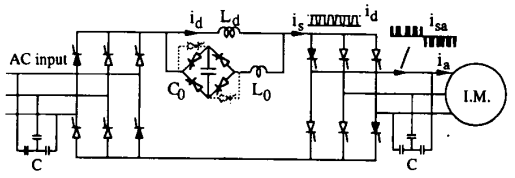

Fig. 4. Modified quasi resonant dc link converter.

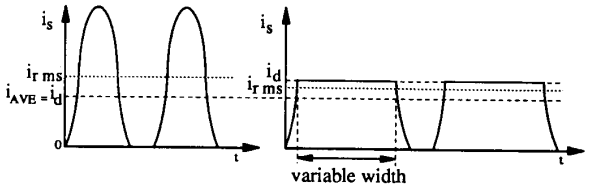

Fig. 5. Example of current pulse waveforms. (a) Basic series resonant waveform. (b) Quasi current resonant waveform.

pulse width can again be generated since there is no need for a reversing time in mode 3 owing to the thyristor bridge.

C. Current Stress of Thyristors

In this system, current stress of thyristors can be reduced in steady state operation. However, during start-up period, this system utilizing prototype series resonant operation, might give relatively high current stresses to thyristors T_{hc} and T_h. The stresses of these thyristors are maintained in low levels by controlling the dc current i_d less than a half of the rated value, so that the current stress can be limited below 1.5 times of rated current. As the start-up period is quite a short time, this value 1.5 remains within the allowance, if considering that the short time current rating of thyristors is usually several times higher than the steady state rating.

Alternately, the peak current stress on T_{ha} becomes as high as in prototype operation even in the steady state. The stress becomes 2–3 times of steady state dc current i_d whereas the average current of T_{ha} is less than that of T_h.

The remaining thyristor T_{hb} has always less value in peak current stress below i_d.

III. Comparisons Between QCRDCL and Basic CRDCL

The resonant current pulse waveforms of QCRDCL and that of basic current resonant dc link (CRDCL) converter are illustrated in Figs. 5(a) and (b), respectively. Both of the average values of current pulses are equal and the duration times of the dead zone between two adjacent pulses are kept equal. As shown in Fig. 5(a), the pulse peak is as high as at least two times of the average current I_d. On the other hand, in Fig. 5(b), the current pulse shape is flat-topped and the pulse width is variable, the limited peak value I_d is much lower than the peak in Fig. 5(a). Also, the rms current becomes lower. Hence, it is clear that the QCRDCL can transfer higher power with low rated switches than with the basic prototype converter.

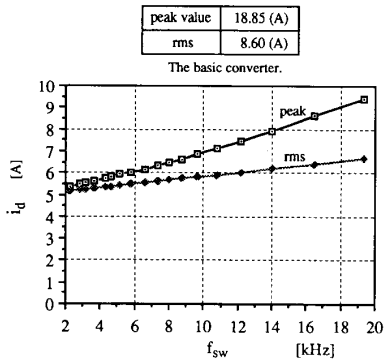

Fig. 6. Peak and rms current of the QCRDCL converter.

To establish the peak and rms current value, simulated results are shown in Fig. 6. The basic prototype converter operates with a 20 kHz switching frequency and the QCRDCL operates at the switching frequency varying from 2 kHz to 20 kHz. Both average output currents and the initial voltages of C_0 at the beginning of the resonance are maintained at the same values of 5 A and 80 V, respectively. The dead zones are adjusted to have a constant value of 30 μs by changing C_0 of the QCRDCL. In the case of the prototype converter, $C_0 = 0.9$ μF and $L_0 = 33$ μH. The peak current of prototype converter was 18.8 A and the rms current was 8.6 A. Comparing to these values, for instance, the peak current and the rms current of QCRDCL were 9.4 A and 6.6 A, respectively, for a switching frequency of 20 kHz. If the switching frequency decreases to 2 kHz, the peak current and the rms current become 5.4 A and 5.2 A, respectively. Accordingly, the peak and rms current clearly decreases under the same average current as the switching frequency becomes lower.

The relationships between the resonant capacitor voltage and I_d are illustrated in Fig. 7. When the link current i_s rises from zero to I_d and subsequently falls in the quasi resonant mode, the energy stored in C_0 is used. To ensure that i_s becomes zero, sufficient voltage must be impressed on v_{C0}. The necessary voltage for v_{C0} is calculated from (8) in the Appendix. The required value is proportional to I_d and becomes smaller as the characteristic impedance Z_0 increases. Since I_d decreases as the switching frequency becomes lower in Fig. 6, if the QCRDCL is operated by lowering the frequency switching, the necessary peak voltage of v_{C0} becomes lower as well.

IV. PWM Control Method

Although various kinds of PWM methods are applicable to QCRDCL, a simple PWM method as shown in Fig. 8 was adopted to investigate the performance of QCRDCL. Using the PWM method, accurate control of the output waveform is possible with moderate frequency of switchings.

In Fig. 8, the reference waveforms and the generated PWM pattern of phase "a" current are shown. The PWM pulse pattern is determined by comparing the reference waveforms

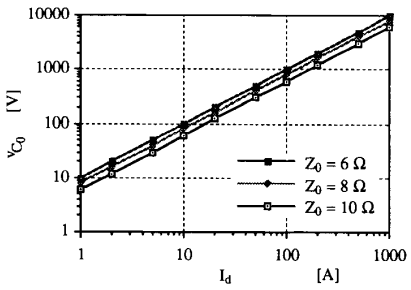

Fig. 7. Necessary voltage of v_{C0} to make i_s into zero.

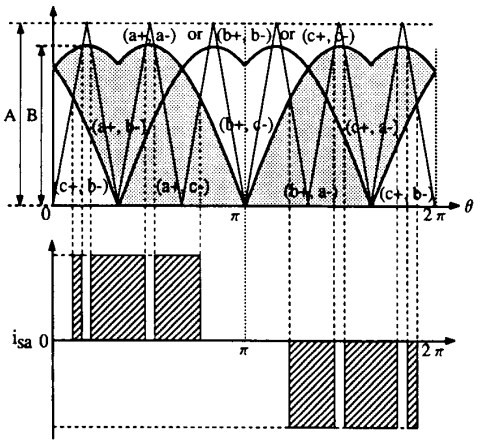

Fig. 8. Reference control waveforms and generated PWM pattern.

with a triangular carrier waveform. The triangular waveform scans over the reference waveforms, and the thyristors to be triggered are selected as noted, e.g., $(a+,\ c-)$ in Fig. 8, according to each scanning area. For $(a+,\ c-)$ case, two thyristors T_{a+} and T_{c-} are triggered. When the carrier wave is scanning over the area noted $(a+, a-)$, $(b+, b-)$ or $(c+, c-)$, upper and lower sides' thyristors of one arm are triggered to realize a short-circuit. For example, PWM pattern of phase "a" produces positive polarity of output current during the carrier wave is passing over the shadowed area on the left, whereas it produces negative polarity of current during the carrier is passing over the shadowed area on the right. The modulation index B/A is the factor that adjusts the amplitude of output sinusoidal current. It is also used to compensate the magnitude loss that happens from the dead-time between resonant pulses as noted "mode 1" in Fig. 3.

When the QCRDCL is controlled by a PWM control, the operation becomes a little different from that of a CSI inverter. To explain this difference, PWM reference waveforms and simulated resonant current waveforms of the QCRDCL are shown in Figs. 9(a) and (b). These traces show the PWM current of the output three phases. The carrier frequency is assumed to be 2 kHz. The figure shows the case that i^*_{sa} continues to flow and i^*_{sb} and i^*_{sc} flow alternately during one cycle period of carrier wave. As shown in the simulated waveforms, the conduction of thyristors does not stop while a current pulse flows.

When other phase thyristor is supposed to conduct, quasi resonance is initiated to stop the currently conducting thyristor momentarily, and the thyristor restores the conduction with the triggering of the supposed thyristor in quasi resonant manner. Therefore, i_{sa} of the QCRDCL in the figure is separated into three parts during one cycle of the carrier wave.

While the output phases change, a dead time exists, and the current does not flow out to the output phases; the current is only circulating in the dc link loop. There are four dead zones during one cycle of the carrier waveform. These dead-times are accumulated, and the compensation is performed in the top area, i.e., $(a+, a-)$, $(b+, b-)$ or $(c+, c-)$, in Fig. 8.

The minimum time difference of A and B in Fig. 8 requires at least the sum of the dead time to perform the compensation. In this simulation, the modulating index B/A was 0.7.

In Fig. 9(b), slight fluctuation of peak value exists on the pulse currents. It is because of that the dc inductance L_d has a finite value, and I_d fluctuates.

As the output voltage is controlled in open loop, the fluctuation of I_d affects the output control. However, the affection to the output current waveform is negligibly small. A similar effect happens also in CSI inverter drives as well by the necessity of a finite link inductance without serious consequences.

V. System Control

Fig. 10 shows the control diagram and circuit configuration. Input three-phase converter is modified into single-phase bridge with dc source to make control simple. In controlling, link current i_d is sensed by hall sensor and compared with i_d reference i^*_d to maintain i_d constant. The timing of generating pulses is determined by the terminal voltage of resonant capacitor C_0. If the voltage of C_0 reaches predetermined threshold value, trigger signals are sent from CPU to gates of thyristors. PWM pattern data are stored in RAM and transferred to CPU.

VI. Resulting Waveforms

A. Simulation Waveform

Fig. 11 shows the results obtained by computer simulation of the three-phase circuit in Fig. 2.

The load is assumed to be a symmetrical three-phase circuit with a 15 Ω resistor for each phase. The output frequency of converter is 30 Hz. The source voltage is balanced three phase at 100 V. The circuit parameters are L_0 = 50 μH, C_0 = 0.5 μF, L_d = 40 mH, C_L = 20 μF, and the carrier frequency is 2 kHz. It is apparent in the figure that smooth sinusoidal output waveforms can be obtained from this circuit concept.

B. Experimental Waveform

At first, experimental result by means of a single phase circuit configuration is shown. Fig. 12 shows waveforms of the resonant current i_s and the resonant capacitor voltage

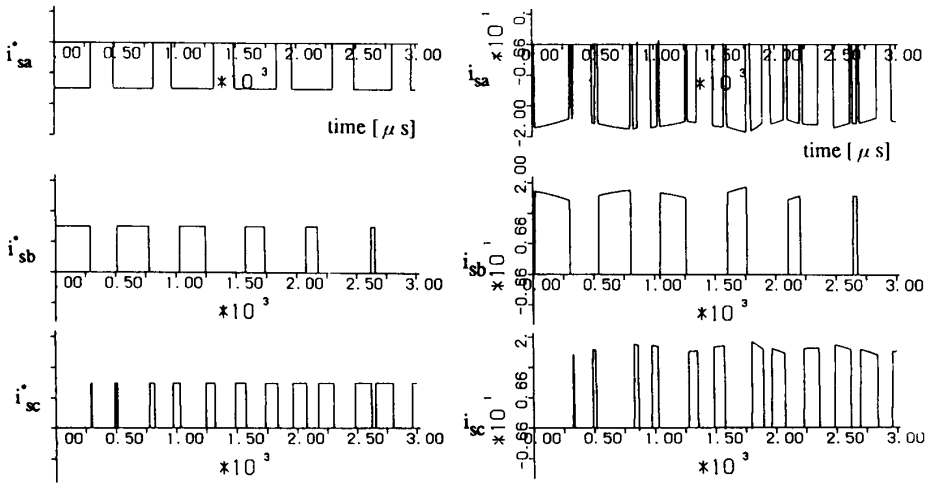

Fig. 9. PWM control reference waveform and resonant current waveforms flowing into output three phases. (a) Reference waveforms. (b) Simulated resonant waveforms.

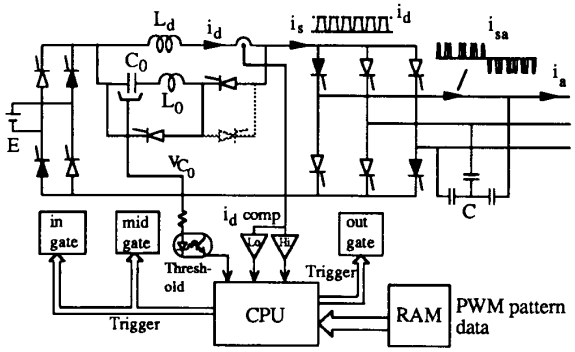

Fig. 10. Control diagram.

v_{C0} of the single-phase equivalent circuit in Fig. 3. The conditions are such that V_d = 80 V and load resistance is 20 Ω. The over-shoot during the rising and falling of i_s are caused because thyristors cannot block the resonant current in this brief moment due to discharge of the storage charge when thyristor makes its reverse recovery. The flat area of v_{C0} after i_s reaches I_d is needed to ensure sufficient turn off time of thyristor T_{hb}. Although the results are of single-phase circuit, these waveforms are quite similar to the waveforms of three-phase operation.

For the three-phase circuit experiment, the main circuit is used as shown in Fig. 4. Though the number of thyristors increases, but PWM control method is precisely implemented due to ability of generating minimum pulses. The circuit parameters used for the experiment are C_0 = 0.3 μF, L_0 = 20 μH, L_d = 40 mH, and C_L = 9 μF. The reference output frequency is 30 Hz and modulation index B/A is 0.75. Under these conditions, the converter is operated with resistor load or induction motor.

Fig. 13 shows the output waveforms for resistor load. Fig. 13(a) is the output line-to-line voltage v_{ab} and Fig. 13(b) is output the line-current i_{sa} which flows from output three phase bridge to the filter capacitors. The experimental conditions are that V_s = 100 V, I_d = 5 A and load resistance are 13 Ω at each of three phases. In Fig. 13(a), although there are slight ripples on the waveform, the frequency of the ripple is high enough to have low distortion sinusoidal waveform. In Fig. 13(b), the waveform i_{sa} consists of a large number of current pulses. The peak of current is maintained almost constant.

Fig. 14 shows the case of driving an induction motor with the ratings of 60 Hz, 200 V, 0.75 kW. The upper waveform is the output line-to-line voltage v_{bc}, and the bottom waveform is the output line current i_a. Both waveforms are well regulated to sinusoidal waveforms.

VII. Conclusion

In this paper, a new quasi resonant current type dc link converter (QCRDCL) was proposed. The features of this new converter are that the generated pulse waveforms are flat-topped and that the pulse width is adjustable. By means of accurate adjustability of pulse width, open loop PWM control was adopted without using any voltage feed back.

The resulting output waveforms are as good as the same quality of conventional CSI inverter. The QCRDCL can also control output accurately with low frequency switching and is very suitable for high power conversion. Since the switching is done by soft switching, the QCRDCL can realize low switching losses with low EMI.

In this paper, an open loop PWM control was adopted to simplify the control and to evaluate the fundamental capability of the QCRDCL. In order to improve the output control under a wide range of load conditions advanced controls are under investigation.

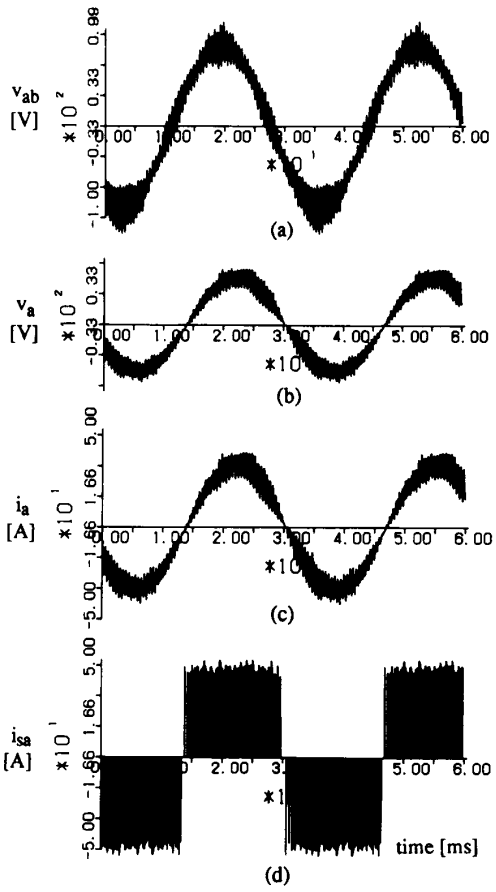

Fig. 11. Simulated output waveforms.

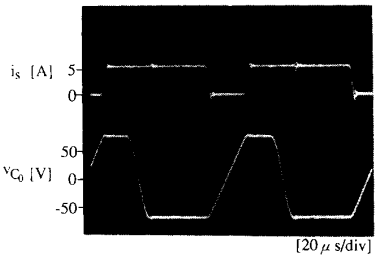

Fig. 12. Experimental waveforms. (Single phase.) (a) Line-to-line voltage v_{ab}. (b) Line current i_{sa}.

APPENDIX
ANALYSIS OF CIRCUIT OPERATION

To analyze fundamental operation of the QCRDCL, a single-phase equivalent circuit can be utilized. It is assumed that all of the devices and components are ideal. During the initial start-up condition, current I_d flows into L_d and voltage v_{C0} is applied to C_0. The moment that T_h is triggered, the voltage which emerges across T_h is

$$V_s = V_d - V_{C_0} - V_{C_L} \tag{1}$$

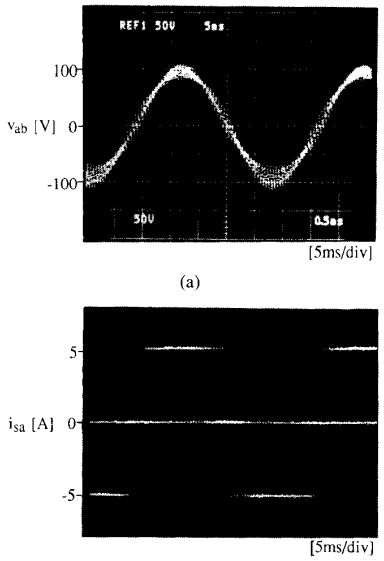

Fig. 13. Output waveforms. (Three-phase resistor load.) (a) Line-to-line voltage v_{ab}. (b) Line current i_{sa}.

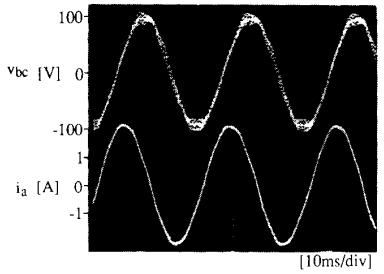

Fig. 14. Output waveforms. (Three-phase induction motor.)

and the circuit equations become

$$E = L_d \frac{di_d}{dt} + V_s \tag{2}$$

$$L_d \frac{di_d}{dt} = \frac{1}{C_0} \int i_0 dt + L_0 \frac{di_0}{dt}.$$

The resulting current i_s during mode 2 is obtained as follows:

$$i_s(t) = \frac{V_s}{Z_0} \sin \omega_0 t + I_d(1 - \cos \omega_0 t) \tag{3}$$

$$v_{C_0} = v_{C_0(t=t_1)} - V_s \cos \omega_0 t - I_d Z_0 \sin \omega_0 t \tag{4}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_0 C_0}} \tag{5}$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}}. \tag{6}$$

The duration time of mode 2, or the time interval $[t_2 - t_1]$, is

$$t_2 - t_1 = \frac{1}{\omega_0} \tan^{-1} \frac{I_d Z_0}{V_s} \tag{7}$$

and the value of v_{C0} at time t_2 is

$$v_{C_0}(t_2) = v_{C_0(t=t_1)} - \sqrt{V_s^2 + I_d^2 Z_0^2}. \tag{8}$$

This becomes the maximum value of v_{C0}.

During mode 3, or the time interval $[t_3 - t_2]$, the equations of the circuit are obtained as follows:

$$i_a(t) = \frac{V_s}{Z_0} \sin \omega_0 t \tag{9}$$

$$v_{C_0}(t) = v_{C_0(t=t_2)} - V_s \cos \omega_0 t. \tag{10}$$

The time interval $[t_3 - t_2]$ is

$$t_3 - t_2 = \pi \sqrt{L_0 C_0}. \tag{11}$$

During mode 4, current i_s flows through L_d so that $i_s = I_d$. During the mode 5, the equations for i_s and v_{C0} are described as follows:

$$i_s(t) = \frac{V_s}{Z_0} \sin \omega_0 t + I_d \tag{12}$$

$$v_{C_0}(t) = v_{C_0(t=t_4)} - V_s \cos \omega_0 t. \tag{13}$$

The time interval $[t_5 - t_4]$ is

$$t_5 - t_4 = \frac{1}{\omega_0} \sin^{-1}\left(-\frac{I_d Z_0}{v_{s(t=t_4)}}\right). \tag{14}$$

During mode 1, v_{C0} is charged by i_d up to the required voltage to generate the next resonant pulse. Assuming that i_d is almost constant, the equations are obtained as follows:

$$i_s(t) = 0 \tag{15}$$

$$v_{C_0}(t) = v_{C_0(t=t_5)} - \frac{I_d}{C_0} t. \tag{16}$$

The time interval $[t_6 - t_5]$ is

$$t_6 - t_5 = \frac{C_0}{I_d}\left(v_{C_0(t=t_6)} - v_{C_0(t=t_5)}\right). \tag{17}$$

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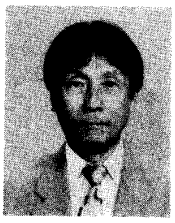

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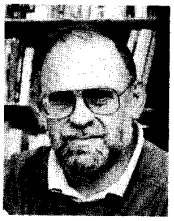

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