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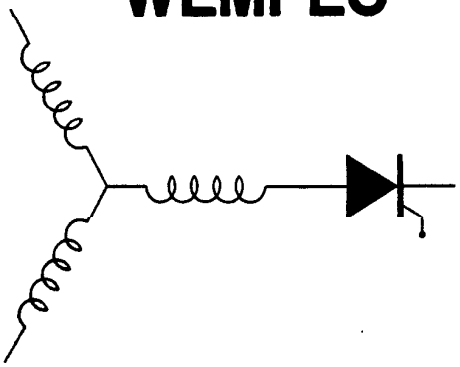

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DC LINK NOTCHING CURRENT INVERTER WITH SOFT COMMUTATION

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ABSTRACT

This paper presents a new dc link notching current inverter with zero-current switching for realizing a current source motor drive. When desired, resonant transition creates notches in the link current, allowing the converter's switches to commutate at zero current crossing and to synchronize with PWM strategy. A regulated dc current source may be obtained by using a conventional rectifier bridge. Compared with traditional PWM current source inverters, performance and efficiency in this inverter is an improvement because high frequency switching occurs at zero current crossings. The paper presents design considerations for the resonant elements and discusses a control strategy for the notched inverter. Simulation results for a three-phase induction motor driven by such inverter are presented. Moreover theoretical analyses and simulation results of a simplified model are verified by comparison with experimental results.

Keywords: current source inverter, inverter, resonant transition; soft commutation

1. INTRODUCTION

An induction motor drive based on current source inverters presents advantages of simple structure, easy regenerative braking implementation and inherent protection against short-circuit [Bose, 1982; Ledwich, 1992]. A conventional current source is dependent on load and suffers from severe torque pulsations at low speeds [Lipo, 1978; Lienau, 1979]. With the use of self turned-off semiconductor switches, such as GTOs, different strategies of PWM to control output current have appeared [Ohnishi, 1983; Hombu, 1985]. Capacitors connected to ac output terminals absorb the overvoltage that occurs when current is cut-off and, acting as filter, helps reduce harmonics in output currents [Hombu, 1985]. Nevertheless, most of GTO based inverters suffer from hard commutation and its attendant disadvantages.

Recently, series resonant dc-link converters were introduced to help reduce device switching losses [Murai, 1988; Caldeira, 1990]. An alternative converter uses the capacitors connected to the output terminals as resonant capacitors, thus using fewer components than previous circuit [Park, 1989], but operating on a lower limit frequency. Switching, in these converters, occurs only at zero crossing instants of the link current. Nevertheless, these both dc link series resonant converters operate at constant frequency and cannot operate with conventional PWM strategies.

In contrast to series resonant link converters, which resonante through the switches of the rectifier and inverter, the proposed converter described in this paper uses an auxiliary commutation circuit to divert current from dc link. To accomplish this current diversion, dc side commutation is used. Although this technique is well-known, it has mainly be used with voltage source inverters [Aldana, 1978; Rashid, 1988]. To our knowledge, its only application to control current at an inverter was made to provide forced commutation in HVDC inverters [Sood, 1984; Po, 1989]. In the proposed circuit, notches are produced in dc link current such that inverter switches commutate at zero current, and capacitors connected to ac output terminal make operation less dependent on load. Resonant transition provides a quasi square-waveform for dc link current pulses.

Self turned-off switches used in the inverter may be GTOs, IGBTs or BJTs. Because auxiliary circuit may provide enough turn-off time, SCRs may be also used if the converter is intended to operate at very high power levels. Comparing with traditional PWM current source inverters, performance and efficiency of this dc link notching current inverter are greatly improved because high frequency switching occurs at zero current crossings. Furthermore, PWM synchronization and soft commutation are obtained by addition of only two switches to the conventional GTO inverter. Simulation results for driving a three-phase induction motor with such inverter are presented. Experimental results verify theoretical and simulation results of a single-phase circuit model.

2. OPERATION AND ANALYSIS OF PROPOSED CIRCUIT

Fig.1 shows the proposed dc link current notching inverter. The auxiliary commutation circuit diverts the current flowing through filter inductor L_d by firing switch T_r. The polarity of capacitor C must be negative in relation to the polarity shown in Fig.1. As a result, a notched current flows at output of the rectifier and at input of the inverter.

2.1. Principle of Operation

Principle of operation may be described with the help of the equivalent circuit shown in Fig.2, making the following assumptions:

(a) Load current is constant during commutation period

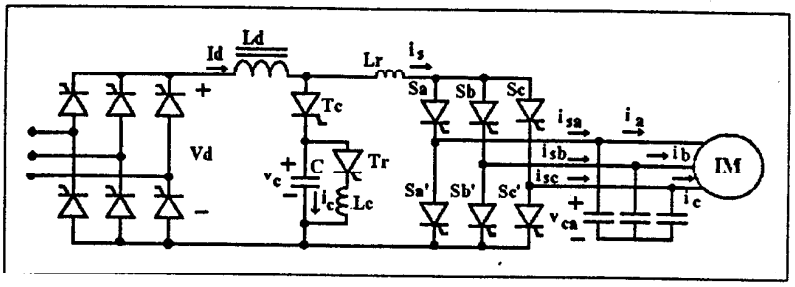


Fig.1. DC link notching current inverter

(b) Switching devices and resonant components are ideal
(c) Inductor L_d is much greater than resonant inductor L_r
(d) During switching time, v_o is constant and equal to V_o

Under these assumptions, six modes are identified during an operation cycle, as shown in Fig.3. It should be noticed that T_s, in Fig.2, is equivalent to two switches in series (from the inverter).

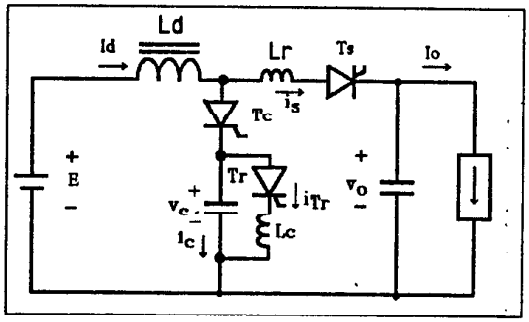


Fig.2. Simplified circuit

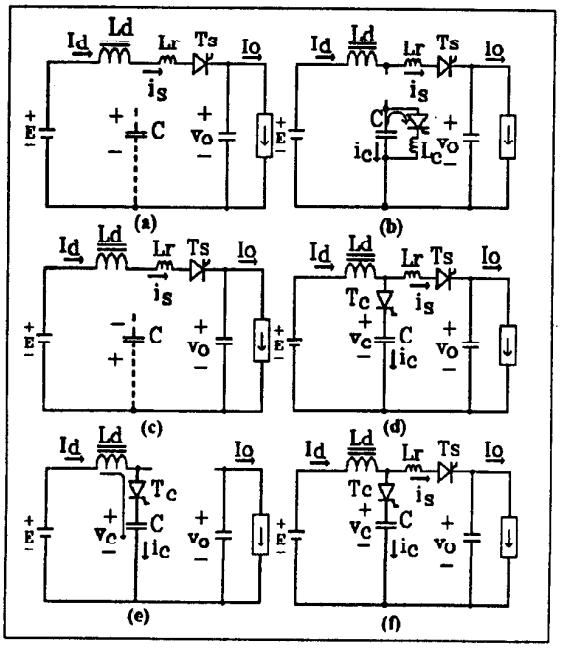


Fig.3. Modes of operation for Circuit in Fig.2

In **mode I** (power mode) current Id is flowing through L_r, T_s and load and

$$i_o = i_s = I_d$$
$$v_o = V_o \qquad (1)$$
$$v_c = V_o = +V_c$$

When T_c is fired, at instant t_1, **mode II** (polarity reversal mode, Fig.3b) starts a resonance between C and L_c. Then capacitor voltage v_c oscillates from $+V_c$ to $-V_c$, if losses in resonant circuit are neglegible. After reaching its peak value, I_p, resonant inductor current falls down and becomes null at instant t_2 in Fig.4. Equations for this mode are:

$$i_c = -i_{Lc} = -I_p \sin(\omega_c t)$$
$$v_c = V_c \cos(\omega_c t) \qquad (2)$$
$$i_s = I_d$$

where $I_p = \frac{V_c}{\omega_c L_c}$ e $\omega_c = \frac{1}{\sqrt{L_c C}}$.

Mode III (Fig.3c) is similar to mode I.

Mode IV (first resonant transition mode, Fig.3d) starts when switch T_c is fired, at instant t_3. Then current in L_r is transfered to capacitor C. Initial conditions for this mode are:

$$v_c(0) = -V_c, i_c(0) = 0, \text{ and } i_s(0) = I_d = I_o$$

Principal equations are:

$$i_c = \frac{V_c+V_o}{\omega_r L_r} \sin(\omega_r t)$$
$$v_c = -(V_c + V_o)\cos(\omega_r t) + V_o \qquad (3)$$

where $\omega_r = \frac{1}{\sqrt{L_r C}}$ is the resonant frequency of the circuit T_s-V_o-T_c-C-L_r. This mode ends at $t=t_4$, when current i_c reaches the value of I_d and current i_s becomes zero. Final value for v_c is

$$V_e = -\sqrt{(V_c+V_o)^2 - \left(\frac{\omega_r L_r I_o}{V_c+V_o}\right)^2} + V_o \qquad (4)$$

It can be seen that necessary condition for a successful commutation is

$$\frac{V_c+V_o}{\omega_r L_r} \geq I_o \qquad (5)$$

Mode V (zero current mode, Fig.3e) starts when current I_d is completly transfered from L_r to the branch C-T_c. Then v_c charges linearly as

$$v_c = \frac{I_o}{C}t - V_e \qquad (6)$$

This is a very important mode for stable operation of the circuit. Thyristor T_s is ensured to be off only if the interval of time in which reverse voltage is applied to its terminals (circuit turn-off time) is larger than the device turn-off time t_q. As $v_{Ts}=E+v_c-V_o$, circuit turn-off time is

$$t_o = \frac{\left[2V_o - \sqrt{(V_c+V_o)^2 - (\omega_r L_r I_o)^2}\right]C}{I_o} \qquad (7)$$

For $t_o > t_q$, minimal value for capacitance C is given by

$$C = \frac{I_o t_q}{2V_o - \sqrt{(V_c + V_o)^2 - (\omega_r L_r I_o)^2}} \quad (8)$$

and establishes the limit of stable operation. The end of this mode is established by the control circuit, which defines at what voltage v_{Ts} switch T_s must be fired ($t=t_6$).

During mode V capacitor C charges linearly. From the instant in which $E-v_c-V_o$ becomes positive, thyristor T_s may be fired. Firing T_s starts mode VI (second resonant transition mode, Fig.3f) with current transfer from auxiliary commutation circuit to circuit L_r-T_s-load. Then,

$$i_c = I_o \sin(\omega_r t)$$
$$v_c = \omega_r L_r I_o \sin(\omega_r t) + V_o \quad (9)$$

During this mode (t_7-t_6) a capacitor overvoltage occurs and final value for v_c is

$$V_c = V_o + \omega_r L_r I_o \quad (10)$$

Principal waveforms are shown in Fig.4.

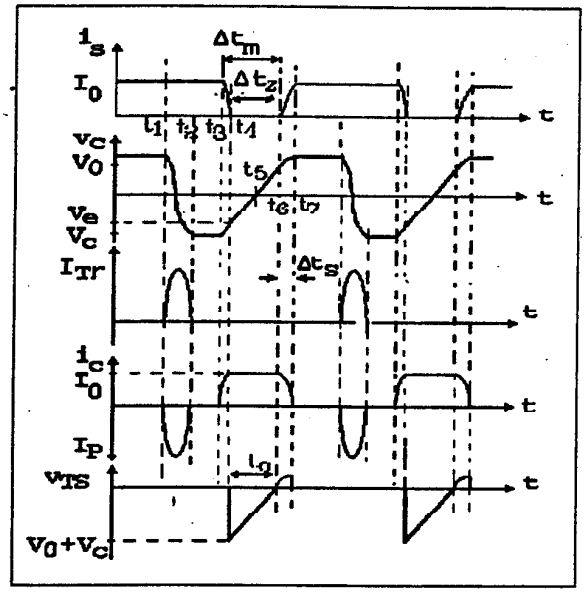


Fig.4. Principal waveforms in Fig.2c

3. DESIGN PROCEDURE

Some parameters are very important for design procedures:

a) reduction of zero current interval, Δt_z, reduces overvoltage on capacitor terminals; nevertheless, the type of switch used imposes a minimal value of Δt_z; use of modified GTO [Mertens, 1991] or IGBT [Ferrieux, 1989] in thyristor mode allows the circuit to operate at higher frequency because, in this case, tail current is pratically null and turn-off time quite reduced;

b) zero current and turn-off resonant transition time intervals determine minimal width. Δt_m, between firing instants for switches T_c and T_s;

c) reversal of capacitor polarity imposes minimal conduction time for ΔT_s, which depends on maximal peak current in T_r, i.e., on L_c value; it also determines minimal time interval between firing instants for T_r and T_c;

d) commutation total time, t_t, determines maximum frequency;

e) energy W in commutation capacitor guarantees commutation.

These parameters may be obtained as a function of $x=\omega_r L_r I_o/V_o$ and $k_L=L_c/L_r$, as follows.

Circuit turn-off time:

$$\frac{t_o I_o}{C V_o} = 2\left(1 - \sqrt{1+x}\right) = f(x) \quad (11)$$

Commutation capacitance:

$$\frac{C_o V_o}{I_o t_o} = \frac{1}{f(x)} \quad (12)$$

Commutation energy:

Energy $CVc^2/2$ may be normalized in terms of $EI_o t_o$ as

$$\frac{W}{EI_o t_o} = \frac{(1+x)^2}{4\left(1 - \sqrt{1+x}\right)} \quad (13)$$

Peak current:

$$\frac{Ip}{Io} = \frac{(1+x)}{x\sqrt{k_L}} \quad (14)$$

Total commutation time:

$$\frac{t_t}{t_o} = \frac{x\left[\frac{\pi}{\sqrt{k_L}} + \arccos\sqrt{1-\left(\frac{x}{2+x}\right)^2} + h(x) + \frac{\pi}{2}\right]}{2\sqrt{1+x}} \quad (15)$$

where $h(x) = \left(1 + 2\sqrt{1+x}\right)x$

Interval between firing pulses of T_c and T_s

$$\omega \Delta t_m = \arccos\sqrt{1-[x/(2+x)]^2} + h(x) \quad (16)$$

Capacitor voltage is influenced by the zero current interval and can be expressed as:

$$\frac{V_{cf}}{V_o} = 2\left[\frac{\Delta t_e}{\Delta t_z} - 1\right]\left(\sqrt{x+1} - 1\right) + x \quad (17)$$

where V_{cf} is final voltage for a zero current time interval Δt_e.

Fig.5 shows that behavior of reverse time, t_o, total commutation time, and voltage V_{cf} is in conflict with behavior of capacitance value, C, commutation energy, W, and current peak in switch T_c. Hence, an adequate choice of x must be made.

4. INVERTER CONTROL STRATEGY

In general, inverter units requires PWM control to produce sinusoidal voltage and current. Moreover, the inverter requires frequency and phase angle control corresponding to motor speed. For a precise control of current in each phase, and to avoid overvoltage, only one switch in the upper three legs and only one switch in the lower three legs of the inverter are allowed to conduct current simultaneously.

There are some excellent methods creating PWM pulse patternfor current inverters but they are based on the synchronized operation between the carrier and output frequencies [Ohnishi, 1983; Hombu, 1985; Nonaka, 1987]. Also, operation based on a constant frequency irrespective of the output frequency has been introduced in literature[Fukuda,1988], The space vector technique used here has a different approach and is an adaptation of a method used

to control voltage source inverters [Van der Broeck, 1986].

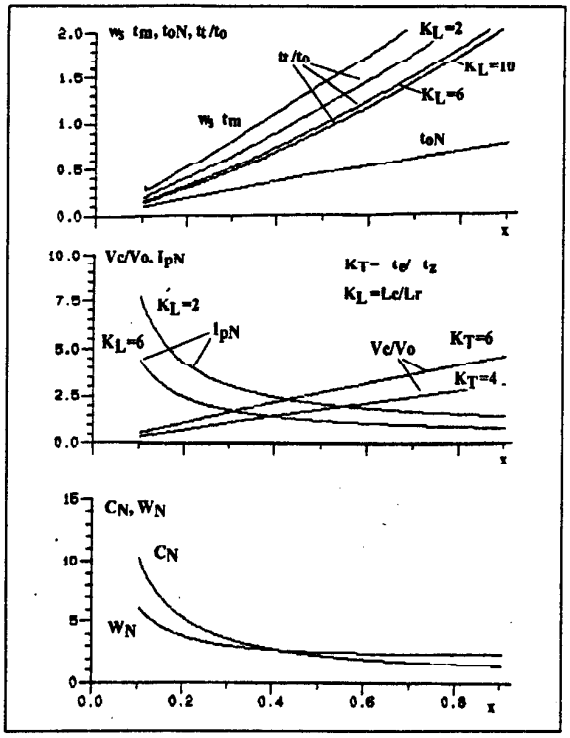


Fig.5. Normalized parameters

4.1. The inverter output current as a space vector

Conceptually, a set of three phase waveforms can be represented by a single rotating vector. Applying this concept to a three phase current source inverter, it can be seen in Fig. 6 that there are seven possible output current states. One of these is the null current vector I_0, which occurs when a shoot-through state is provided (I_0) or current is zero at dc-link (I_7). Remaining six active vectors (I_1 to I_6) have the same length $\sqrt{3}\ I_d$ (I_d=amplitude of dc-link current) and are each spatially displaced 60° degrees apart.

The technique involves vectorially equating volt-second integrals between a desired reference and the output current vector realizable by the inverter. Active vectors I_k and I_{k+1}, for k=1...6, are adjacents. If one reference vector is located at any of the six possible sectors K (K=1,2,3,4,5,6), two adjacent active vectors are selected. Application time for each one of these vectors may be calculated such that, during time interval T, an average vector equals the reference vector.

For location of reference vector in Fig. 6, equation relating the volt-second integrals of vectors I_1 and I_6 to that of reference I* is given as

$$I^*T=I_6.t_6+I_1.t_1 \qquad (18)$$

where t_1 and t_6 are application times of vectors I_1 and I_6, respectively. Usually, t_1+t_6 is smaller than T. So zero vectors, which do not contribute to average vector, are added for the rest of time $t_0=T-t_1-t_6$. It should be noticed that, with this strategy, frequency of operation is 1/(2T).

Different switching patterns are possible for vectors I_k, I_{k+1} and I_0 during interval T [Van der Broeck, 1986; Nabae, 1989]. When only one pattern is used for any operating point, ideal pattern (if vectors I_k, I_{k+1} and I_0 are applied for more than one interval of time T) is

$$\begin{aligned}&[I_0.(t_0/2)-I_k.(t_k)-I_{k+1}.(t_{k+1})-I_0.(t_0/2)] \quad \text{for } 0<t<T\\ &[I_0.(t_0/2)-I_{k+1}.(t_{k+1})-I_k.(t_k)-I_0.(t_0/2)] \quad \text{for } T<t<2T\end{aligned} \qquad (19)$$

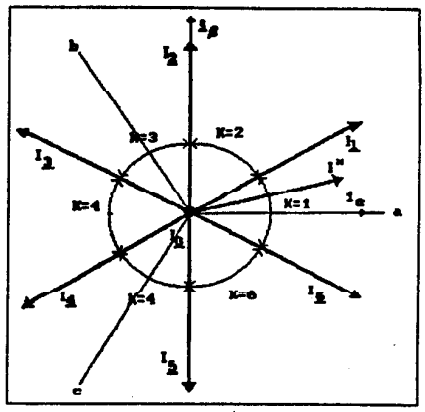


Fig.6. Current vector diagram

4.2. Detection for the sector to which reference belongs

Once reference vector is known, its angle with reference axis s_a may be used to determine sector K and adjacent active vectors I_k, I_{k+1}. If three phase components of I* (Ia*, Ib* and Ic*) are available, then a simple signal test is sufficient to determine sector and active vectors:

If Ia*>0 and Ib*<0 and Ic*<0, then K=1 and k=6, k+1=1;
If Ia*>0 and Ib*>0 and Ic*<0, then K=2 and k=1, k+1=2;
If Ia*<0 and Ib*>0 and Ic*<0, then K=3 and k=2, k+1=3;
If Ia*<0 and Ib*>0 and Ic*>0, then K=4 and k=3, k+1=4;
If Ia*<0 and Ib*<0 and Ic*>0, then K=5 and k=4, k+1=5;
If Ia*>0 and Ib*<0 and Ic*>0, then K=6 and k=5, k+1=6.

Times t_k and t_{k+1} may be calculated by equation (18) in polar form or in terms of their cartesian components of reference current (Iα*, Iβ*), method which is used here (Fig.6). Then,

$$\begin{aligned}t_k&=A[(I\alpha^*\sqrt{3}/2+I\beta^*/2).\sin(k\pi/3)-\\ &\qquad (-I\alpha^*/2+I\beta^*\sqrt{3}/2).\cos(k\pi/3)]\\ t_{k+1}&=-A\{(I\alpha^*\sqrt{3}/2+I\beta^*/2).\sin[(k-1)\pi/3]-\\ &\qquad (-I\alpha^*/2+I\beta^*\sqrt{3}/2).\cos[(k-1)\pi/3]\}\\ t_0&=T-t_k-t_{k+1}\end{aligned} \qquad (20)$$

where $A=\sqrt{\frac{2}{3}}\ (T/I_d)$.

As trigonometric functions assume six different values (1<k<6), they can be previously calculated.

4.3. Considerations related to the proposed circuit

Some characteristics have been presented specific to the commutation circuit used:

a) overvoltage on the capacitor terminals requires, as already mentioned, a minimal zero current interval, Δt_z, determined by the switch used;

b) capacitor polarity reversion requires a minimal pulse width.

On the other hand switches of inverter are switched at zero current, vector I_7. By considering interval Δt_z as constant, pattern (19) becomes:

$$\begin{aligned}&[I_0.(t_0'/2)-I_7.(\Delta t_z)-I_k.(t_k)-I_7.(\Delta t_z)-I_{k+1}.(t_{k+1})\\ &\qquad -I_7.(\Delta t_z)-I_0.(t_0'/2)] \text{ for } 0<t<T\\ &[I_0.(t_0'/2)-I_7.(\Delta t_z)-I_{k+1}.(t_{k+1})-I_7.(\Delta t_z)\\ &\qquad -I_k.(t_k)-I_7.(\Delta t_z)-I_0.(t_0'/2)] \text{ for } T<t<2T\end{aligned} \qquad (21)$$

where $t_0'=t_0-3\Delta t_z$.

At limit of operation, if $t_0'<0$ then t_k and t_{k+1} must be replaced by $t_k+t_0'/2$ and $t_{k+1}+t_0'/2$, respectively, and t_0' null.

4.4. Rectifier Control

Regulation of current in bias inductance can be obained by phase control of input rectifier

5. CIRCUIT VARIATION

Zero current interval of proposed circuit is dependent on dc link current Id and capacitor voltage at the moment in which auxiliary switch is fired. A variation of auxiliary commutation circuit, which is less dependent on dc link current and commutation capacitor voltage, is presented in Fig.7. Firing T_a resonates capacitor current i_c and provides an almost constant reverse voltage for all switches at the inverter.

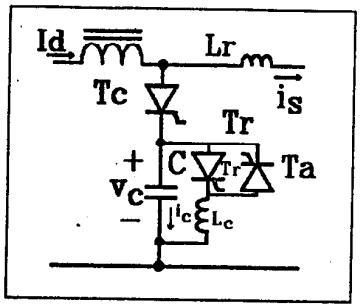


Fig. 7. The modified commutation circuit

6. SIMULATION AND EXPERIMENTAL RESULTS

In order to check the theoretical analysis, the operation of the dc link notching current inverter was simulated and an experimental prototype implemented.

Simulation results for principal waveforms in Fig.2 are shown in Fig.8. For simulation of the three phase notching current inverter, operating with vector control, an induction motor was used as load. Fig.9 shows simulation results of inverter phase current, i_{as}, and phase voltage v_{as} and current i_a of induction motor.

Fig.10 shows the experimental link current i_s, voltage on switch T_a, v_{Ta}, and voltage on commutation capacitor, v_c, of the simplifed single-phase prototype of circuit in Fig.2. This prototype, rated for 100V output capacitor voltage and 4.5A of load current, operated at 3 kHz with SCRs of 15μs of turn-off time. Disadvantage of using a slow device such as SCR is shown in Fig.10. Reverse peak in current i_s (upper trace in Fig.10a) and voltage oscillations v_{Ta} (bottom trace in Fig.10b) exist because of SCR's turn-off time.

7. CONCLUSION

The paper has presented a dc link notching current inverter. Current pulses, which are quasi-square waves, may have variable width and are obtained with the help of a notching circuit in the dc link. As a result, inverter switches operate at zero current. For that, only a few number of additional components is needed when compared with conventional GTO version. Because of zero current switching, SCRs may be used for implementation at higher power levels, but use of faster self-turned-off devices, as modified GTO or IGBT, allow higher frequency limit of operation for the inverter. A disadvantage of the scheme is that even though the inverter operates on high frequency, under vector control, the rectifier is phase controlled at line frequency and, so, it is not possible to obtain sinusoidal input currents. A simplified circuit of the proposed scheme was simulated and experimental tests verified theoretical studies. Finally, a topology that makes zero current period less dependent on commutation capacitor voltage and dc link current peak, is also indicated. Topologies that allows to control input currents and power factor, through high frequency switching of the input converter, are under investigation.

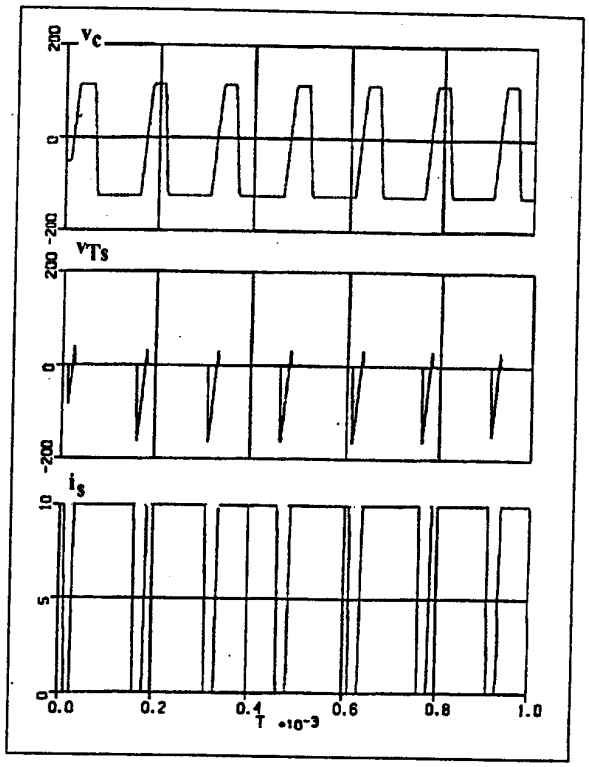


Fig. 8. Simulation results for the equivalent circuit of Fig.2

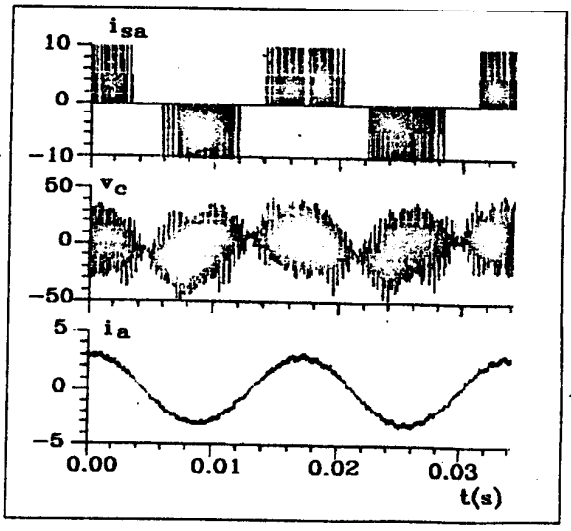


Fig. 9. Simulated waveforms for three phase operation

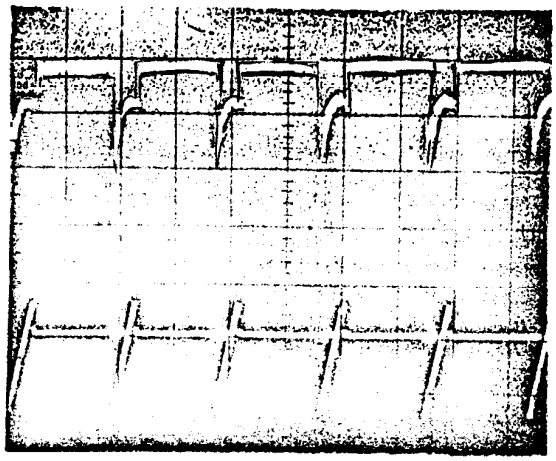
APPENDIX

a) Parameters in induction motor simulation:

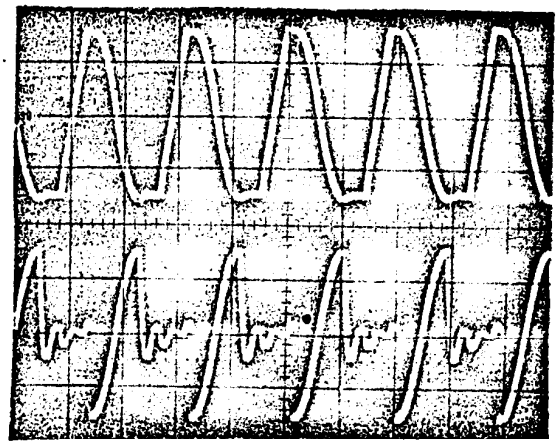
R_s=0.39Ω, Rr=1.41Ω, L_s=0.094μH, L_r=0.094μH, M_{sr}=0.091μH

b) Parameters of commutation elements in experimental results:

L_r=60 μH, L_c=600 μH, C=2.5 μF



(a) upper trace: current i_s (vert. scale: 5A/div)
bottom trace: voltage v_{T_2}; vert. scale: 100V/div



(b) upper trace: capacitor voltage ,v_c (vert. scale: 100V/div)
bottom trace: Lc voltage, v_{Lc}(vert. scale:100V/div)

Fig.10. Experimental results (hor. scale: 200 μs/div)

REFERENCES

1. Bose, B.K. (1982). "Adjustable speed ac drives - A technology status review", Proc. of IEEE, Vol. 70, N. 2, pp. 116-135.

2. Caldeira, P. (1990). "High frequency series resonant dc link power conversion system", Ph.D. thesis, University of Wisconsin-Madison.

3. Ferrieux, J.P. (1989). "The insulated gate bipolar transistor; switching modes", Proceedings of European Power Electronics Conference, pp.171-175.

4. Fukuda S., and Hasegawa, H. (1988). "Current source rectifier/inverter system with sinusoidal currents", IEEE PESC'88 Conference Record, pp. 909-914.

5. Hombu, M. et alii. (1985). "A new current source GTO inverter with sinusoidal output voltage and current", IEEE Trans. Ind, Appl., Vol. IA-21, N. 5., Sept./Oct., pp. 1192-1198.

6. Ledwich, G. (1992). "Current source inverter modulation", to appear in IEEE Trans. on Power Electronics.

7. Lienau, W. (1979). "Torque oscillation in traction drives with current fed asynchronous machines", IEE Conference Publication, N. 79, Electrical Variable Speed Drives, pp. 102-107.

8. Lipo,T.A. (1978). "Analysis and control of torque pulsations in current-fed motor drives", IEEE PESC'78 Conference Record, pp. 89-96.

9. Mertens, A., Skudelny, H. Caldeira, P., and Lipo. T.A. (1990). "Characterization of GTOs under different modes of zero current switching", IEEE IAS'90 Record Conference

10. Murai Y. and Lipo, T.A. (1988). "High frequency series resonant dc link power conversion", IEEE-IAS Annual Meeting Conference Record, pp. 772-779.

11 Ogasawara, S., Akagi, H., and Nabae, A. (1989). "A novel PWM scheme of voltage source inverters based on space vector theory", European Power Electronics Conf. Record, pp. 1197-1202.

12. Ohnishi, T. and Okitsu, H. (1983). "A novel PWM technique for three phase inverter/converter", IPEC'83 Conference Record, pp. 384-395.

13. Park, S. and Cho, G. (1989). "A current regulated pulse width modulation method with new series resonant inverter", IEEE/IAS Annual Meeting Record, pp. 1045-1051.

14. Van der Broeck, H.W., Skudelny, H. Ch., and Stanke, G. (1986). "Analysis and realization of a pulse modulator based on voltage space vectors", IEEE IAS'86 Conference Record, pp. 244-251.