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A PWM High Frequency Series Resonant DC Link Converter and Its Utilization as a DC Motor Drive

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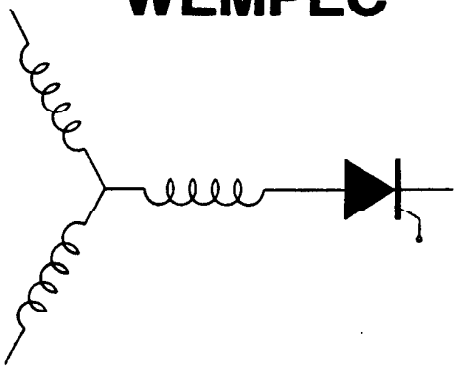

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A PWM HIGH FREQUENCY SERIES RESONANT DC LINK CONVERTER AND ITS UTILIZATION AS A DC MOTOR DRIVE

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The pulse width modulated series resonant dc link converter introduces a pwm control in the series resonant dc link converter. The scheme is able to operate with reduced switching losses at a high switching frequency. Synchronization capability allows to develop suitable modulation techniques to improve input current waveforms. Different strategies for armature current regulation is examined. Simulation and experimental results verify the use of the converter as a dc motor drive.

Introduction

In the past, most of dc motor drive used thyristor rectifiers with phase control. Nowadays, faster turn-on and turn-off controlled switches are utilized in a chopper that follows an uncontrolled rectifier [1] or in a conventional converter power circuit [2]. Although some structures use soft switching [1], most of schemes proposed in the technical literature are hard switched or use too many components.

In the last five years, remarkable progress has been made in the development of resonant link converters [3]. These converters are unique in that they allow devices to switch at zero voltage or zero current crossing. Recently, a high frequency series resonant dc link converter (SRDCLC) was used to drive a dc motor [4]. Resonant pulses of 20 to 35 kHz are distributed in the input phases corresponding to the system requirements such as low harmonic content and complete control of the input power factor including the distortion and displacement factors. Consequently, nearly sinusoidal fundamental input current can be obtained, with improved harmonic content. Also, efficiency is greatly improved when compared with hard-switching schemes. However the resonant pulse constitutes its control unit. In this case low frequency errors, introduced in the regulation of the armature (dc link) current, are difficult to be eliminated. On the other hand PWM techniques can eliminate these errors without much difficulty.

More recently, a paper introduced a new soft switching converter, which retains the advantages of the SRDCLC but allows switching instants that can be synchronized to a PWM type of strategy [5]. In both series resonant converters a stiff inductor provides dc bias to realize pulsating dc currents.

This paper presents the PWM high frequency series resonant converter (PWM-SRDCLC) operation and its utilization as a dc motor drive. It also shows that a slight modification in the basic structure improves its performance. Experimental results verify the basic operation of one version of the dc motor drive.

Principles of operation

The basic schematic of the PWM-SRDCLC feeding a dc motor placed in series with the bias inductor Ld, is shown in Fig.1. Although switches in Fig.1 are represented by GTOs, any switch with controlled turn-on and turn-off but operating on thyristor mode (zero current switching) can be used. If higher power is required, SCRs can also be used. L_d. The pulse width modulation feature is implemented by the addition of the diode D_a and the thyristor S_a to a series resonant link converter [5].

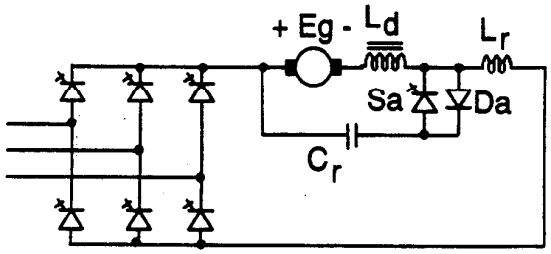


Fig.1 PWM series resonant dc link converter as a dc motor drive

Suppose, initially, that the auxiliary GTO (S_a) is turned on all time and operates like a diode. This is equivalent to a short-circuit in the set D_a/S_a and corresponds to a SRDCLC operation [5]. Through an adequate choice of GTO turn-on in the bridge, a positive voltage is applied to the link. A dc offset I_d, provided by inductor L_d, is added to the ac resonant current in L_r and C_r resulting in the generation of a high frequency resonant current pulse. As the resonant current i_r returns to zero one or two switches in the bridge are turned off. As a consequence, the bias current I_d, which is also the

armature current, is completely transferred into C_r causing a linear discharge of the capacitor voltage. When an adequate positive voltage (V_{swt}) is applied to the switches they are triggered again and a new current pulse is generated. This positive bias voltage V_{swt} across the devices increases the system stability ensuring that the resonant pulses reach zero in each cycle. It also ensures the application, at turn-off, of a negative voltage across the devices with a value equal to V_{swt}. It can be observed that no special operating mode is needed during start up; at the beginning, the capacitor C_r and inductors L_r and L_d are completely discharged but since first resonant pulse the system is already in the charging mode.

The high resonant frequency determined by the resonant elements L_r and C_r imposes the maximum operation frequency. In reality, this limit switching frequency is always slightly lower than the resonant frequency due to an additional time needed to reach the required forward voltage V_{swt} across the bridge switches.

Dc link resonates at a much higher frequency when compared to the input side voltages and current's frequency. Therefore, the equivalent circuit in Fig.2 can be used to explain the converter operation.

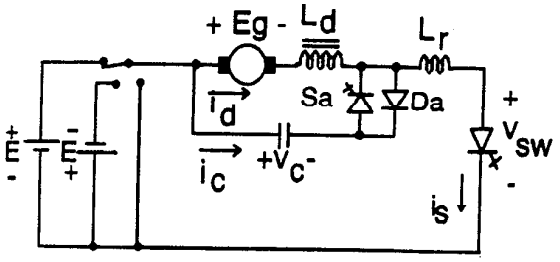


Fig.2 Monophase equivalent to the PWM-SRDCL converter

In this figure, S_w correspond to two series GTOs in the bridge and sources E, -E and 0 represent the three possible values for the rectified voltage V_d. Let's examine now the role of the bi-directional switch D_a/S_a, which introduces two resonant intervals in the circuit operation. For that, consider the case in which V_d=+E. The first resonant interval starts with the conduction of D_a. The second resonant interval starts when S_a is turned on. In reality, auxiliary switch S_a introduces an interruption in the resonant pulse. The operating intervals for the circuit in Fig.2, in this case, are presented in Fig.3.

Suppose that the current in inductor L_d is flowing through capacitor C_r and diode D_a. At the moment in which $v_c(t)=E-V_{swt}$, switch S_w is fired and first interval (I) starts (Fig.3a). Equations which characterize this first resonant interval are:

$$v_c(t) = E - V_{swt}\cos(\omega_r t) - Z_r I_d \sin(\omega_r t) \quad (1)$$

$$i_s(t) = I_d - I_d\cos(\omega_r t) + \frac{V_{swt}}{Z_r}\sin(\omega_r t) \quad (2)$$

$$i_c(t) = -I_d\cos(\omega_r t) + \frac{V_{swt}}{Z_r}\sin(\omega_r t) \quad (3)$$

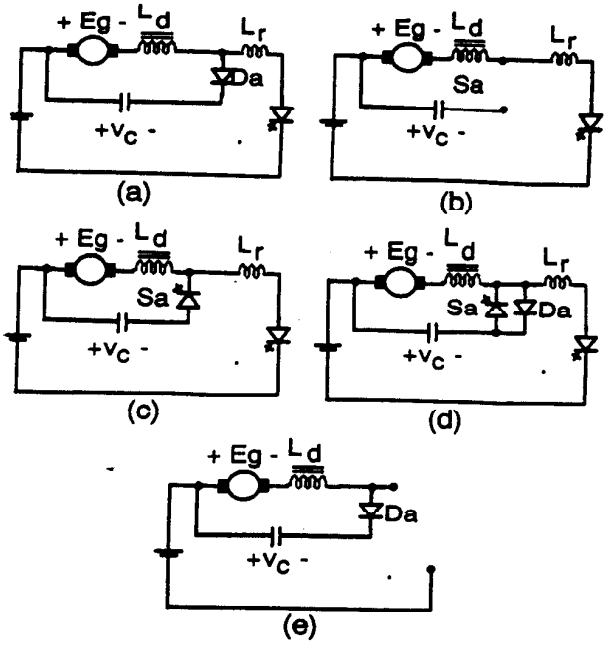


Fig.3 Sequential equivalent circuits for V_d =E

with $Z_r = \sqrt{\frac{L_r}{C_r}}$ and $\omega_r = \frac{1}{\sqrt{L_r C_r}}$

This interval end when current i_s equals I_d, at the instant $\omega t_1 = \tan^{-1}(I_d Z_r / V_{swt})$, and diode D_a turns off.

Since the diode is off, the dc current I_d flows through the equivalent switch S_w during the second interval (II) as shown in Fig.3(b). The resonant capacitor C_r voltage is maintained at a constant value of

$$V_c = E - \sqrt{V_{swt}^2 + Z_r^2 I_d^2} \quad (4)$$

This situation holds until the instant at which the auxiliary switch S_a is turned-on (Fig.3c) and the third interval (III) begins. This second resonant interval is governed by the equations

$$v_c(t) = E - (E - V_c)\cos\omega_r t \quad (5)$$

$$i_s(t) = I_d + \frac{E - V_c}{Z_r}\sin\omega_r t \quad (6)$$

$$i_c(t) = \frac{E - V_c}{Z_r}\sin\omega_r t \quad (7)$$

After reaching the resonant peak, the current i_s equals the value I_d again and the auxiliary switch S_a turns-off. This is the end of the third interval.

Interval IV starts with the auxiliary diode D_a conducting the difference I_d-i_s (Fig.3d). Equations (5) to (6) are also the governing equations for this interval. When current i_s reaches zero, switch S_w turns-off and the capacitor voltage, at the end of the interval, is equal to

$$V_{c0} = E + V_{swt} \quad (8)$$

During the interval V, the capacitor is discharged from the initial V_{c0} through D_a with the following equation:

$$v_c(t) = -\frac{I_d}{C_r}t + V_{c0} \quad (9)$$

The resonant current i_s is zero during this interval and the

current I_d is completely transferred to capacitor C_r. When $v_{sw}=V_{swt}$, which corresponds to $v_c(t)=E-V_{swt}$, switch S_w can be turned on again. The time interval of the resonant capacitor discharge from $E+V_{swt}$ to $E-V_{swt}$ corresponds to the zero current interval between two pulses and equals to

$$2t_O = 2\frac{V_{swt}C_r}{I_d} \tag{10}$$

where t_o is the interval of time in which a reverse voltage is applied to the switch S_w.

The operation period T_{op} can be defined as

$$T_{op} = T_r + 2t_O + T_{pw} \tag{11}$$

in which T_{pw} is the variable pulse width and T_r is the resonant period ($2\pi/w_r$). Therefore, operation frequency is

$$f_{op} = \frac{1}{T_{op}} \tag{12}$$

The maximal frequency operation (f_{mop}) is obtained when T_{pw} is equal to zero.

Fig.4 presents waveforms of the resonant current $i_s(t)$, the resonant capacitor current $i_c(t)$, the resonant capacitor voltage $v_c(t)$, and the switch's voltage v_{sw}, for different operation intervals of the circuit in Fig.2. During the turn-off process a negative voltage is applied across the switches with a minimum peak value equal to $V_{swt}+E_g$, where E_g is the emf of the dc motor. It is the presence of this reverse voltage that guarantees the use of SCR's, if the device speed is compatible with the resonant frequency desired.

Equations related to the cases in which the resonant circuit is short-circuited or fed by V_d=-E are presented in Ref.[5].

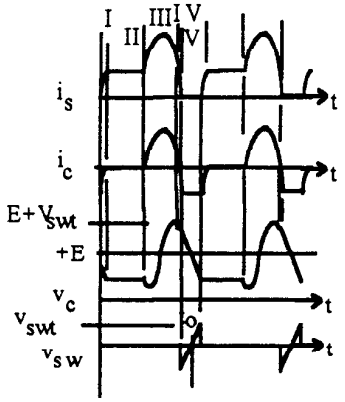


Fig.4 Principal waveforms for V_d=+E

Design Criteria

Some points are very important for design. C_r and L_r must ensure soft switching and L_d must ensure a good regulation of current i_d. A minimum value V_{swt} ensures stability in the process. Furthermore, the peak current must be less than a maximum specified value. The pwm resonant pulse can be considered as an interrupted resonant pulse and therefore the same selection criteria as in Ref. [6] can be applied for the resonant component selection. Minimization of the resonant inductor L_r losses results in the optimized value for the resonant impedance

$$Z_r = \frac{V_{swt}}{I_d} \tag{13}$$

The selection of V_{swt} can be expressed as

$$V_{swt} \geq [\frac{I_d t_o}{C_r} + \frac{2\sqrt{3}\,\pi}{f_{op}} V_{ipk}]\frac{1}{K_r} \tag{14}$$

where k_r represents a resonant pulse peak reduction due to the losses in the resonant inductor, t_o is chosen to be, at least, the reverse recovery time t_{rr} of the switching device, f_r is the resonant frequency, f_i is the input frequency and V_{ipk} is the peak value of the input voltage.

Strategy for Id Regulation and Other Considerations

Regulation of armature current I_d is necessary to guarantee zero current crossing at dc link. If large variations occur in I_d, the energy in the diverting circuit may no longer guarantee zero current crossing for a specified V_{swt}.

Fig.2 shows the input control possibilities for the monophase equivalent circuit of the PWM-SRDCL converter. One possible strategy to regulate I_d is to apply conveniently positive (V_d=E) or negative (V_d=-E) dc voltage to the link. This technique, which will here be called +E/-E/+E strategy, tends to equalize the value of current I_d to a set value I_{ref}. Besides the fact that the voltage accelerates the current drop, its application also allows the system to operate in a regenerative mode. Nevertheless, in this case, the system suffers from current and voltage stress increase, when V_d goes from -E to +E.

In Fig.5, the pulse width control is set by the criterion that the system stays in one switch configuration as long as the signal representing the error between the reference and the bias current does not change its polarity. Therefore, as long as i_d current does not reach the reference value i_{dref}, a voltage V_d=E is applied to the resonant link. Once i_d becomes greater than i_{dref} a voltage V_d=-E is applied. When i_d becomes smaller than i_{dref} again, V_d=+E is reapplied and a current pulse of different amplitude and a higher peak of capacitor voltage is obtained.

One solution to this problem is to apply zero voltage to the link before connecting the positive voltage again. Therefore, two strategies can be applied: (a) +E/-E/O/+E; and (b) +E/0/-E/0/+E. A third strategy, +E/0/+E is usually neglected because in case of a short-circuit the drop of current i_d is very slow. Nevertheless, the generated emf of a dc motor, used as load, accelerates this drop and the use of the +E/0/+E strategy becomes practical.

A complete control of the converter and dc motor, can include armature current regulator and power factor controller [6]. The error signal of the mandatory *Id* regulator can be used as a reference for regulation of the actual input currents. The bridge triggering is established with base on these error values and polarities.

If speed control is included, the error generated in the motor speed loop can go through a proportional-integral regulator and generates the current reference signal I_{dref}, to be compared with the armature current I_d.

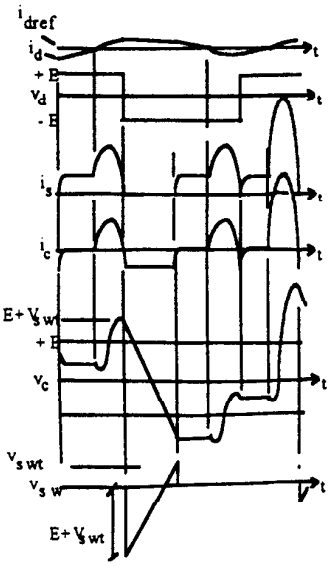


Fig.5 Principal waveforms for strategy +E/-E/+E

Choice of Switching Device

The PWM resonant dc current link converter requires unidirectional current switches with zero-current turn-off. Conventional SCR's are able to operate at high frequency, with resonant circuits [6]. Nevertheless, the switching structure composed by a GTO (being utilized in the gate assisted turn-off mode), a series and an anti-parallel diode, improves the switching characteristics, reducing significantly the turn-off losses (see Fig.11).

Loss Estimation

Reference [7] established a detailed methodology for loss calculation in a series resonant dc link converter with the improved gate assisted turn-off GTO. Three loss components may be identified for the proposed converter: device conduction loss, switching loss and passive component's loss. By considering the results presented in references [7] for the SRDCL converter as a base, only the additional losses introduced by the auxiliary devices S_a and D_a will be presented here.

Conduction Loss

Conduction losses for main switches and for auxiliary S_a and D_a may be easily obtained for all time intervals except for variable width interval, which depends on the control strategy used or external PWM synchronization. The conduction loss of the main device S_w, P_{csw}, can be calculated as the integral of the product of the resonant current and the device forward drop V_{son} in the period T_{op}:

a) losses during the pulse width interval

$$P_{csw} = V_{son} I_d T_{pw} f_{op} \quad (15)$$

b) losses during the resonant intervals

$$P_{crsw} = V_{son}[I_d T_r + \frac{4}{\omega_r}(\frac{V_{swt}}{Z_r} - I_d)] f_{op} \quad (16)$$

Conduction losses for auxiliary device S_a, and for diode D_a, may be calculated from waveforms in Fig.4:

c) D_a and T_a losses during the resonant intervals

$$P_{crdsa} = 2[A \sin \omega_r t_1 + B(1 - \cos \omega_r t_1)] f_{op} \quad (17)$$

with

$$A = (V_{don} - V_{son})\frac{I_d}{\omega_r} \text{ and } B = \frac{V_{son} V_{swt}}{\omega_r Z_r}$$

d) D_a losses during the charging interval

$$P_{ccda} = 2 V_{don} I_d t_o f_{op} \quad (18)$$

Though, total device conduction loss is

$$P_c = P_{csw} + P_{crsw} + P_{crdsa} + P_{ccda} \quad (19)$$

Switching Losses

Turn-on loss, P_{on}, can be calculated by considering a rise time t_r for the current i_a and voltage drop in the device. During the turn-off process the resonant current falls instantaneously below zero due to the reverse recovery process of the device. The turn-off loss is caused by the losses on the reverse recovery, P_r, forward reverse recovery process, P_f, and due to the device tail current, P_{tail}:

$$P_{off} = P_r + P_f + P_{tail} \quad (20)$$

These losses play a minor role in the overall losses and, for sake of space, are not presented in paper.

Passive Component's Losses

Losses caused by resistive elements of capacitors and bias inductor must be taken into account for loss calculation. Nevertheless, only those caused by the resistive component of the resonant inductor, P_{RLr}, are influenced by the pwm feature:

$$P_{RLr} = \frac{R_{Lr}}{2}[3 I_d^2 + \frac{V_{swt}^2}{Z_r^2}]\frac{T_{pw}}{T_{op}} \quad (21)$$

The losses due to the snubber elements are very small and will not be considered in this paper.

Modified PWM-SRDCL

One advantage of the PWM-SRDCL converter over the conventional series resonant dc link converter is its possibility to synchronize with external PWM signals and its ability to reduce the steady state error for the regulated current I_d. In the converter of Fig.1, the command for interruption of the link current is accomplished by turn-on of auxiliary switch T_a. Nevertheless, no other action can be determined by the control system until the produced resonant pulse reaches zero. Therefore, the resonance originates a delay in control action.

One alternative solution for this problem is the introduction of a predictive control in the system thus increasing the complexity of control. A better solution is obtained with the circuit in Fig.6. As compared to the circuit in Fig.1, the only difference is the opposite connection of the bi-directional switch (S_a/D_a). As a result, intervals II and III, of operation, as well as Fig.3(b) and Fig.3(c), are interchanged. Principal waveforms for the modified converter are shown in Fig.7. Equations that

characterize the intervals are easy to to be calculated. Also, design criteria and control strategy can be the same as for the converter in Fig.1.

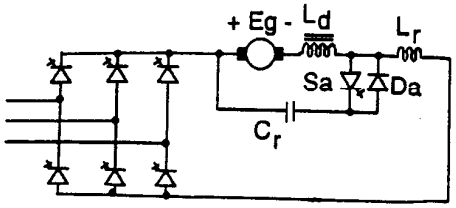


Fig.6 Modified PWM-SRDCL converter

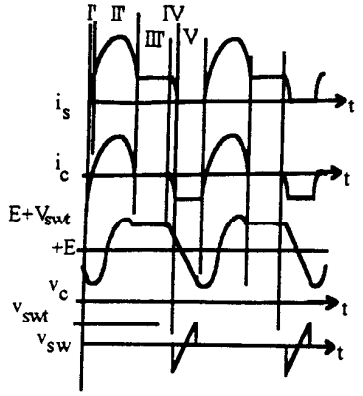


Fig.7 Principal waveforms for circuit in Fig.6

Simulation and Experimental Results

Simulation results for dc link current (i_s), motor current, (i_d), input current (without input filter, i_{sain}), input voltage (v_{sin}), motor voltage (v_m), and dc link voltage (V_d) is presented in Fig.8 and Fig.9 for strategies +E/-E/+E and +E/0/+E, respectively. In both cases, dc link and armature current are continuous at start and regulation process only initiates when current i_d reaches I_{dref}. Fig.10 shows that the ripple obtained in the regulated armature current id, for the circuit in Fig.1, is smaller with the use of the +E/0/+E strategy than that obtained with the use of the +E/-E/+E strategy. The steady state error for current id is less oscillatory when the modified circuit of Fig. 6 is used (Fig.11). The schematic of the three phase experimental converter assembled in laboratory is presented in Fig.12, where L_s includes dc bias inductance L_d and armature inductance.

An existing 20 kHz 5 kW series resonant converter was converted to the link structure of Fig.12. An input ac voltage of 115 Vac was used to feed the resonant converter converter, built with gate assisted turn-off GTOs (IR 81RDT). Series (IR R18CGF10A) and anti-parallel (IR 40HFL100S05) diodes were incorporated to the basic device with the aim of avoiding the reverse and forward recovery process. This way, turn-off losses are significantly reduced. Current sensors to measure I_d amplitude and is zero crossings, voltage sensors for measuring the voltage across the switches, and a GTO drive circuit was used to implement control. A delta modulator was used with the objective to regulate the bias

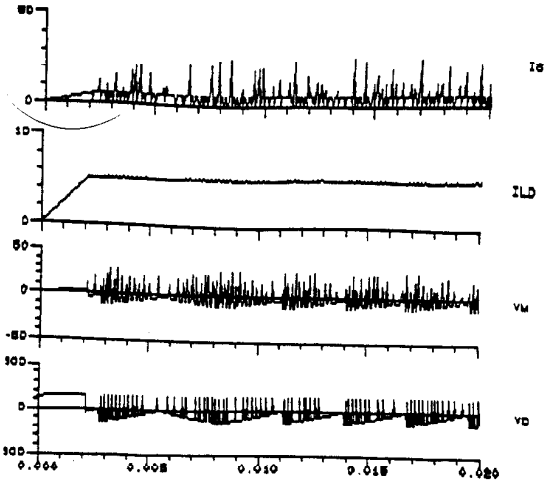


Fig.8 Simulation results of currents (A) and voltages in Fig.1 for +E/-E/+E strategy

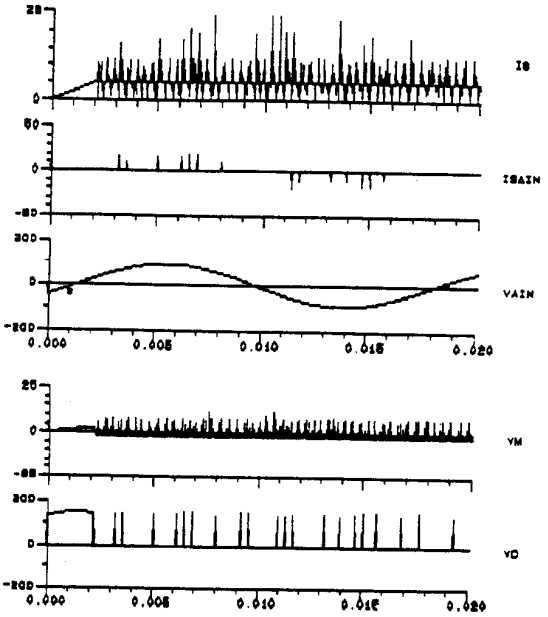


Fig.9 Simulation results of currents (A) and voltages(V) in Fig.1 for +E/0/+E strategy

current I_d. The complete control algorithm was implemented in a DSP Motorola 56000 system. Resonant capacitor, resonant inductor and bias inductor were, respectively: L_r=60 μH, C_r=0.3 μF and L_d=45 mH. The filter capacitance used were C_f=10 μF.

The results of Fig.12 show the current in L_r (i_s), the voltage across C_r and the ripple of the armature current I_d for a strategy +E/0/+E. In this case it can be noted that the resonant current remains in a particular state until the error in I_d exceeded a given threhold or until the maximum width of 400 μs is reached. Compared with the standard resonant converter, the use of the PWM-SRDCL converter results in a lower operation switching.

Simulation showed that even with the addition of two

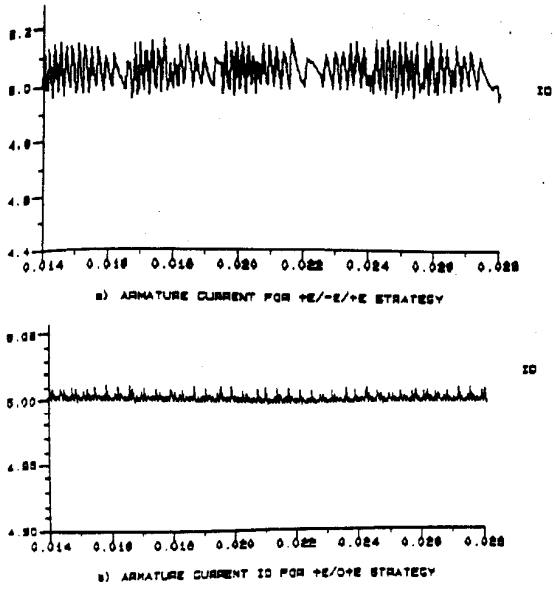


Fig.10 Armature current Id for +E/-E/+E (upper trace) and +E/0/+E (lower trace) strategies in the circuit of Fig.1

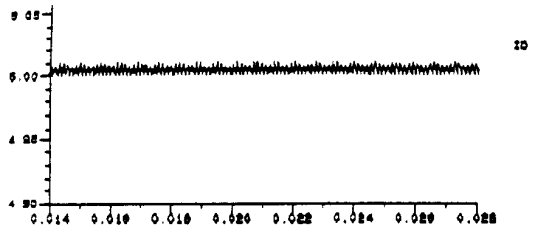
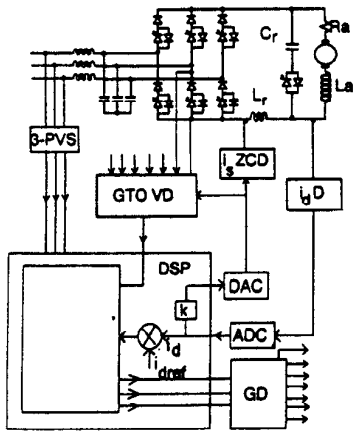


Fig.11 Armature current Id for +E/0/+E strategy in the circuit of Fig.6



3-PVS: 3-phase voltage selector
GTO VD: GTO voltage detector
i_sZCS: current i_s zero crossing detector
i_dD: $i_d$detector
DAC: digital/analog converter
ADC: analog/digital converter
GT: gate driver

Fig.12 Control of the PW-SRDCL converter

devices to the standard converter, efficiency of the overall three-phase system stays around 95%.

Motor parameters used for simulation were: 40 HP,

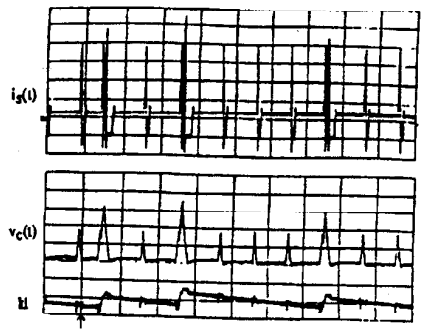


Fig.12 Experimental results: (a) Resonant current i_s (top), 5 A/div; (b) Capacitor voltage v_c (middle), 100 V/div; (c) Ripple of the dc current I_d (bottom), 0.2A/div (0.5 ms/div)

L_a=4.3 mH, R_a=0.57 Ω, J=0.0881 kgm/rad/sec^2, B=0.02 kgr/rad/sec, T_{rated}=40.65 Nm, w_{rated}=1750 rpm.

Conclusions

This paper examines the use of a PWM-series resonant dc link converter as a dc motor drive. Compared with the standard SRDCL converter, the PWM-SRDCL converter had a smaller number of switchings in one cycle. An improvement is suggested to eliminate a delay in the response of the system due to the resonance period. Simulation and experimental results verify theoretical studies.

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