Research Report
94-10

Current Clamped, PWM, Quasi-Resonant DC Link Series Resonant Converter

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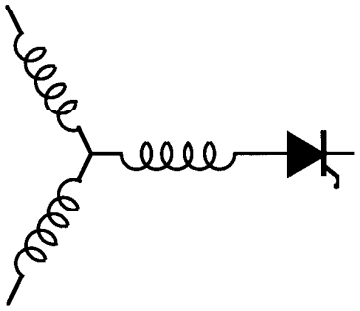

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Abstract **This paper presents a new High Frequency Series Resonant DC Link Topology derived from [1], wherein the resonant tank does not bring about peaky currents in any portion of the system. The characteristic overall-clamping mechanism permits lower-current-rating for the semiconductor devices, resonant capacitor and filter capacitors, easing the cost burden. Moreover, the values of the resonant inductor and the capacitor can be reduced substantially, limited only by the di/dt ratings of the devices, since the resonant current peaks, which would otherwise have risen to a higher value (tank storage energy burden) no longer appear in this configuration. In the paper, converter is digitally simulated using "ACSL" and output performance is investigated. The voltage stresses across the auxiliary switches are estimated using the "SABER" simulator on a mono-phase model. PWM-capable other series resonant topologies are compared with the new topology for voltage stresses across the auxiliary switches. using the SABER simulation code.**

I. INTRODUCTION

High switching frequencies allow a power converter to synthesize high fidelity waveforms while offering a higher power density. Soft switching schemes are therefore of utmost importance in exploiting the thermal limitations of the semiconductor devices. Unfortunately, many of the soft-switching schemes in the literature have topology dependent limitations, such that well-known PWM techniques cannot be implemented. Therefore such schemes call for an increased switching frequency, in order to keep sub-harmonic frequency components from appearing at the output. Other adverse properties of the soft switching schemes are higher resonating current peaks or voltage peaks due to the oscillations caused by the stored-tank energy. Parallel-resonant converters and series-resonant converters share the same problems in a dual nature, regardless of the two linking modes available (dc or ac link). The original Series Resonant DC Current Link Converter scheme [1] is indicated in Fig. 1. This topology has subsequently been improved by using a saturable core-clamping [2] to limit resonant peaks thereby to reduce the cost of devices. However, those topologies lack pulse controllability. The topologies introduced later [3-5], provide better pulse controllability at the expense of additional number of devices over the basic topology and the auxiliary /main or both devices are subject to higher current peaks. Therefore, current commutated thyristor devices which can tolerate repeated higher current peaks have been the natural solution for the device type. However, the inverse relation of the blocking voltage and the circuit commutated turn-off time (t_q) and also allowable peak currents proscribe a limit for the output voltage and the fidelity of the output waveform. The topology introduced in this paper is unique in its operation that it has PWM capability and also all currents are clamped at 1 pu whereby MCT or a cost effective IGBT-DIODE combination could be used to replace thyristor devices. Therefore with this topology switching frequency can be further increased leading to a compact design.

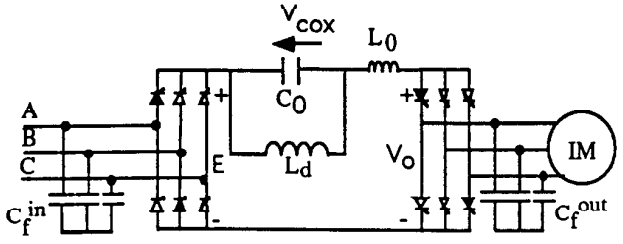

Fig.1 Basic SRDCL topology

II. PRINCIPLE OF OPERATION

Fig. 2, illustrates the new power circuit topology. In the circuit, inductor L_d is comparably large and acts as the current source. Components C_0 and L_0 form the resonant tank. Auxiliary thyristors S_2, S_3 and S_4 act as the pulse shaping elements and also modulate the width of the link current. The output bridge operates to synthesize the given 3-phase reference voltages and the input bridge controls the DC biasing current I_d at a constant reference. It is assumed here that the input and output bridge thyristors are initially off, therefore the existing biasing current I_d of the inductor L_d is carried by the switches S_3 and S_4. The bridge switches are

forward biased as the capacitor C_0 continues to charge in the direction shown in Fig. 2 through the switches S_3 and S_4.

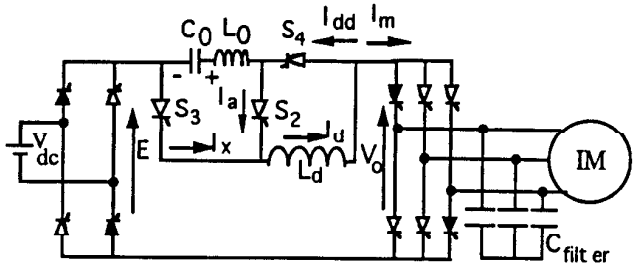

Fig.2 New Current-Clamped SRDCL Topology

Upon reaching a stipulated voltage across the selected 4-thyristor set (or IGBT-DIODE) shown in black in Fig. 2, firing signals are applied. As the input and output voltage variations during a few resonant cycles can be ignored safely, the mono-phase equivalent circuit shown in Fig. 3 can be used to describe the operation of the converter from this point forward in time.

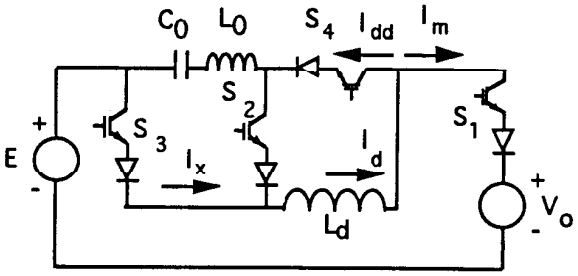

Fig.3 Mono-phase equivalent circuit of the converter

Note that in Fig. 3 all the switches are, for the sake of convenience, drawn as an IGBT-DIODE combination, and in which S_1 represents the lumped four switches of the input and output bridges. However, it is clear that since the currents are brought to zero in each switching device, thyristors are equally capable of operating in this circuit. Typical current

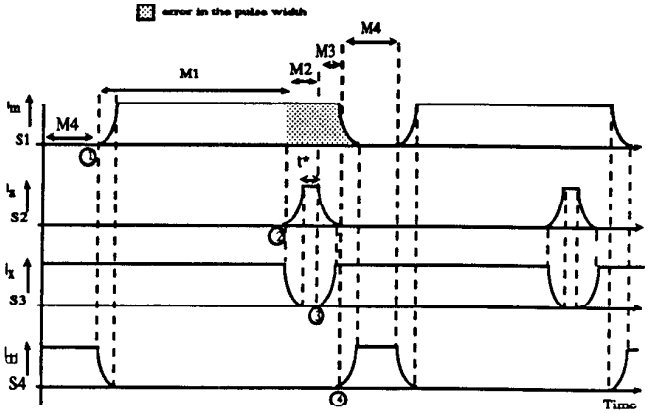

Fig. 4(a) Typical switching waveforms

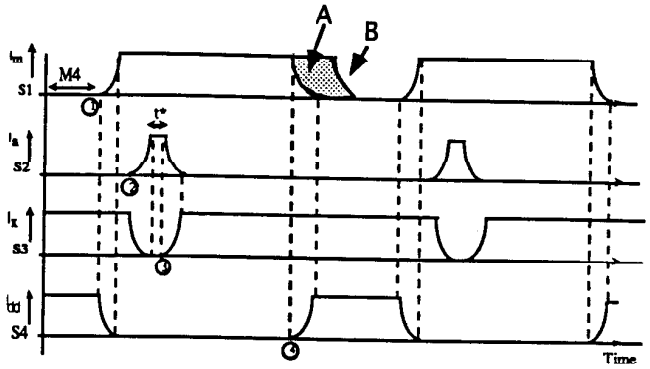

Fig. 4(b) Switching pattern with advanced S2 firing.

waveforms in the switches and four operating modes are shown in Fig. 4. The starting point of each mode is shown by encircled numbers, attached to the plot of the relevant switch. It should be noted here that all currents are well clamped at the link level and also all are occur in a soft manner due to the resonant-tank-excited mode transfer. The shaded area in the Fig. 4(a), top-trace, reveals the amount of error that can take place if the S_2 is activated when the required pulse width has been reached. This result is ideally due to the delay of the current transfer as well as the requirement of the resonant capacitor charge reversal. In order to eliminate the above error, switch S_2 can be strategically turned on in advance as shown in the Fig. 4(b) to set the required voltage of the capacitor C_0. Once the set voltage has reached current in S_2 can be transferred back to S_3 to continue the cycle. The locus shown by "A" represents the error free pulse width whereas "B" represents the erroneous locus.

Mode 1:

From Fig. 5(a) the equation for mode 1 can be written as,

$$I_m + I_{dd} = I_d \qquad (1)$$

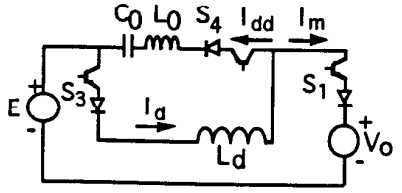

Fig. 5 (a) Mode-1, current transfer

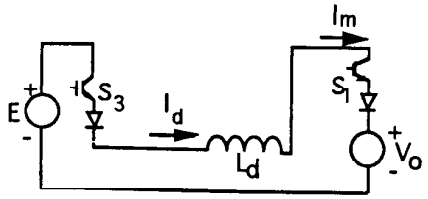

Fig. 5 (b) Mode-1, power transfer

Assume that the voltage across the switch S_1 is V_{thm} then since E and V_o are voltage sources, having fired S_1 on, the voltage held off by S_4 should be taken over by the inductor L_0 to satisfy the voltage equation of the loop. Thereby, the resonant tank is heavily excited and the current I_{dd} starts decreasing with an initial decay-rating given by V_{thm}/L_0, which forces I_m to increase in a resonant way, towards I_d to satisfy Eq.(1). At the end of the transfer, I_{dd} reaches zero, whereupon S_4 turns off and the clamped link current (I_m) continues to flow through the load as shown in Fig. 5(b) in which most of the power is transferred.

Mode 2:

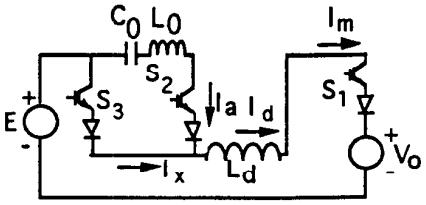

Fig. 6(a) Mode- 2, current transfer

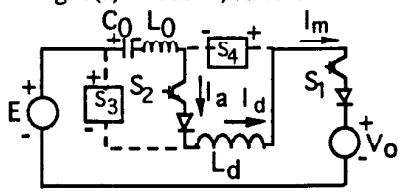

Fig. 6(b) Mode- 2, charge reversal

When the pulse width commanded by the controller has been reached, switch S_2 is fired, whereby current in the switch S_3 is transferred to S_2 in a resonant manner and the capacitor C_0 is charged in the direction shown at a constant rate. Mode 2 is used to reverse charge the resonant capacitor to provide adequate forward biasing for S_3 and S_4 to be activated in the Modes 3 and 4 respectively. Time t* shown in the Fig. 4 signifies the charging of the capacitor C_0 to achieve the desired voltage across S_3 and S_4.

Mode 3:

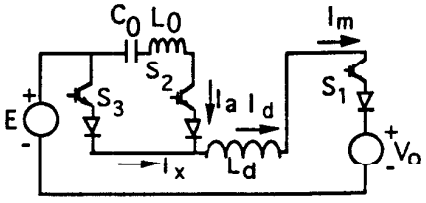

Fig. 7 Mode-3, current transfer

In this mode, S_3 is turned-on and therefore, S_2 turns-off by transferring the bias current I_d to S_3 in a soft manner as shown in the Fig. 7. Soon after the transfer has completed, Mode 4 could be started. Care must be taken here, however, not to fire S_4 until the complete current transfer from S_4 to S_3 has occurred. This delay is to ward off the possibility of I_d trapping, that may take place in the loop through the switches S_2 and S_4, whereby the circuit operation would be inhibited as shown in the Fig. 8.

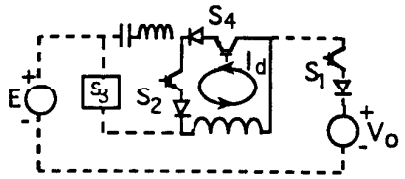

Fig. 8, Showing current trapping

Mode 4:

Mode 3, has adequately set the forward voltages for the switches S_3. and S_4. Therefore when S_4 is turned-on resonant tank is re-excited and the current I_m starts reducing to make the way for the increasing resonating current in the switch S_4. At the end of the current transfer S_1 turns off and the resonant capacitor continues to charge as shown in the Fig. 9 in preparation for the next switching cycle.

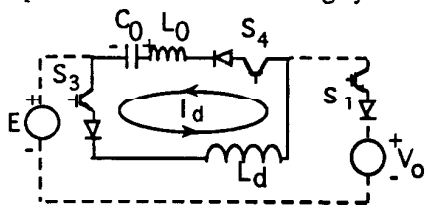

Fig. 9 Mode-4

Converter Control:

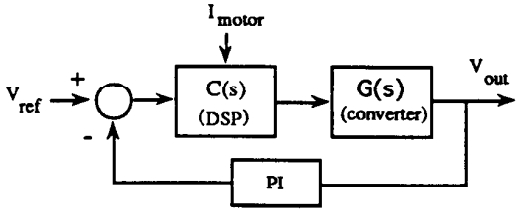

Fig. 10 Control diagram

An output controller synthesizes the output voltage references by properly distributing the pulses among phases. Simple open-loop PWM controller introduced for hard switching in [7] which has been also well tested for soft switching in [4], can be easily adopted. However, in this paper the close loop control scheme used in [5] is examined with an average switching frequency of 40 kHz. As shown in the control diagram of Fig. 10, voltage errors at the output and existing motor currents are used to calculate the charge requirement of each and every phase during the next pulse to eliminate errors in phase voltages. Then the controller generates the information for thyristor selection and also the command reference for the pulse width. Detailed derivation of equations and method of output thyristor selection are the

same as that was used in the literature [5] and therefore would not be repeated here. Following three equations represent the charge required by each phase and subscripts x, y and z signifies the three phases. DV is the voltage change demanded by phases from the next pulse, to correct errors of the output voltage and C_f is the filter capacitor. DT is the average pulse period (should DT be constant, the link current is to be circulated by turning on the two thyristors on one leg)

$$DQ_x = \frac{C_f}{3}(DV_{xy} + DV_{xz}) + I_x DT \quad (2)$$

$$DQ_y = \frac{C_f}{3}(DV_{yx} + DV_{yz}) + I_y DT \quad (3)$$

$$DQ_z = \frac{C_f}{3}(DV_{zx} + DV_{zy}) + I_z DT \quad (4)$$

Assume that phases x and y have obtained the maximum and minimum charge demand after the n-1th pulse, and also DQ_X is the absolute maximum. Then the charge reference for the PWM controller for the nth pulse would be DQ_X. The triggering time of the switch S_2, t_{on}, is determined by the following relation.

$$\int_0^{t_{on}} I_m \, dt = DQ_{ref} \quad (5)$$

Therefore, neglecting the period of I_m build-up, t_{on} could be written as,

$$t_{on} = \frac{DQ_x}{I_d} \quad (6)$$

Input Converter Control:

The input side H-bridge shown in the Fig. 2 must be controlled to keep the biasing current(link current) at a given reference value. Since the reference can be changed in steps a simple PI controller would yield better results here. When the bias current is smaller than the current reference, input bridge is set positive to supply energy from the source to the system and on the contrary, if the bias current is greater than its reference energy could be supplied to the system to compensate the excess current. However it can be seen that this negative voltage at the input would impress an additional voltage penalty on the auxiliary switches S_2, S_3 and S_4. Therefore, instead of the negative pulse being applied, the input can be set to have a zero voltage. Fig. 12 represents the saber simulated voltage plots of the equivalent and auxiliary switches respectively. It can be noted from the plots that the worst case voltage across auxiliary switches are typically 3 pu. It should be noted that the top-trace represents the voltage stress across the auxiliary thyristor. Voltage stresses across individual thyristors can be derived as described in the following section.

Shown in Fig. 11 are the results of digital computer simulation in ACSL . It can be observed that a biasing inductor of the order 1 mH and filter capacitors of the order 20 μF would be adequate at a switching frequency of 40 kHz. The parameters used in the simulation are as follows.

Circuit Parameters :

Biasing Inductor (L_d)	1 mH
Resonant Inductor (L_0)	0.5 μH
Resonant Capacitor (C_0)	0.6 μF
Filter Capacitors (C_f)	20 μF

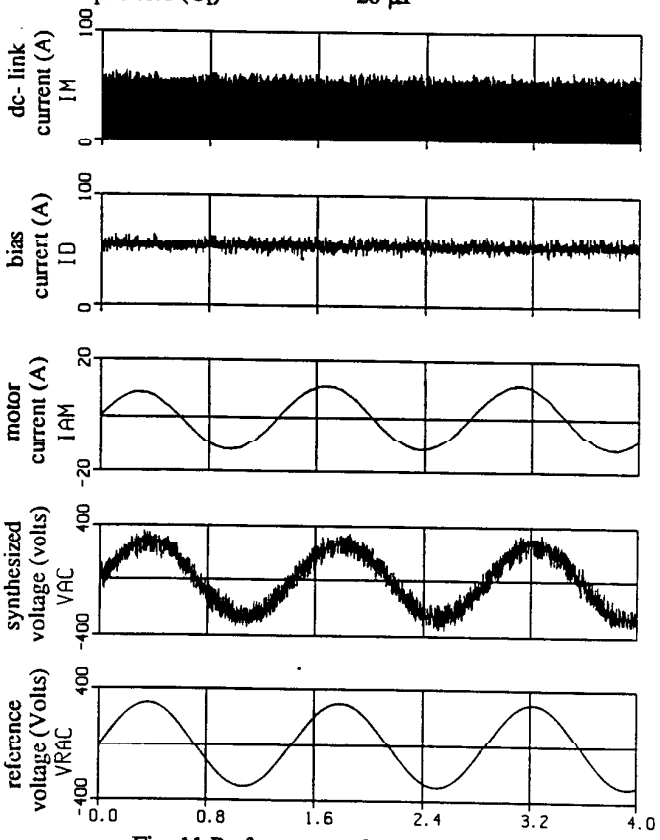

Fig. 11 Performance of the inverter ACSL simulation results

III. VOLTAGE STRESS COMPARISON

By reference to Fig. 1, the voltage of the resonant capacitor just before a current pulse can be written as,

$$V_{cox} = E - V_{thm} - V_o \quad (7)$$

V_{thm} is the selected threshold voltage of the equivalent switch just before the firing. Noting the fact that the resonant capacitor is charged to $2V_{thm}$ during a resonant cycle, the voltage

of the resonant capacitor just at the end of a current pulse can be written as,

$$V_{cox}' = E+V_{thm}-V_o \quad (8)$$

and now the above equation can be generalized as,

$$(V_{cox})_{n-1}' = (E-V_o)_{n-1}+V_{thm}$$

where, the subscripts signify the fact that it represents the capacitor voltage at the end of the $(n-1)^{th}$ pulse. If the voltage across any possible equivalent thyristor is V_{sw}, then the voltage across any equivalent thyristor at the end of $(n-1)^{th}$ pulse could be written in general as,

$$V_{sw} = (E-V_o)_n - (V_{cox})'_{n-1} \quad (9)$$

$(E-V_O)_n$ represents the new combination of the input and output voltages. Note that should it be the same V_{sw} becomes $-V_{thm}$. Substituting, for V_{COX},

$$V_{sw} = (E-V_o)_n - (E-V_o)_{n-1} - V_{thm} \quad (10)$$

Therefore, the maximum probable forward voltage (as shown in the direction in Fig. 1) across a new equivalent thyristor just at the end of one current pulse is derived to be,

$$V_{sw} = 4 - \frac{V_{thm}}{V_o} \text{ pu} \quad (11)$$

Thus, if the threshold V_{thm} is selected to be $2V_O$ we can optimize the probable forward voltage across any equivalent thyristor set to be 2pu and there by regular pulse height could also be obtained. It should be noted here that the optimal parameters are topology dependent but the same approach described here has been adapted in the comparison scheme. For the modified clamped version, an analysis is set forth in the literature [5].

It is now appropriate to establish individual voltages across the bridge devices. Assuming the input and output bridge devices are identical and therefore offer identical leakage impedances and also steady state three phase conditions do exit and, the voltage across the upper thyristor on the arm of phase A can be written as,

$$V = \frac{V_{dc}}{2} - \frac{2}{3}V_{ab} - \frac{1}{3}V_{bc} \quad (12)$$

and can be reduced to,

$$V = \frac{V_{dc}}{2} - V_a \quad (13)$$

where, V_{dc} represents the voltage across the output bus which can be substituted in terms of the worst resonant capacitor voltage (4 pu as can be found from Eqs.(8) -(11)). When all the thyristors are off V_{dc} can be assumed to carry half the resonant capacitor voltage under the assumption that the input and the output bridge-leakages are identical. By doing so and normalizing the voltages, the worst case condition can be written as,

$$V = \frac{2V_o}{2} + \frac{|V_o|}{\sqrt{3}} \quad (14)$$

where, V_o is the maximum output voltage and taken as the base for the voltage and then by normalizing,

$$V = 1.58 \text{ pu} \quad (15)$$

This result was verified using the SABER simulator to determine the voltages on the output bridge. It should be noted from the above analysis that the bridge thyristors are subject to different worst case voltages due to the topology depended difference in worst case V_{dc}. SABER simulations have also been carried out using the mono-phase equivalent circuits of the different four converter topologies that have been listed under the references and the results can be found in the Table 1.

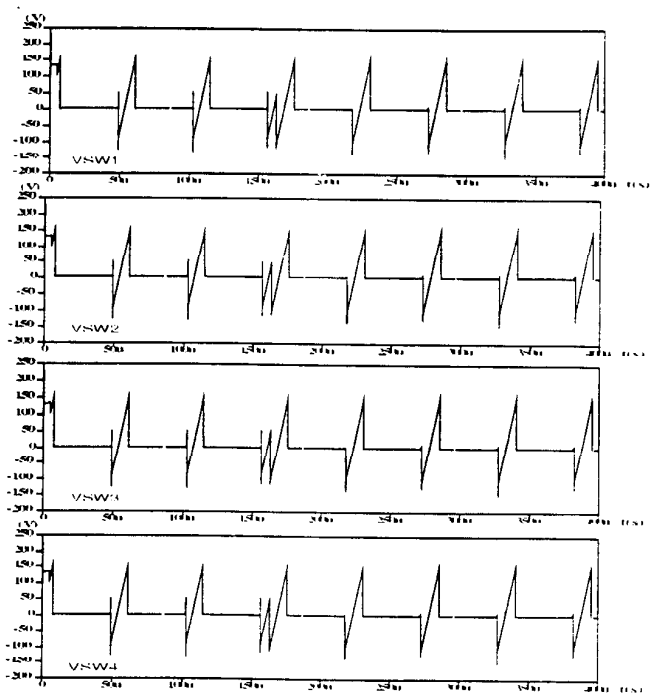

Fig. 12 SABER simulated voltages across the switches of the new topology (see Fig.3 ; VSW1,2,3,4 = voltages of S_1,S_2, S_3 and S_4); 50V= 1 pu

	Peak Voltage(pu)		Peak Current(pu)	
Topology in Ref. #	Main	Aux	Main	Aux
1	1.58		*	-
3	1.58	~2.5	*	*
5	1.82	~2.1	1 **	*
New	1.82	3	1	1

* Resonant current peak

** Output side switches only. Input side switches have resonant current peak

Table 1: Voltage and curent stress comparisons

Typical current waveforms obtained from the SABER simulations for all topologies that have been compared in the paper are shown in the Fig. 13 and 14 of the appendix.

IV. CONCLUSION

The new topology introduced in this paper allows all switches to perform resonant transition switching while all currents being well clamped at the biasing level (I_d), which, in turn, enables replacing thyristors by lower current rated IGBT's, whereby higher converter switching ratings could be adopted. Therefore, the size of filter elements and biasing inductor can be made much smaller easing the cost and space constraints. Noting the fact that peak currents are absent, resonant elements may be selected smaller only limited by the di/dt rating of the devices. The PWM capability of the system enables to achieve better spectral content at the output current wave. Lower EMI generation (low dv/dt), efficient switching characteristics due to soft switching and lower device cost (due to lower current rating) are also highlights of this new circuit. However, since five power switches are in series during maximum power transfer period of any given cycle, higher conduction loss appears to be the major disadvantage of this topology. Higher voltage stresses, however, across the switches S_2 ,S_3 and S_4 limit the converter output voltage.

The above topology could find applications in moderate-voltage, high-frequency, high-current applications where a low EMI environment is essential. High di/dt capable, low on state voltage, fast MCT device could also be used to exploit the 1 pu low current nature of the topology.

V. ACKNOWLEDGMENTS

The authors are grateful to the Electric Power Research Institute (EPRI) for funding of this research.

REFERENCES

[1] Y. Murai, T.A. Lipo "Current Pulse Control of High Frequency Series Resonant DC-Link Power Converter", IEEE IAS Annual Meeting,, 1988, pp. 772-779.

[2 Y. Murai, S. G. Abeyratne, T. A. Lipo, P. Caldeira, "Current Peak Limiting for a Series Resonant DC-Link Power Conversion Using a Saturable Core", EPE Proceedings, 1991, pp. 2-008 - 2-012.

[3] E. DaSilva, G. Ledwich, M. Aydemir, T. A. Lipo, "Pulse Width Modulated Series Resonant Converter", IAS Annual Meeting,, 1992, pp. 744-749.

[4] H. Nakamura, Y. Murai, T. A. Lipo ,"Quasi Current Resonant DC Link AC/AC Converter", IAS Annual Meeting,, 1993, pp. 279-284

[5] S.G. Abeyratne, T. A. Lipo, Y. Murai, J. Horikawa, "Current Clamped, Modified Series Resonant DC-Link Power Converter for a General Purpose Induction Motor Drive " IEEE APEC 1994 Proceedings, vol.1, pp. 267-274

[6] M.T. Aydemir, P. Caldeira, T.A. Lipo, Y.Murai, E. DaSilva, G. Ledwich, "Utilization of a Seriees Resonant DC-Link for a DC Motor Drive", IEEE IAS Transactions Sep-Oct 1993, Vol. 29, No.5, pp 949-958.

[7] Mitsuyuki Hombu, Shigeta Ueda, Akiteru Ueda, "A Current Source GTO Inverter with Sinusoidal Inputs and Outputs ", IEEE-IAS Trans. Ind. Application, vol. IA-23, No. 2, pp. 247-255, March/Apr 1987.

V. APPENDIX

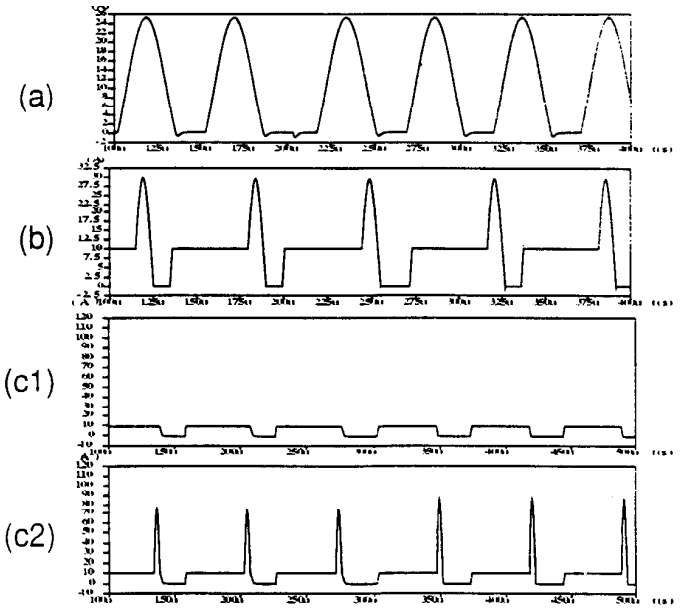

Fig.13 Typical current waveforms for topologies of Ref. [1], [3] and [5]. (obtained from SABER simulations)

(a) [1] ; input and output currents (same)

(b) [3] ; input and output currents (same)

(c1) [5] ; output current

(c2) [5] ; input current

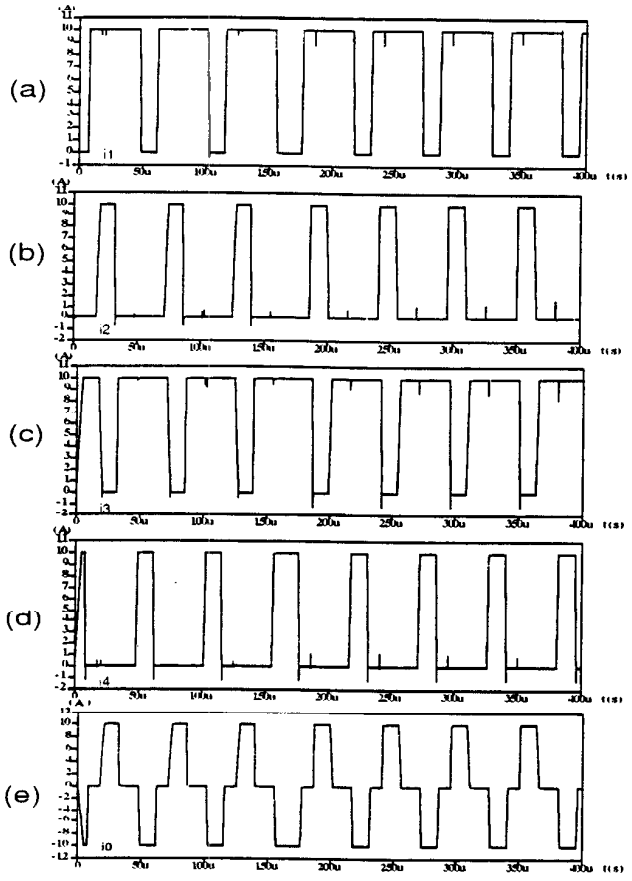

Fig. 14: Typical current waveforms of the new topology (obtained from SABER simulation) see Fig.3;

(a) Current in S_1

(b) Current in S_2

(c) Current in S_3

(d) Current in S_4

(e) Inductor Current