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Comparison of Multilevel Inverters for Static Var Compensation

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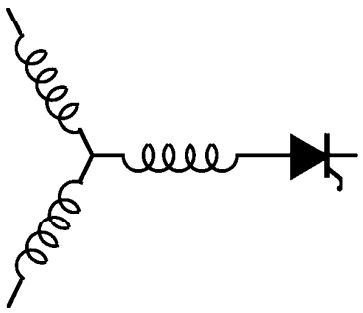

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Abstract— Inverter–based Static VAR Compensators (STATCONs) can benefit from the use of a Multilevel structure which allows the elimination of the step up transformer. The inherent high quality of the multistep waveform allows operation without PWM, thus high switching losses are avoided. This paper discusses the issues affecting the application of multilevel structures as reactive power compensators and compares the device MVA and reactive component MVA requirements of two topologies that have been presented in prior literature. The modulation strategy strongly affects the voltage balancing in the DC bus capacitors as well as their ripple current rating and capacitance value.

I. INTRODUCTION

There is considerable interest in applying voltage source inverters in the utility system as controlled sources of reactive power. In steady state operation an inverter–based static var compensator (STATCON) produces controlled reactive current similar to other static var compensators such as thyristor controlled reactors (TCRs) and thyristor switched capacitors (TSCs). However, applying a voltage source inverter for reactive power compensation can reduce the physical size of the compensator and improve its performance during power system contingencies. A STATCON can provide transient current beyond its ratings even when the system voltage is depressed. In this paper the benefits of using a high voltage multilevel inverter in a STATCON application are examined.

The use of a high voltage inverter makes possible direct connection to the 13 kV distribution system, eliminating the distribution transformer and reducing system cost. In addition, if the harmonic content of the inverter waveform can be reduced without filtering or pulse width modulation, the efficiency of the system will be improved.

Multilevel inverters present a new set of features which are well suited to use in inverter based reactive power compensation. It may be easier to produce a high power, high voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. The power rating can be increased by increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly.

II. LIMITATIONS OF THE SIX PULSE INVERTER

In a typical distribution level STATCON, a voltage source inverter is connected to the power system via a step–up transformer. The transformer boosts the inverter voltage to match that of the distribution system. The leakage reactance of the transformer provides some filtering of the harmonics of the inverter voltage. Inverter harmonics are further reduced by pulse width modulation of the inverter's voltage or by adding harmonic filters with a corresponding penalties in system efficiency and cost.

A number of problems are associated with utilizing the standard two-level, six pulse inverter in utility applications. First, it is difficult to extend the power capability of the structure beyond the ratings of an individual switching device. The six step inverter must use series connected devices to boost the DC bus voltage beyond the voltage rating of an individual force commutated device. The number of devices which can be placed in series is limited by the need for dynamic and static voltage sharing. To ensure dynamic voltage sharing, large snubber components are used and the turn–off time of each device must be carefully controlled so that all devices see the same voltage stress. Turn-on and turn-off coordination of long strings of GTOs becomes difficult, if not impossible. The number of devices that can be successfully connected in series in this fashion is limited and device voltage utilization is generally poor. The snubber losses can become significant.

Second, the harmonic performance of the inverter is poor unless pulse dropping or pulse width modulation is used. In utility applications, the gate turnoff thyristor is the only force commutated power device available and its switch losses are comparatively high. The switching energy losses

associated with PWM are unacceptable as the total compensator system loss should be less than 1.0%. This efficiency number is typical for most utility applications of power electronics.

To get around the limitations of the inverter, six pulse inverters have been connected together in ways which reduce their harmonic content and combine their output power. Transformer coupled six step inverters have been used to create pseudo twenty-four pulse (or higher) arrangements. This arrangement improves the harmonic performance of the waveforms and increases the total system power. Prior work by Mori [5] has demonstrated a STATCON compensator which used eight six pulse inverters connected by a large phase shifting transformer.

III. ADVANTAGES OF MULTILEVEL INVERTERS

Use of a multilevel inverter structure can eliminate the need for the step up transformer and reduce the harmonics produced by the inverter. Initially, the multilevel inverter structure was introduced as a means of reducing the output waveform harmonic content. It was also realized by Nabae [1] that in a multilevel structure the DC bus voltage could be increased beyond the voltage rating of an individual power device by the use of a voltage clamping network consisting of diodes. The harmonic reduction advantages of a multilevel structure with more than three levels was addressed by Bhagwat et al [2]. The extension of the system KVA rating beyond the limits of an individual device was further examined by Carpita et al [3] where the concept of using diodes to limit device voltage stress was extended to an unlimited number of levels. Meynard et al [4] proposed a multilevel structure where the device off state voltage clamping was achieved by using clamping capacitors rather than clamping diodes. The intriguing feature of these multilevel inverter structures is their ability to be scaled up in power and simultaneously have their harmonic performance greatly improve without having to resort to PWM.

The multilevel inverter topology attempts to address some of the limitations of the standard two level inverter. The key properties of a multilevel structure are:

1. Voltage and power output increase with number of levels
2. Harmonics decrease as the number of levels increases
3. Increasing output voltage and power does not require an increase in rating of individual force commutated devices.
4. Dynamic and static voltage sharing among main devices is built into structure.

As additional voltage levels are added, the voltage waveform has more free switching angles which can be chosen for harmonic elimination. PWM losses can be avoided and filtering requirements are reduced. Adding a voltage level involves adding GTOs to each phase but it does not require an increase in the voltage rating of an individual GTO. Dynamic voltage sharing across GTOs is built into the structure either through clamping diodes or clamping capacitors. These points will be examined further in the following sections.

For a STATCON that is intended for use in a distribution system, a 9–level inverter will have an output voltage that is sufficiently large so that the inverter may be connected directly to the 13 kV AC system. The expensive high voltage step-up transformer can be eliminated and replaced by a set of much smaller inductors. A 9–level inverter has four free switching angles which can be chosen to eliminate the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics of its voltage. The fundamental output voltage of the inverter is set by the DC bus voltage which can be controlled by charging or discharging the main DC bus capacitor. The phase shift between the inverter's voltage and the system voltage is used to control the real power flow into the inverter which then charges or discharges the DC bus capacitor.

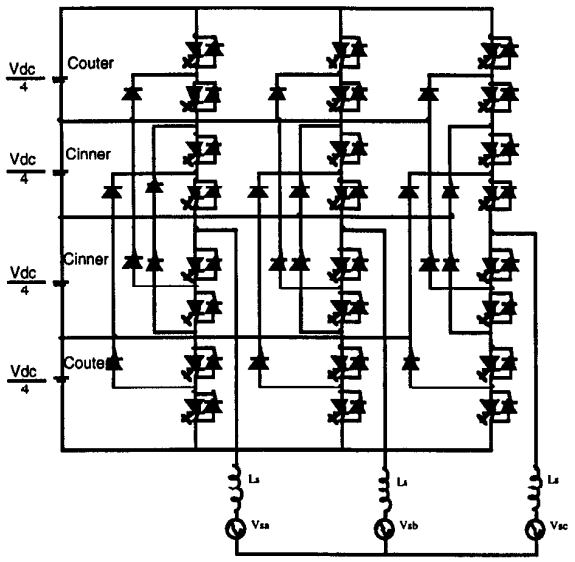
IV. TOPOLOGY DIFFERENCES OF MULTILEVEL INVERTERS

The two multilevel inverter topologies which have previously been described in the literature will be compared. The first is referred to by us as the Diode Clamped Multilevel Inverter DCMLI, the second is referred to as the Flying Capacitor Multilevel Inverter (FCMLI). For the same number of voltage levels, they produce the same high quality multilevel waveform, however the voltage synthesis method, device MVA requirements and capacitor MVA requirements are quite different. To illustrate these points, five–level versions of each inverter will be compared.

A. Description of the inverters

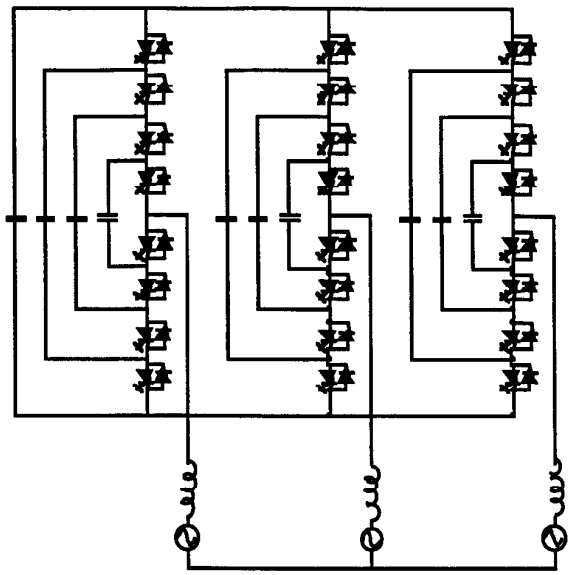
The DCMLI uses a series string of capacitors to divide up the DC bus voltage into a set of voltage levels. Each phase leg consists of a number of force commutated devices in series which are connected via diodes to the tap points along the DC bus capacitor. The forward voltage across each main device is clamped by the connection of diodes between the main devices and tap points along the string of DC bus capacitors. The tap points provide clamping voltage levels.

The FCMLI uses a ladder structure of DC side capacitors where the voltage on each capacitor differs from that of the next capacitor. The size of the voltage increment between two capacitors defines the size of the voltage steps in the output waveform. Separate capacitors are used for each phase leg of the inverter.



- Device voltage stress scale with the number of voltage levels
- Capacitors can be precharged as a group
- Capacitors see current ripple>=3rd harmonic
- Clamping diodes see high voltage stress
- All three phases use the same capacitor bank

Figure 1. Structure of a three phase five level Diode Clamped inverter (DCMLI).



- Capacitors see current ripple at fundamental frequency or greater depending on modulation strategy
- Precharging and startup are more complex
- Device voltage stress scale with the number voltage levels
- Large number of redundant voltages allow extra opportunities for capacitor voltage balancing

Figure 2. Structure of a three phase five level Flying Capacitor inverter (FCMLI).

B. Voltage Synthesis

DCMLI output voltage synthesis is relatively straight forward. In each phase leg, a set of four adjacent main devices are on at any given time. For the outer voltage levels, the four on devices clamp the phase output to the top or bottom of the DC bus. For the inner voltage levels, the group of 'on' devices acts as a short connecting two of the clamp diodes back–to–back. The other end of these back–to–back clamp diodes are connected to one of the voltage taps along the DC bus. The circuit then can be thought of as a type of multiplexer, attaching the output to one of the five available voltage levels.

FCMLI output voltage synthesis is performed by turning on switches so that adding or subtracting of the capacitor voltages takes place. For the five level inverter considered in this paper, there are four capacitors used in the synthesis of each phase voltage. The capacitors have voltages of V_{dc}, (3/4) V_{dc}, (1/2) V_{dc} and (1/4) V_{dc}. The switch operations are constrained so that the capacitors are never shorted to each other and current continuity to the main DC bus capacitor is maintained.

As an example of voltage synthesis, a phase voltage level of (1/2) V_{dc} can be synthesized in six different ways. The capacitor combinations which produce this phase voltage level are listed below in (1) through (6).

$$V_{dc} - \frac{1}{2}V_{dc} \quad (1)$$

$$V_{dc} - \frac{3}{4}V_{dc} + \frac{1}{4}V_{dc} \quad (2)$$

$$V_{dc} - \frac{3}{4}V_{dc} + \frac{1}{2}V_{dc} - \frac{1}{4}V_{dc} \quad (3)$$

$$\frac{3}{4}V_{dc} - \frac{1}{2}V_{dc} + \frac{1}{4}V_{dc} \quad (4)$$

$$\frac{3}{4}V_{dc} - \frac{1}{4}V_{dc} \quad (5)$$

$$\frac{1}{2}V_{dc} \quad (6)$$

In inverter operation, one is concerned with line–to–line voltages, however, it is convenient to consider one phase at a time. The FCMLI has redundancy at its inner voltage levels. A voltage level is redundant if it can be synthesized by two or more valid switch combinations. In a normal six–

step inverter, the phase voltage levels can only be reached by one combination of switch settings (on or off). The DCMLI does not have phase voltage redundancies due to the different constraints on switch operation imposed by its structure.

The availability of voltage redundancies in the FCMLI provides special opportunities for controlling the voltage on the individual inverter capacitors. In producing the same output voltage, the FCMLI can involve different combinations of capacitors allowing preferential charging or discharging of individual capacitors. This flexibility makes it easier to manipulate the capacitor voltages and keep them at their proper values. It is also possible to transfer real power with the FCMLI which may be advantageous when the compensator is used for balancing of unbalanced loads.

V. EFFECTS OF MODULATION SCHEME

Finding the proper modulation sequence is a multidimensional problem as the inverter must operate with charge balance on the capacitors. Overall DC bus voltage regulation can be achieved by power balance after compensating for losses. Capacitor charge balance may be maintained by using line to line voltage redundancies or other adjustments to the modulation strategy. The problem is less severe in STATCONs where the current is at 90 degrees to the voltage than in VSIs which transfer real power.

A) Capacitor ratings

The modulation scheme of the inverter which produces the output voltage waveform also affects the voltages on the DC capacitors as well as the current through them. Consider that if one uses (3) for synthesizing a voltage level of (1/2) V_{dc} in the FCMLI, the phase current will pass through more capacitors in the phase leg than if we use (6) which passes the phase current through only one of the capacitors. The rms current ratings of the capacitors will necessarily be higher in (3) than in (6). The modulation strategy therefore affects the rms current ratings of the capacitors. The main DC bus capacitor is a special case since the three phases are connected at its terminals and the modulation of all three phases must be factored into finding its ratings.

The modulation strategy also affects the number of microfarads required to suppress voltage ripple. The amount of current seen by each capacitor varies greatly with the modulation sequence employed, particularly in the FCMLI. Optimization of the switch modulation has to be performed in conjunction with the sizing of the capacitors. The switching losses also change with the modulation sequence, as the number of switches changing from off to on or vice versa is different in (1) through (6). As there are a large number of redundancies in the FCMLI, it has yet to be explored what the optimal modulation sequence is.

B) Controlling voltage on each capacitor.

Maintaining the proper voltage on each capacitor is an essential goal of the modulation scheme. The problem of capacitor voltage balancing is somewhat lessened because the compensator is intended to handle only reactive power flow and thus the capacitor energy should remain constant. To maintain the capacitor voltages in the face of losses, the inverter voltage is phase shifted from system voltage and a small amount of real power flows into the inverter.

The capacitor voltages can become unbalanced by asymmetrical losses or by harmonics coming from the power system. Whatever the source of the disturbance, it is desirable to have a means by which the capacitor voltages can be manipulated via the modulation scheme. The alternative would be to have an external apparatus which could charge or discharge each capacitor as needed.

In the FCMLI, the use of voltage synthesis redundancies appears sufficient to readily control each capacitor's charge within a few cycles. A state can be chosen from the available redundancies to that a particular capacitor voltage is adjusted. By using redundancies, the voltage waveform would remain undisturbed by the voltage balancing scheme.

In the DCMLI, the problem is more difficult to solve as there are far fewer redundancies available to the modulation controller. The line–to-line redundancies which do exist in the DCMLI are clustered near the center of the QD voltage plane and thus represent voltage vectors with small amplitudes. If the DCMLI is to use these states in normal operation, the bus voltage utilization will be poor and the device utilization will suffer. PWM of the voltage may also be used to alter the capacitor voltages, although additional losses will be incurred.

The capacitor voltages can be controlled by a modulation scheme which introduces small changes in the switching instants. This method introduces a slight distortion to the voltage but allows selective charging of each capacitor without requiring an increase in the number of switching events.

VI. INVERTER MVA REQUIREMENTS

A. Device MVA Requirements - for five level inverter

While both of the inverter topologies under consideration are capable of producing high quality voltage waveforms, the device count, total device KVA rating, capacitor ratings and number of capacitors are different. A comparison is made of the device MVA requirements of a five level DCMLI and FCMLI relative to a similarly rated six step inverter. The system under consideration is a 10 MVA reactive compensator.

In each inverter, the total DC bus voltage is taken to be 8000 v, however the fundamental component of the phase voltage is different for each inverter. The six step inverter produces a phase voltage whose peak is 1.27 times Vdc/2. The amplitude of the five level inverter's phase voltage is a function of the switching angles used in its modulations strategy.

A five level inverter has two free switching angles, A1 and A2. The angles are usually chosen to minimize the harmonic content and to maximize the fundamental component of the phase voltage. The switching angles in the example that follows were chosen for convience rather than harmonic minimization. With A1 equal to 55 degrees and A2 equal to 85 degrees, the amplitude of the fundamental phase voltage is 1.11 Vdc/2 for both the FCMLI and DCMLI.

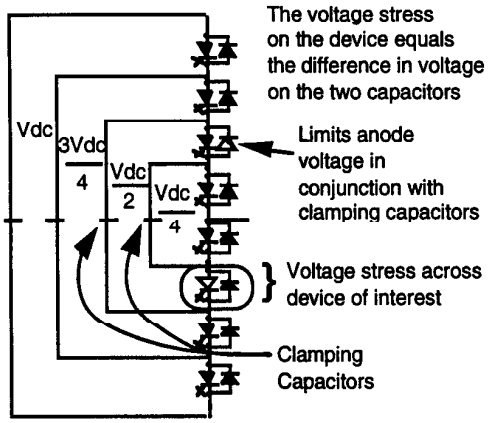


Figure 3. Voltage clamping mechanism in FCMLI

Figures 3 and 4 show how the voltage stresses are found for the FCMLI and DCMLI. The FCMLI uses the difference in the voltage on the capacitors to limit the voltage stress seen by the main switching devices.

The maximum forward voltage of the main devices in the FCMLI is equal to the voltage difference between the capacitor connected to its cathode and the capacitor connected to its anode. Consider the highlighted GTO in Figure 3. The forward voltage of this GTO can be increased until the highlighted antiparallel diode becomes forward biased. At this point, capacitors C4 and C3 provide a clamping voltage equal to $(V_{dc}/2) - (V_{dc}/4) = V_{dc}/4$. All the GTO's in the circuit are clamped in a similar fashion to the voltage difference between adjacent capacitors. The circuit uses no additional clamping diodes but does require a large number of capacitors since there are separate sets of clamping capacitors for each phase leg.

Figure 4 shows voltage clamping components affecting the maximum forward voltage on switch S3. The maximum forward voltage of the main devices is limited by a clamping diode on one end of the device and on the other end, by the offstate voltages of the adjacent switches. Switch S3's anode voltage is limited to (3/4) V_{dc} by the highlighted clamping diode. The clamping diode is connected to a voltage level of (3/4) V_{dc} at a tap point along the DC capacitor string. The cathode voltage of switch S3 is given by the off state voltage of switches S2 and S1. To the extent that the offstate voltages of S1 and S2 can be controlled, limitation of the offstate voltage stress on S3 can be assured.

The fact that the voltage stress on some of the switches of the DCMLI may not be clamped directly by capacitors or diodes is of concern. If the offstate voltage across S1 and S2 was zero, S3 would see a forward voltage of (3/4) V_{dc}. However, in normal operation, the offstate voltages are controllable and can be limited to (1/4) V_{dc}. Consider the sequence of switching leading up to S3 being turned off. Initially, S1, S2, S3, and S4 are on. In the next state, S2, S3, S4, and S5 are turned on and S1 is turned off. The anode voltage of S1 is equal to the output voltage of the phase leg at this point, which is (1/4) Vdc when S2, S3, S4, and S5 are on. The offstate voltage across S1 is clearly determined. The stray capacitance in parallel with S1 will hold this voltage.

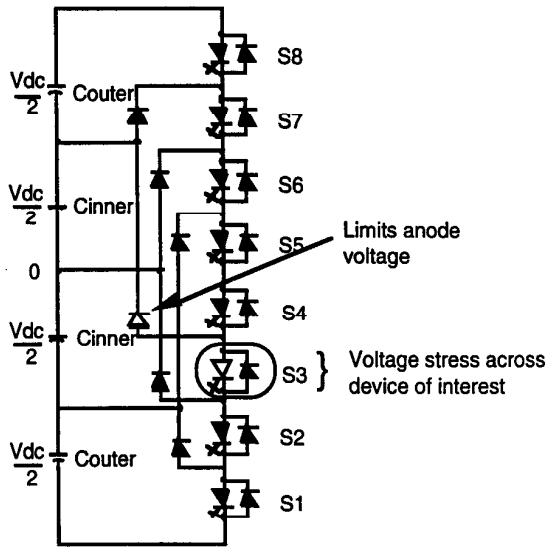


Figure 4. Illustration of voltage clamping in DCMLI

In the next transition, S2 is turned off and S3, S4, S5, and S6 are turned on. The anode voltage of S2 will equal the phase voltage of (1/2) V_{dc} at this point. As S2 turns off, the stray capacitance in parallel with it will charge up to (1/4) V_{dc}. The charging current can flow either through the clamping diode across S1 or into the stray parallel capacitance across S1. If the current flows into stray capacitance across S1, it will charge up until the clamping diode across S1 becomes forward biased.

TABLE II.

COMPARISON OF DEVICE VOLTAGE STRESSES

Inverter	Device	Number of Devices	Voltage Stress on Device (pu)	Total MVA Vdev * Ipeak (pu)
Six Step	reverse diodes	6	1.0	6.86
	GTO's	6	1.0	6.86
DCMLI	reverse diodes	24	0.25	6.86
	clamp diodes	18	0.25 to 0.75	10.3
	GTO's	24	0.25	6.86
FCMLI	reverse diodes	24	0.25	6.86
	GTO's	24	0.25	6.86

In either case, the offstate voltage across each switch (S1 and S2) will be held to no more than (1/4) V_{dc} so long as the stray parallel capacitance across S1 and S2 does not discharge significantly in one fundamental period.

In the DCMLI, the voltage stresses overall are higher. Among the devices in the the DCMLI, the clamp diodes have the highest voltage stress. The high voltage demands on the diodes are less of a problem than having high voltage stress on GTO's. It is common in HVDC systems to have long strings of series connected diodes with adequate voltage sharing.

VII. CAPACITOR MVA REQUIREMENTS

The reactive component requirements are quite different for the FCMLI and the DCMLI. The FCMLI uses separate clamping capacitors for each phase. As mentioned previously, the modulation strategy has a large effect on the ratings of the capacitors.

To compare the cost and size of the capacitors required, we need to decide how to size the capacitors. The DC side capacitors in an inverter serve two functions :

1) limit the peak voltage stress on the devices
2) handle the rms ripple currents passed from the AC to DC side.

The peak voltage stress determines the number of microfarads of capacitance that is needed. The rms ripple current demands define the power rating of the capacitors. There are two types if MVA ratings that are used. The first is the classical ac MVA rating of a capacitor:

$$MVA = \frac{V_{dc}^2}{Xc} \tag{7}$$

Second is the dc power rating of a capacitor:

$$MVA = V_{dc} \times Irms \tag{8}$$

For a given allowable voltage ripple, the capacitance required is found from taking the peak change in charge on the capacitor divided by the allowable ripple voltage.

$$C = \frac{\Delta Q \text{ max}}{\text{Ripple voltage}} \tag{9}$$

where

ΔQ max is the max of the integral of the current into the capacitor minus its average value.
Ripple voltage is the ripple on the capacitor

The value of ΔQ and I rms of the capacitor are found from the waveforms of the currents into the DC bus capacitors. Figures 7 and 8 show the phase voltage and capacitor currents from an EMTP simulation of a five level DCMLI. The currents in the inner and outer capacitors are shown and ΔQ max and Irms values can be calculated assuming that the phase currents are pure sinusoidal sources. The values of ΔQ max and Irms in the inner and outer capacitors are dependent upon the modulation angles A1 and A2, so that the results are valid only for the particular modulation angles used.

Figure 5 shows the capacitor currents for one phase leg of a five level FCMLI. The sequence of inverter switch configurations is shown on the left hand side. The dark lines trace out the current path through the capacitors. The current waveform for the DC bus capacitor (C1) reflects the influence of all three phases. Note that all three phases share the same DC bus capacitor in the FCMLI. The current is the DC bus cap (C1) reflects the influence of all three phase currents.

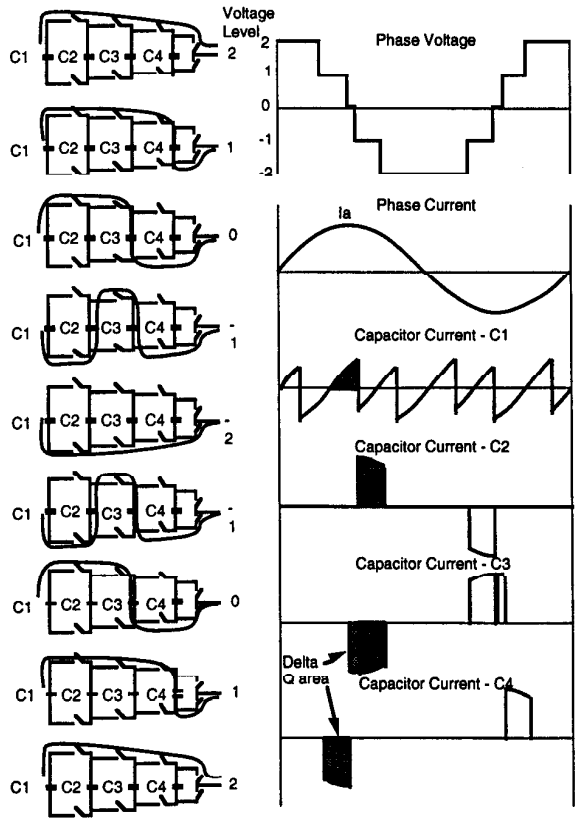


Figure 5. Phase voltage synthesis and capacitor current waveforms for five level FCMLI.

The frequency of the ripple current in the DCMLI's capacitors has been observed to be mostly third harmonic in the outer capacitors and sixth harmonic in the inner level capacitors. The ripple frequency of the current in the FCMLI's capacitors is dependent on the modulation strategy. For the particular modulation strategy shown, C4 through C2 see fundamental frequency current ripple and C1 sees sixth harmonic current.

There is a large number of redundant switch sequences which produce the same phase voltage waveform but use different combinations of capacitors to synthesize the voltage. The rms current and peak ΔQ are likely to be different for each modulation strategy and the one which minimizes the capacitor cost and system losses should be used.

VIII. SIMULATION RESULTS

A five level DCMLI was simulated using EMTP. The linking inductance was 20 mH, and the DC side capacitors were 500 μF each. The AC system phase voltage had an amplitude of 5600 volts.

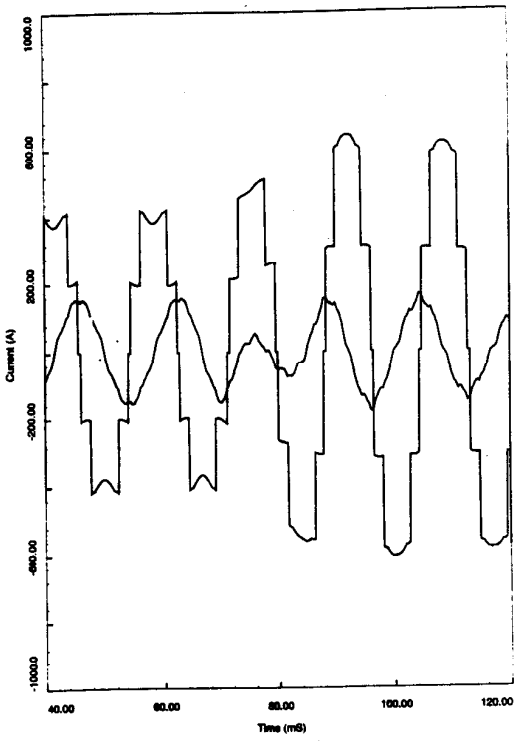


Figure 6. EMTP simulation of five level inverter with var production changed from inductive to capacitive by a change in the DC bus voltage.

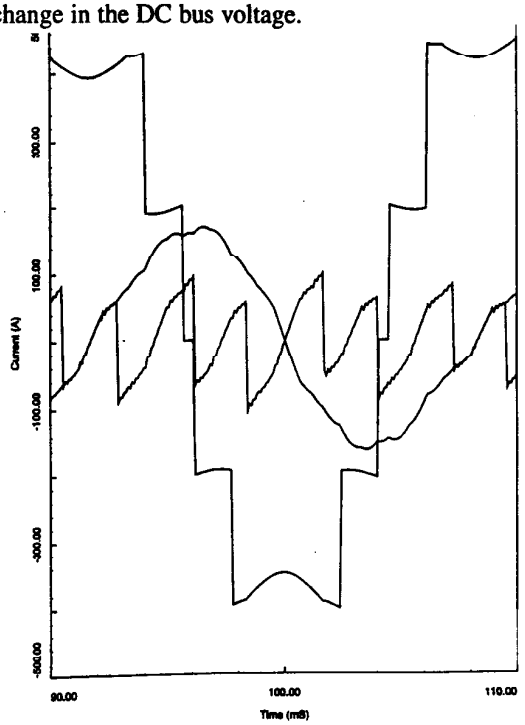


Figure 7. EMTP simulation of five level DCMLI showing phase voltage waveform and inner capacitor current.

The performance of the inverter as a source of reactive power is shown in figure 6 where the var production is changed from inductive to capacitive by a step change in the DC bus voltage. The inner and outer capacitor currents are shown in figures 7 and 8, respectively.

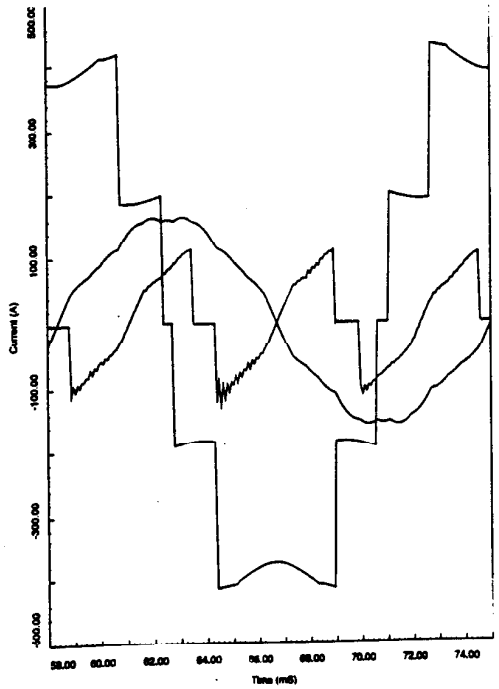


Figure 8. EMTP simulation of five level DCMLI showing phase voltage waveform and outer capacitor current.

IX. CONCLUSIONS

Modulation strategy has a very large effect on the capacitor ratings so that it is difficult to compare the capacitor Mvar requirements of the three inverter topologies. The FCMLI has thousands of combinations of states which can produce the same sinewave approximation. In one comparison without optimization of the capacitor ratings, the DCMLI was seen to require capacitor power ratings 50 % higher than a comparable six step inverter. The FCMLI capacitor requirements were 400 % higher than the six step inverter.

The benefits of the multilevel inverter must be weighed against the cost of the extra devices and capacitors it requires.

X. ACKNOWLEDGEMENTS

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