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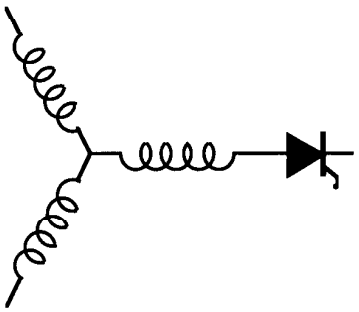

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Abstract - *This paper proposes a passively clamped quasi resonant dc link converter topology which adds a small switched inductor to the conventional passively clamped resonant dc link inverter. The problem with high voltage stress in the conventional inverter is resolved, while its ruggedness, reliability and high power handling capability are preserved. The device voltage stress can be reduced from 2 per unit to 1.1-1.3 per unit, and PWM operation and link resonance control become easily fulfilled. Analysis and simulation have demonstrated the successful operation of the new topology. The introduction of the auxiliary switched inductor circuit is also well justified by its requirement of components with low stresses and ratings. Application of the quasi resonant inverter is aimed at those requiring high power, high efficiency, low EMI and a high quality spectrum.*

I. INTRODUCTION

Various soft switched voltage source inverter (VSI) and current source inverter (CSI) topologies have been intensively studied for high performance drive applications in recent years [1-4]. The elimination of switching losses in a soft switched inverter allows better utilization of the transistor switches, which facilitates the devices to overcome their physical limitations and provides higher switching frequency, low dv/dt and di/dt stresses, and reduction of EMI.

For soft switched VSI's, the resonant dc link inverter possesses the simplest structure which adds only an inductor and a capacitor to a hard switched dc link VSI [2]. As the inverter impresses substantial voltage stress (about 2.5 per unit) across the devices, the actively clamped resonant dc link (ACRL) inverter has been proposed to limit the device voltage stress to 1.3-1.5 per unit [4]. The active clamp, however, gives rise to a number of problems. Firstly, a "per cycle" charge balance of the clamp capacitor is required to sustain link oscillation. That is, losses in the resonant components and the clamp switch must be anticipated and are compensated by storing sufficient initial current in the resonant inductor before the resonant cycle. The compensation technique tends to pump excessive charge into the clamp capacitor in order to ensure that the link voltage will return to zero. Unfortunately, the excessive charge accumulation in the clamp capacitor causes the clamp voltage to increase. Thus, a regulation loop is required to coordinate the conflict between sustaining link resonance and limiting the clamp voltage increase. The regulation requires a complicated control algorithm for the clamp switch which relies either on precise current sensing or current observer [5]. The link resonance, therefore, becomes difficult to maintain over all operating conditions. Another apparent drawback of the "per cycle" charge balance of the clamp capacitor is that it prevents variation in the width of the link voltage pulses from cycle to cycle. To produce the same spectrum quality, the switching frequency must be 4 to 5 times higher than a hard switched PWM strategy. High link frequency can elevate the clamp factor and worsen the losses in the active clamp circuit, especially at high power level. As a result, the ACRL inverter is generally limited to a power level below 50 KW.

The needs for simple resonance control, PWM capability and lower device stresses therefore become the key issues for a soft switched inverter at higher power levels. The auxiliary commutated resonant pole (ACRP) inverter [6,7] possesses those desired features. However, the circuit requires six extra switches and three additional inductors to accomplish the soft switching task. Hence, this approach is attractive only for very high power rating (roughly greater than 500 kW) where its cost vs. performance can be justified.

Recently, the quest for alternatives has led to the parallel resonant dc link structure [8], which has lately evolved to several topologies nominally referred to as the quasi resonant dc link (QRL) inverter [9,10]. Unlike the ACRL, a QRL inverter connects its LC tank in parallel with the dc voltage source. Due to the parallel structure the resonant tank is minimally involved with power transfer and the resonant circuit is activated only during the resonant transient. PWM capability becomes a true reality and the device voltage ratings never exceed 1 per unit. However, the soft switching relies on a main resonant switch inserted in series between the dc voltage source and the resonant bus. The switch has to withstand all three phase load currents and to operate at high switching frequency, usually several times the switching frequency of the main inverter switches in order to ensure a resonant transition in all three phases. This option is not attractive for practical high power application because the losses in the main resonant switch are much higher than the active clamp switch in the ACRL. Thus, no higher power handling capability than the ACRL is expected.

Passively rather than actively clamping the link voltage removes the problem with the highly stressed clamp switch [11]. The passively clamped resonant dc link (PCRL) inverter has been built with a 200 KW capacity [11]. However, its requirement for a device voltage rating of more than 2 per unit must clearly be removed before gaining any practical acceptance. Therefore, a suitable resonant link inverter able to handle power ratings up to 500 KW has yet to be realized.

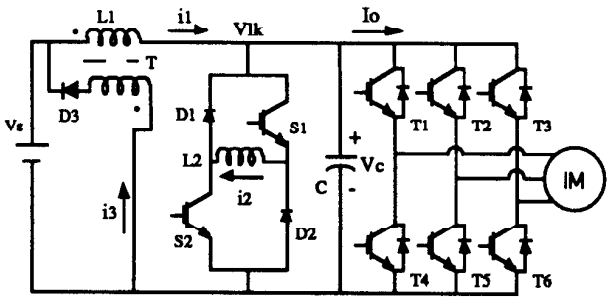


Fig. 1 Passively clamped quasi resonant dc link inverter

This paper is concerned with re-investigating the PCRL topology, making use of its many advantages while getting rid of its disadvantages. It is found that by adding a parallel switched inductor to the PCRL circuit, the problem with high

voltage stress can be solved and PWM operation and resonance control become easily fulfilled, while all the ruggedness and reliability inherent with the passive clamp topology are preserved. The device voltage stress can be reduced to as low as 1.1-1.3 per unit in comparison with the 1.3-1.5 requirement in ACRL or 2.0 requirement in the PCRL because a high resonant frequency is possible. No charge balance or clamp voltage regulation algorithms are required to operate the inverter. Performance comparable to the QRL inverter is achieved and most of QRL structures can also be inherited to realize the switched inductor. The limitation of using a switch in series with the dc link power flow in the QRL is eliminated by replacing the switch with an inductor in the main dc link. This change is believed to be a much preferred structure because an inductor can much more readily handle high power than a transistor. Like the PCRL inverter this passively clamped quasi-resonant link (PCQRL) inverter topology is expected to be able to operate at high power levels up to 500 KW.

II. PASSIVELY CLAMPED QUASI RESONANT DC LINK INVERTER

The proposed passively clamped quasi resonant dc link (PCQRL) inverter is shown in Fig. 1. The circuit is realized by adding a small switched inductor L2 to the conventional passively clamped resonant dc link (PCRL) inverter. In contrast to the conventional PCRL [11], the clamp transformer, T, is designed to have a clamp factor, K, equal to 1.1-1.3 instead of more than 2. For current reset purposes, the switched inductor L_2 is realized by two auxiliary switches S_1 and S_2, which are driven by the same gating signal, and two diodes D_1 and D_2. The primary of the passive clamp transformer, T, also serves as the main resonant inductor L_1, which is preferred by using the coaxial transformer technique [12].

It is noted that the switched inductor circuit is similar to that used in a quasi resonant dc link inverter [9]. It may be further simplified to reduce the device count by several other methods as proposed in the literature [13,14]. However, an even more attractive simplification which takes advantages of magnetic coupling and leads to a minimum device count and the best component utilization will be discussed later in this paper.

The operation of the inverter can be illustrated by referring to Figs. 1, 2 and 3. Assume a constant dc link load current, I_o. Before a resonant cycle is initiated the link voltage, V_c, is nominally clamped at a voltage between V_s and KV_s. The auxiliary inductor L_2 is reset to zero current condition and the auxiliary switches S_1 and S_2 are off. Current i_1 of inductor L_1 is thus equal to the dc link load current I_o. These conditions represent the steady state after a resonant transition which is indicated as mode 0 (M0 in Fig. 2). In this mode, because the passive clamp limits the link voltage to KV_s, the resonance between L_1 and C is disabled and the steady state will remain as long as the auxiliary switches S_1 and S_2 are off.

Whenever a PWM switching command is generated, the switches S_1 and S_2 are turned on first in a zero current switched (ZCS) manner to initiate a resonant transition. The link voltage, V_c, is applied to inductor L_2 and forces the inductor current to increase. The link voltage starts to drop and the resonance between L_1, L_2 and C is thus triggered. This process is shown as mode 1. The waveforms are easily explained by observing that, when switches S_1 and the S_2 are turned on, the load current does not change and the current in th main inductor L_1 can not increase rapidly to supply current to L_2 so that the capacitor dumps its energy into the inductor L_2. The resonance, or capacitor discharge, will drive the link voltage towards a value below zero.

After the link voltage drops to zero, mode 2 is entered. The link voltage is then clamped at zero by the anti-parallel diodes in the inverter switches. This zero link voltage will be maintained for a sufficiently long period of time as long as the auxiliary switches S_1 and S_2 remain closed. The inverter switches can then perform the required soft switching during mode 2. At the zero link voltage condition, the current in inductor L_2 will not change, while current in L_1 will increase linearly to store sufficient energy for link voltage ramp-up in mode 3. After the inverter poles finish the switching as a PWM modulation commanded, switches S_1 and S_2 are then turned off in a zero voltage switching (ZVS) manner and the link proceeds into mode 3.

The operation of mode 3 is exactly the same as the link ramp-up process of a conventional resonant dc link circuit if we consider that the cathode of diode D_1 is connected to dc voltage source V_s instead of V_{1k}. In this case, the current i_2 in auxiliary inductor L_2 is drained directly back to Vs, and the resonance between L_1 and C will drive the link voltage towards $2V_s$ until it hits the clamped voltage KV_s.

When link voltage reaches KV_s, the secondary of the clamp transformer, T, produces a voltage equal to V_s which causes a positive bias across the clamp diode, D_3, and forces it to conduct. The excessive energy or current is then feedback through the clamp transformer to the dc voltage source, V_s, and the link voltage, V_c, is clamped at the desired value KV_s. The clamp action is denoted as mode 4. After the energy is fed to the source, the clamp action will be relieved and the current in inductor L_1 continues to supply the steady state dc link load current I_o. The inverter returns to steady state mode 0.

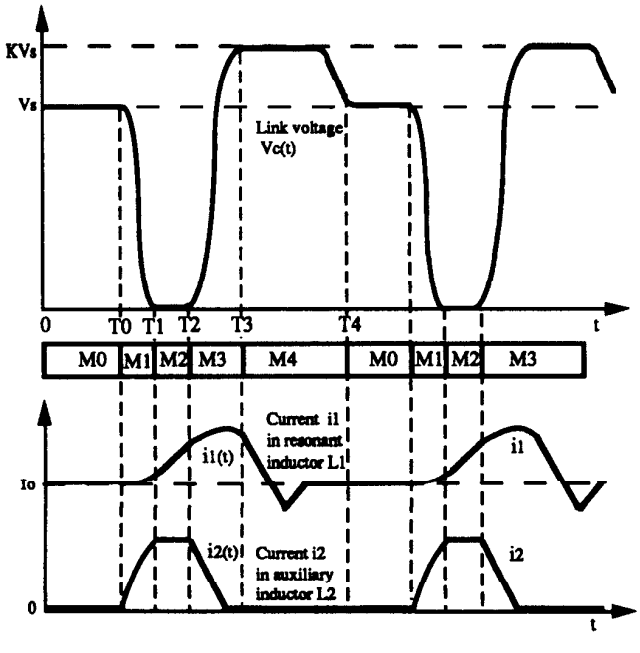


Fig. 2 Resonant link waveforms

It is important to note that when the diode D1 is connected to V_{lk} as shown in Fig. 1, the resonance between L_1, L_2 and C will occur to pull up the link voltage. This variation will mainly change the resonant frequency of mode 3. In a practical implementation, either means of diode connection can be used.

III. ANALYSIS OF PCQRL INVERTER

An analysis of the PCQRL inverter can be performed based on the equivalent circuits for each mode which are shown in Fig. 3. Because the resonant transient occurs only during a very short period of time, the dc link load current, I_O, is assumed to be constant during a resonant cycle. Also, for clamp action, perfect coupling between the primary and the secondary of the coaxial clamp transformer is assumed, which means that the link voltage will be clamped exactly at KV_S. As is indicated in Fig. 2, the time at which each mode ends will be denoted as T_i for i=0 to 4.

Mode 0: Steady State (S_1 and S_2 Off; D_1 and D_2 off)
This mode is actually a pseudo steady state in the sense that the link voltage is not exactly equal to V_S. As the link capacitor is very small, the link voltage, V_C, is not a stiff source. In fact, the link voltage may swing to the clamp voltage KV_S or below the dc source voltage V_S depending upon how the link load current changes during this mode. However, the resonance between L_1 and C together with the clamp action tends to stabilize the voltage to V_S. Since the auxiliary switches are off, the current in L_2 is equal to zero. Thus, the link state can be described by

$$V_c(t) = V_s \tag{1}$$

$$i_1(t) = I_o \tag{2}$$

$$i_2(t) = 0 \tag{3}$$

Mode 1: Link Voltage Ramp-Down (S_1 and S_2 on; D_1 and D_2 off)
The resonant transient is initiated and link resonance between L_1 and L_2 and C occurs. Based on the equivalent circuit in Fig. 3b, the link current and voltage can be derived as

$$V_c(t) = \frac{V_S}{L_1 + L_2}[L_2 + L_1 \cos\omega_1(t - T_0)] \tag{4}$$

$$i_1(t) = I_o + \frac{V_S}{\omega_1(L_1 + L_2)}[\omega_1(t - T_0) - \sin\omega_1(t - T_0)] \tag{5}$$

$$i_2(t) = \frac{V_S}{\omega_1(L_1 + L_2)}[\omega_1(t - T_0) + \frac{L_1}{L_2}\sin\omega_1(t - T_0)] \tag{6}$$

where

$$\omega_1 = \frac{1}{\sqrt{L_{12}C}}$$

and

$$L_{12} = \frac{L_1 L_2}{L_1 + L_2}.$$

It is seen that the necessary and sufficient condition for bringing the link voltage to a negative value is that L_2 be smaller than L_1. Also, the duration of mode 1 can be obtained from $V_c(t)=0$. which yields

$$\cos\omega_1(T_1 - T_0) = \frac{L_2}{L_1} \tag{7}$$

Mode 2: Zero Link Voltage (S_1 and S_2 on; $V_c = 0$)
This mode will be maintained until S_1 and S_2 are turned off. Ideally, the duration of mode 2 would be zero. However, due to the storage time in realistic switching devices, mode 2 has to be held for certain period to ensure inverter soft switching. From the equivalent circuit, for this mode,

$$V_c(t) = 0 \tag{8}$$

$$i_1(t) = i_1(T_1) + \frac{V_s}{L_1}(t - T_1) \tag{9}$$

$$i_2(t) = i_2(T_1) \tag{10}$$

Although the link voltage may automatically increase if the duration of mode 2 is held too long. In a practical application, a prolonged mode 2 will always be avoided to prevent the overload of current in inductor L_1. Therefore, the duration of mode 2 is always controlled by the turn-off of switches S_1 and S_2.

Mode 3: Link Voltage Ramp-Up (S_1 and S_2 Off; D_1 and D_2 on)
Consider the case that the cathode of diode D_1 is connected to dc voltage source V_S instead of V_{lk}. In this situation, the current in the auxiliary inductor L_2 is drained back to V_S, and the resonance between L_1 and C drives the link voltage towards $2V_S$ until it hits the clamped voltage KV_S. Since $i_1(T_2)$ is larger than I_o. the link voltage and current in mode 3 are described by

$$V_c(t) = V_s[1 - \cos\omega_2(t - T_2)] \tag{11}$$

$$i_1(t) = I_o + [i_1(T_2) - I_o]\cos\omega_2(t - T_2) + \frac{V_s}{Z}\sin\omega_2(t - T_2) \tag{12}$$

$$i_2(t) = i_2(T_1) - \frac{V_s}{L_2}(t - T_2) \tag{13}$$

where

$$\omega_2 = \frac{1}{\sqrt{L_1 C}}$$

and

$$Z = \sqrt{\frac{L_1}{C}}$$

Mode 4: Clamp Action (S_1 and S_2 off; D_3 on)
Clamp action occurs when link voltage reaches KV_S. The equivalent circuit for mode 4 is shown in Fig. 3e. Unlike the pseudo steady state mode 0 where diode D_3 basically does not conduct for most of the time, the clamp mode is characterized by full conduction of the diode D_3. Under the ideal coupling assumption, the link voltage, V_C, will be held at KV_S during this mode. As no current can flow in capacitor C. the link current i_1 must jump from $i_1(T_3)$ to I_O. As a consequence, the clamp current i_3 will increase abruptly at the beginning of mode 4 to satisfy the continuity of flux linkage. Based on above observation, it is trivial to use the equivalent circuit to obtain the result that

$$V_c(t) = KV_S \tag{14}$$

$$i_1(t) = I_o \tag{15}$$

$$i_3(t) = (1-K)^2[i_1(T_3) - I_o] - \frac{V_s}{L_3}(t - T_3) \qquad (16)$$

where L_3 is the self inductance of the secondary of the clamp transformer T.

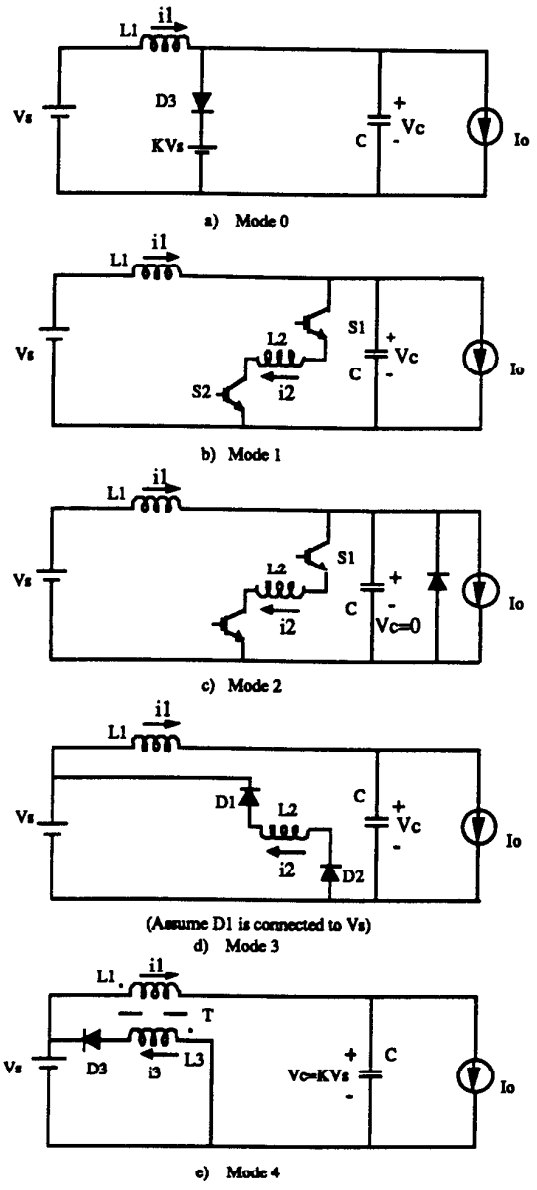


Fig. 3 Equivalent circuits

IV. CHARACTERIZATION OF PCQRL INVERTER

Based on above analysis, several major features of the new PCQRL topology can be revealed. First, it is seen that one of the key advantages of this circuit in addition to its PWM capability is that the introduction of the auxiliary inductor also eliminates the energy balance control loop in the conventional resonant link converters. Link voltage return-to-zero which remains a major control issue in the conventional converters becomes an inherent mechanism for this combined parallel and serial LC resonant link structure. In fact, from equation (4), it can be seen that link voltage can be driven to a voltage below zero simply by proper choice of the relative value of L_2 to L_1.

As the choice of the resonant link parameters L_1, L_2 and C heavily influences the peak current stress in inductors L_1 and L_2, it is important to derive a formula for determining the peak current in inductors L_1 and L_2. Referring to the analysis, it is found that the current of inductor L_1 keeps increasing from mode 0 to mode 3, so that the peak current will occur in mode 3. By equation (12),

$$i_{1peak} = I_o + \sqrt{(\frac{V_s}{Z})^2 + (i_1(T_2) - I_o)^2} \qquad (17)$$

It is seen that, for a given I_o and V_s, the peak current i_1 can be reduced if the characteristic impedance Z is large and that current increment in mode 1 and mode 2, $i_1(T_2)-I_o$, is minimized. From equations (5), (7) and (9), the following result is obtained

$$(i_1(T_2) - I_o) = \frac{V_s}{\omega(L_1+L_2)} K_{i_1} + \frac{V_s}{L_1}(T_2 - T_1) \qquad (18)$$

where

$$K_{i_1} = \omega_1(T_1 - T_0) - \sin\omega_1(T_1 - T_0)$$
$$= \pi - \cos(\frac{L_2}{L_1}) - \sqrt{1 - (\frac{L_2}{L_1})^2} \qquad (19)$$

For constant resonant frequency ω_1 and dc source voltage V_s, the peak current is thus determined merely by inductances L_1, L_2 and the duration of mode 2, T_2-T_1.

The same property applies to the peak current in L_2. It can be shown that

$$i_{2peak} = \frac{V_s}{\omega_1(L_1+L_2)} K_{i_2} \qquad (20)$$

where

$$K_{i_2} = \omega_1(T_1 - T_0) + \frac{L_2}{L_1}\sin\omega_1(T_1 - T_0)$$
$$= \pi - \cos(\frac{L_2}{L_1}) + \sqrt{1 - (\frac{L_2}{L_1})^2} \qquad (21)$$

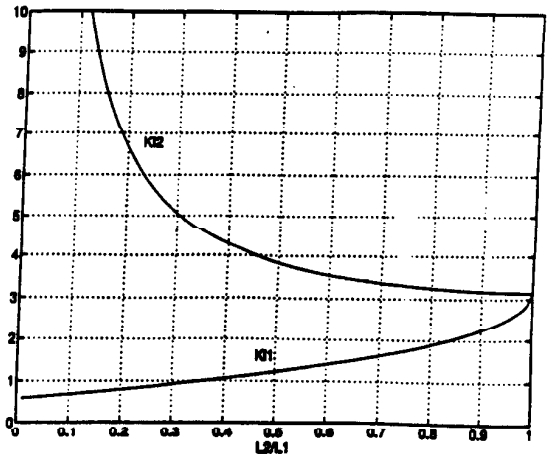


Fig. 4. Curves for designing inductor currents - Ki_1 and Ki_2 vs. L_2/L_1

Notice that Ki_1 and Ki_2 depend only on the relative value of L_1 and L_2. A plot for Ki_1 and Ki_2 vs. L_2/L_1 is given in Fig. 4. It can be used to choose an optimal L_2/L_1 to reduce the current increment in inductor L_1 during mode 1 and to determine the peak current stress of inductor L_2. It is interesting to find that the current of inductor L_1 during mode 1 can be controlled to be almost constant by choosing an appropriate ratio of L_2 to L_1. Due to this phenomenon, the resonant or ac current component in inductor L_1 is mainly produced in mode 2 to mode 4, which suggests that the characteristic behavior of the current waveform in inductor L_1 is similar to that in a conventional ACRL inverter.

Another important characteristic of the PCQRL inverter is that the resonant or ac current component in L_1 and L_2 is independent of the dc link load current I_o. This means that, no matter how large the load current, the resonant current or resonant energy circulated inside the inverter is the same. Hence, the topology will favor a high power application as the relative ratings of ac current components in the inverter will decrease proportionally.

Because of the quasi-resonant or resonant transient property, link resonance is activated only when a PWM switching instant is commanded. The resonant frequency can be designed to be very high so that commutation takes place only over a very small fraction of an average PWM switching cycle. As a result, one apparent advantage over previous resonant dc link converters can be easily met, that is the voltage-second balance of the resonant inductor L_1 and thus a small clamp factor of 1.1-1.3 can be readily implemented. On the other hand, for the same clamp factor, a higher link frequency can be realized in the quasi resonant scheme.

In fact, for any resonant dc link type inverter, given the desired clamp factor and the device physical parameters, i.e., the rise time T_r, fall time T_f and storage time T_s, the relationship between maximum average link frequency, f_{avg}, and the minimum clamp factor, K, can be calculated based on the voltage-second balance equation of the resonant inductor L_1. By using a linearization approximation of the link voltage waveform as shown in Fig. 5, the maximum average link frequency is given by

$$f_{avg} = \frac{K-1}{K} \frac{1}{T_s + \frac{1}{2}(T_r + T_f)} \text{ (Hz)} \qquad (22)$$

As an example, for certain IGBT devices with T_r=1.5μs, T_s=1.0μs and T_f=1.2μs, the K vs. f_{avg} curve is drawn in Fig. 6. It is apparent that for a given clamp factor, the maximum link frequency is limited. Any attempt to further increase the link frequency can only be achieved with the sacrifice of a considerable increase in the clamp factor.

Finally, it should be noted that as the resonant frequency is decoupled from the link frequency in the quasi resonant dc link inverter, the inverter can easily produce a waveform close to the physical T_r, T_s and T_f specifications, it is expected that a better utilization of device resources can be achieved. In addition, the feasibility for designing a high resonant frequency while maintaining a low PWM switching frequency will be beneficial. The reasons are that the low PWM switching frequency will further decrease the inverter switching losses and that the high resonant frequency will make it possible to use very small resonant LC components. The resonant energy involved is also reduced considerably. Due to the decoupling of the switching frequency from the resonant frequency, any PWM modulation strategy including the delta modulation method can be used freely to synthesize the inverter output voltage waveforms.

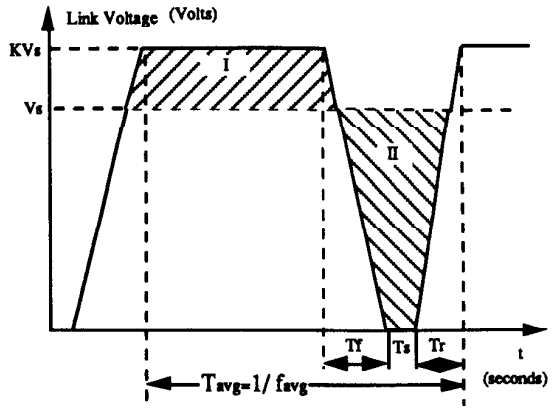


Fig. 5 Equal area criterion for determining relationship between clamp factor and link frequency

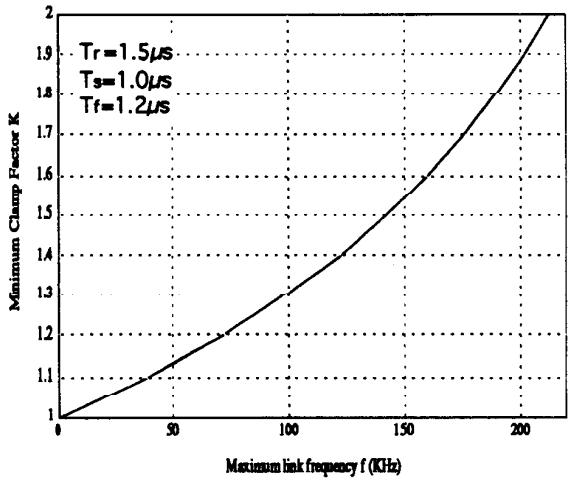


Fig. 6 Relationship between clamp factor K and link frequency f_{avg}

V. SIMULATION RESULTS

Simulation has been performed to verify the analysis and to demonstrate the inverter operation. As is known, the choice of the resonant link parameters L1, L2 and C heavily influence the peak current stresses in inductors L_1 and L_2. It is necessary to optimize the link parameters based on specific inverter design specifications.

As the device physical limitation is an important factor in link design, an IGBT device with a rise time T_r=1.5 μs, a fall time T_f=1.2 μs and a storage time T_s= 1.0 μs is used as the inverter switches. To utilize the devices to their limitation, one can design a link voltage waveform such that T_1-T_0=T_f, T_2-T_1=T_s and T_3-T_2=T_r. By choosing L_1 to be 20 μH, the curves in Fig. 4 are used to determine the optimal value for L_2, which indicates that L_2 equal to 8 μH will permit small ac current

components in both L_1 and L_2. The rise time and fall time parameters are then used to determine the resonant frequency ω_1 and ω_2 and, thus, the link capacitance C. Based on the above procedures, a 15 KW PCQRL inverter with a 320 V dc bus has been designed. The main inverter parameters are included in Table 1. By the peak current formulas (15) and (18), it is calculated that the peak ac currents in inductors L1 and L2 will be only 29.0 A and 28.5 A, respectively.

For a constant dc link load current I_o equal to 50 A, a simulation has been performed to demonstrate the operation of the resonant converter and the related link waveforms. The gating signal of the auxiliary switches is trigged by a constant frequency of 20 KHz. The zero link voltage condition is detected to determine the turn-off time of switches S_1 and S_2. The simulated link voltage and current waveforms are plotted in Fig. 7. It is seen that the current in inductor L_1 is maintained around 50 A due to the constant dc link load current condition. The peak current of inductor L_1 is about 80 A, which means that the resonant or ac component is only about 30 A. The current waveform in inductor L_2 shows a peak current of only about 30 A. It is important to notice that since the resonant frequency is very high, the ac components exist only during a very short interval in each resonant cycle. Thus the rms ac component will be much smaller than the peak value. From the simulation results, it is also seen that the link voltage and current waveforms as well as the peak current parameters are in good agreement with theoretical prediction.

In comparison with an actively clamped resonant link (ACRL) inverter, the current waveform of the main resonant inductor L_1 is almost the same, although, with much smaller resonant or ac component circulated. The initial current of inductor L_1 in mode 3 is usually slightly higher than the load current due to the link pull-down process, which automatically satisfies the condition for link voltage pull-up. Thus, no current monitoring nor complex regulator is required to control the link resonance or oscillation. This feature is one of the key advantages of the PCQRL circuit in addition to its PWM capability, low device current ratings and low voltage stresses.

In comparison with the conventional passively clamped resonant link (PCRL) inverter, the quasi resonant converter produces a much smaller clamp current than that in the PCRL. From the simulation result, it is found that the peak clamp current is less than 5 A due to the use of a low clamp factor of 1.1. The disadvantage is that the secondary of the clamp transformer produces a high voltage equal to $V_s/(K-1)$ which imposes a high reverse break-down voltage to the clamp diode D3. However, this is not deemed as a serious drawback since several series diodes could be readily used in a high power application.

To demonstrate the PWM capability of the PCQRL inverter, a three phase sinusoidal PWM modulation has been implemented to control the operation of inverter switches to synthesize the output waveforms. A wye-connected three phase R-L load with R = 5 ohms and L = 6.67 mH is connected to the inverter. The triangle reference frequency is 6 KHz. The sinusoidal reference frequency is 50 Hz and the modulation index is 1.0. The output line to line voltage and load current waveforms are presented in Fig. 8.

Simulation results show that the inverter operates satisfactorily for three phase operation. The inverter outputs a 50 Hz fundamental current waveform with almost the same spectral quality as that of a hard switched dc link PWM inverter switched at the same 6 KHz. The line to line voltage waveform is also very similar to a hard switched PWM.

Table 1 Inverter Parameters

Inductor L_1	20 μH
Inductor L_2	8 μH
Capacitor C	60 nF
DC Source Vs	320 V
Clamp Factor K	1.1
Pull-Up Time (T1-T0)	1.5 μs
Link Short Period (T2-T1)	1.0 μs
Pull-Down Time (T3-T2)	1.2 μs

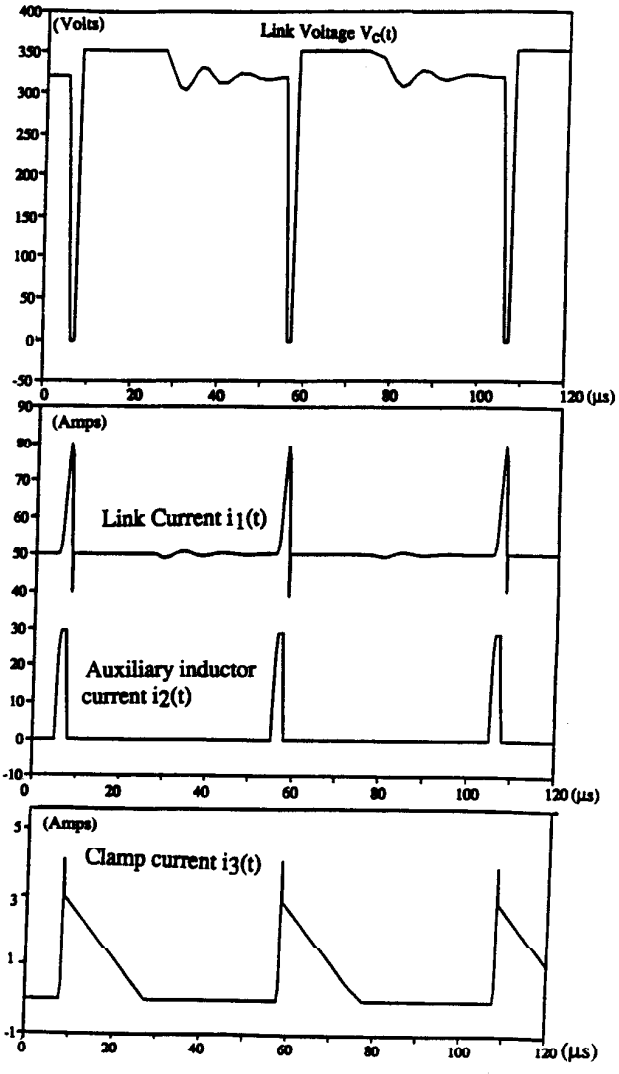
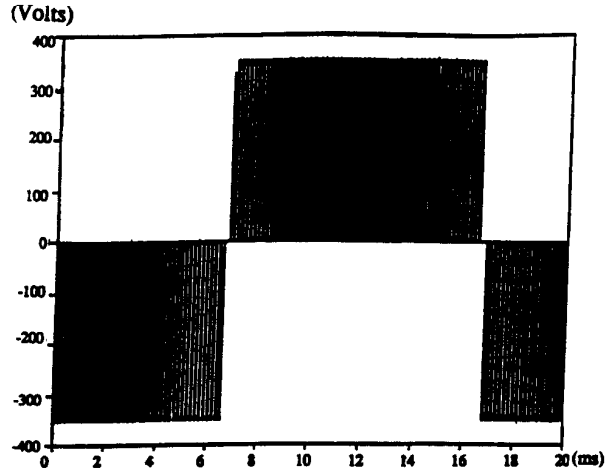
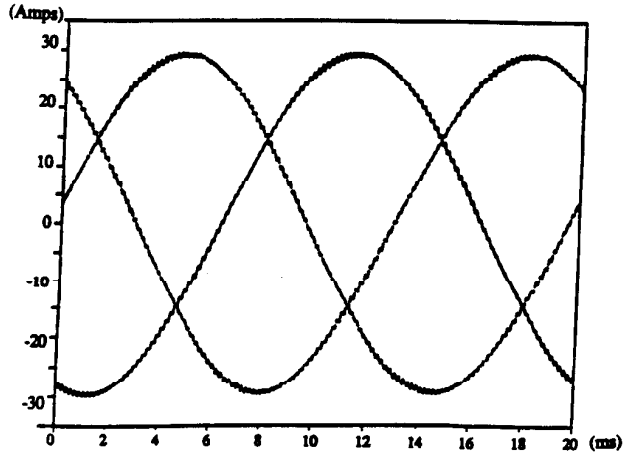


Fig. 7 Simulated Link Waveforms for a constant 20 KHz link frequency and a constant 50 A dc link load





Top: Line to Line Voltage
Bottom: Three Phase Load Current

Fig. 8 Simulated three phase line voltage and load current with sinusoidal PWM operation
(Output fundamental frequency 50 Hz,
Modulation Index=1.0,
Triangle reference frequency = 6 KHz)

VI. FURTHER SIMPLIFICATION OF PCQRL INVERTER

Another version of the PCQRL converter topology has also been developed which is included in Fig. 9. It can be seen that the difference in this version is the reduction of the auxiliary switch count from two to one. This reduction is made possible by mutual coupling between inductor L_1 and inductor L_2. The operation modes and operating principles are similar to those of the previous case except that the mutual coupling of L_1 and L_2 will cause the current in inductor L_2 to be reversible. Thus, the two-switch inductor reset circuit can be simplified to a one-switch circuit. When inductor L_2 is switched on, its current will increase and then become reversed. Once the current reverses, the auxiliary switch is then turned off in a zero voltage switching (ZVS) manner.

As the clamp action and the conduction of inductor L2 occur at different time instants, it is possible to construct inductor L2 to share the same magnetic core with the inductor L1 which would lead to a considerable reduction in cost and while providing a minimum device count. A detailed discussion of this alternative topology will be given in a future paper.

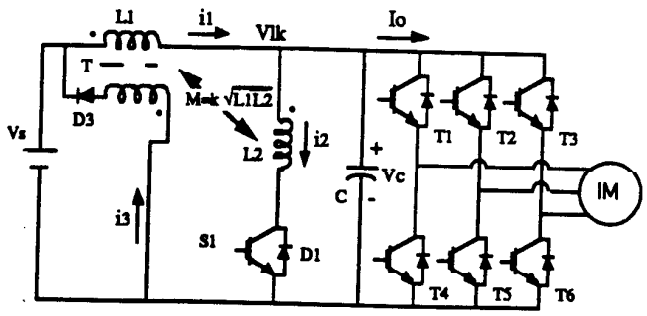


Fig. 9 PCQRL Inverter with magnetic coupling between L1 and L2

VII. OTHER CLAMP METHODS

While a passive clamp transformer is used to provide the link voltage limitation in the PCQRL inverter, the new topology is by no means restricted to this clamp method. In fact, if the dc source is provided by a battery instead of a diode and capacitor rectifier, the clamp circuit can be simplified as shown in Fig. 10. In Fig. 10, the secondary of the passive clamp transformer is simply replaced by a low voltage dc source with a voltage equal to $(K-1)V_S$ and a clamp diode. In the case of small V_S (for example and electric vehicle), the clamp could even be realized using only diodes since $(K-1)V_S$ may become equal to a few diode voltage drops.

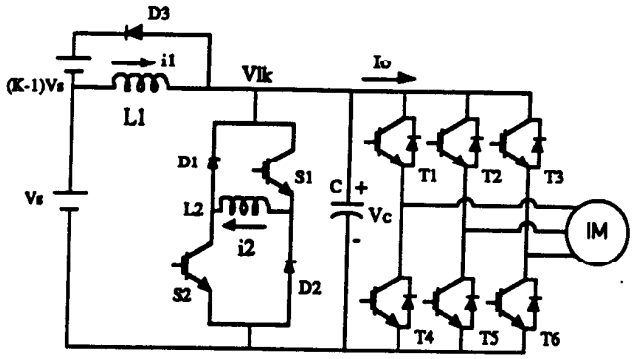


Fig. 10 Quasi resonant inverter with a diode clamp

VIII. CONCLUSIONS

This paper presents a novel topology for resonant dc link converters. The topology allows a conventional passively clamped resonant dc link (PCRL) inverter to be able to operate at a low device voltage rating of 1.1 to 1.3 per unit instead of the previous requirement of more than 2 per unit. By changing the continuous resonant operation mode into the resonant transition or the so called quasi-resonant operation mode, the restriction on resonant converters modulation methods can be eliminated and pulse width modulation (PWM) of any type can be easily implemented. Another important improvement of the quasi-resonant converters is that the resonant current

components and, thus, the associated resonant losses can be reduced considerably.

Analysis and simulation were performed to reveal the various characteristics and the performance of the new inverter. It is seen that the novel topology allows the use of simple control to initiate and maintain a resonant cycle, which is different from the conventional resonant dc link converters where closed-loop regulation of link energy balance is required for sustaining resonance. The resonant energy which circulates inside this type of resonant link is parameters dependent rather than load dependent. Therefore, the link can be designed to offer high current capability without an increase in the resonant ac current ratings of the resonant components.

The topology also preserves the high power handling capability, ruggedness and reliability of the conventional passively clamped resonant circuit. With a dc battery source, the voltage clamp circuit does not require a transformer coupling method. Ordinary diode clamp method can also be used to provide a cost effective low power implementation.

Another new version of the PCQRL topology which employs mutually coupled inductors has been presented which further offers better utilization of magnetic cores and the minimum device count. The alternative version requires only one additional switch and one three winding transformer. Together with compatibility to other clamp methods, it is apparent that the PCQRL topology provides for various simple structures which can realize near-optimal utilization in different applications.

A practical implementation of this PCQRL inverter is being developed. Experimental results will be reported in a future paper.

IX. ACKNOWLEDGMENT

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