New Series Resonant DC Link Inverter For Electric Vehicle Drives

Y. Murai, H. Ishikawa
Dept. of Electronics & Computer Eng.
Gifu University
1-1 Yanagido, Gifu, Gifu 501-11, Japan
Tel: 582-30-1111, Fax: 582-30-1894

T. A. Lipo
Dept. of Electrical and Computer Eng.
University of Wisconsin - Madison
1415 Johnson Drive, Madison, WI 53706
Tel.: 608-262-0287, Fax: 608-262-1267

Abstract

This paper developed a new series resonant (current resonant) dc link inverter with fixed pulse frequency aimed for electric vehicle drives. The fixed pulse frequency of 20-50 kHz enabled the system to work with no audible noise, and to involve only 1/100 of dc inductance and 1/10 of output capacitors in comparison with conventional series resonant dc link converters. In this paper, explanations of the new circuit configuration, the simulation, and designing consideration are included.

1. Introduction

In these days, electric vehicles (EV) are growing to big business for their pollutionless nature. Usually electric vehicles utilize hard switched PWM inverters with relatively high frequency switching for quiet operations and better performances.[1] The inverters, however, bring about unexpected high frequency electro-magnetic interferences (EMI) which cause the failure of adjacent electronic equipment, and give disturbance to radio communications.

To solve these problems, resonant link converters with soft switching seem to work excellently in reducing high frequency components. The resonant converters are usually classified to a voltage resonant type or a current resonant type[2],[3]. The voltage type has the merit of limited voltage peak, although it has the demerit of using low current devices. While the latter current resonant type has the features dual to the voltage types, it also has the flexibility to control both in motoring and in regeneration modes. The current resonant type, however, has had the demerits of unfixed pulse frequencies [3],[4]. Because of that, the system used to need large dc inductance and large filter capacitors in the output to get better waveform.

This paper provides newly developed series resonant (current resonant) dc link inverter with fixed pulse frequency as shown in Fig. 1. The fixed frequency operation with 20-50 kHz enables the system to use only 1/100 in size of dc inductance, and 1/10 in size of output capacitors. The feature makes it possible for the system to work in no audible frequency noise, as well as feature of low EMI operations.

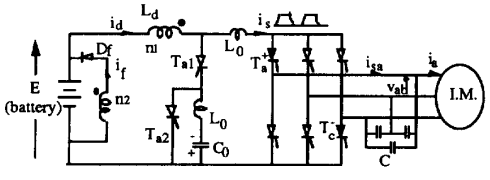


Fig. 1. Proposed Current Resonant DC Link PWM Inverter.

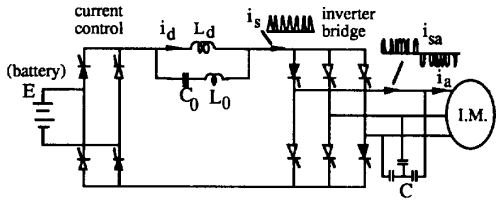


Fig. 2. An example of conventional series resonant inverter.

2. Problems in Conventional Series Resonant Converters

Although the conventional series resonant dc link inverters, as an example shown in Fig. 2, have the merits of soft switching, minimum devices of the system, high current and voltage margins using thyristors, and high power density use, the systems also have the demerits of unfixed pulse frequencies due to the limitation of pulse width control ability. In addition, the system needed the input bridge to adjust the dc current i_d. This bridge deteriorates the merit of high efficiency drive with soft switching feature in comparison with the efficiency of normal PWM inverters.

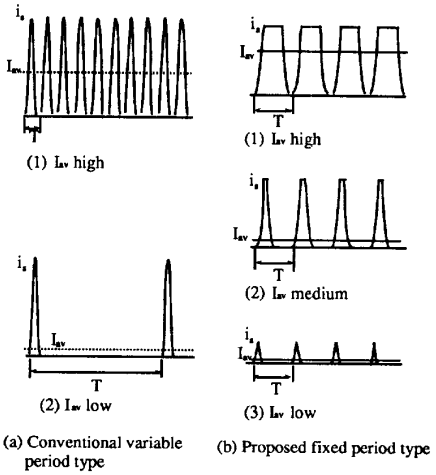


Fig. 3. Comparison of current control.

Fig. 3a shows an example of current pulses produced in the prototype system. In the figure the time period T between pulses

0-7803-1993-1/94 $4.00 © 1994 IEEE

is shown. The pulse frequency (=1/T) of i_s is excellently high when the load current I_{av} is high, and no audible noise is generated if the pulse frequency is beyond audible frequency. In case of reduced load current, however, the pulse train becomes sparse because of the charging delay of capacitor C_0. The delay happens from the shortage of charging current i_d raised from low load current.[3] In the result, audible noise, pulsation of output voltage, instability in controlling output voltage, etc., sometimes happen. In addition to this, the sizes of inductance L_d and C_L had to be increased to suppress these problems.

Fig. 3b illustrates the merit of fixed pulse frequency system with fully adjustable pulse width. The average current I_{AV} can be altered without changing the pulse frequency. The effect of the fixed pulse frequency makes smallest L_d and filter capacitors C possible with no audible noise.

3. Fixed Pulse-Frequency System (proposed)

In the proposed system in Fig. 1, C_0 and two L_0's form a series resonant circuit, and they enable the main thyristors to switch on and off by soft-switched manner. L_d is dc inductance rather large compared with L_0, and it feeds dc current i_s to the inverter bridge. L_d also has a closely coupled auxiliary winding which feeds dc current i_f back to the dc voltage source E (battery) through diode D_f. Output inverter bridge consisting of all thyristors, outputs flat-topped pulses to three-phase load. Capacitors C are the filters to absorb high frequency components involved in three-phase currents.

Fig. 4 explains the behavior of each device. Provided that main thyristors T_a^+ and T_c^- in Fig. 1 are initially in conduction, and that L_d is carrying main current i_s (= i_d), the following sequence start to work repetitively. Mode numbers (1)-(3) correspond to the numbers appearing in Fig. 4.

Mode (1): When auxiliary thyristor T_{a1} is triggered on, dc current i_d starts to flow through L_0 to C_0, reducing i_s, and finally T_a^+ and T_c^- become off.

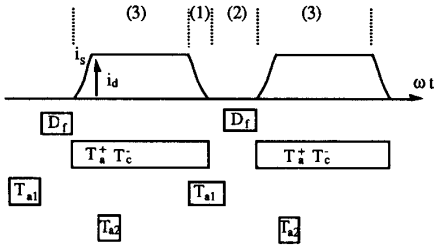


Fig. 4. Firing Period of Devices.

Mode (2): The current i_d continues to charge C_0 up to the direction of up-side positive. After charging up C_0 to a certain level depending on the winding ratio n_1/n_2 between L_d and auxiliary coil, feed-back diode D_f starts to carry i_f, and finally T_{a1} turns off. D_f feeds excessive power back to the voltage source (or battery) E.

Mode (3): Firing T_a^+ and T_c^- again, i_s increases gradually up to the level i_d that is the beginning state of this sequence. As the voltage polarity of the capacitor C_0 has reversed during mode (2), another auxiliary thyristor T_{a2} is turned on to reverse the polarity again back to the original polarity as shown in Fig. 1. T_{a2} turns off after reversing the polarity.

Above sequence produce flat-topped pulses i_s as shown in Fig. 4 or in Fig. 1, and the pulses are distributed to three-phase output-lines.

Starting mode: As neither dc current i_d nor i_f exists at starting the system, auxiliary thyristor T_{a1} is triggered first, then wait for the establish of the capacitor voltage v_{C0}, and then turn on main thyristors such as T_a^+ and T_c^-. After this process the sequence from modes (1) - (3) become ready to begin.

Besides, the operating modes explained above are only major behaviors, and do not include all of the modes appearing in this system, while the modes without explanation do not affect the major sequence.

The width of the pulses in this system is fully adjustable according to the current references, while the pulse frequency remains constant.

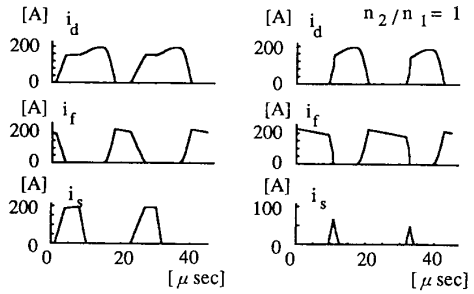


Fig.5 An example of current pulses.

Fig. 5 shows an example of the waveforms of i_d, i_f, and i_s. For example, if the width of i_s pulse becomes narrower, the feed-back period of D_f (= pulse-width of i_f) increases, and the current level of i_d results to decrease. Instead, if a pulse width of i_s becomes wider, the feed-back period of i_f pulses becomes narrower, and the level of i_d results to increase. Accordingly, the adjustment of i_d is automatically performed.

4. System Control

Figure 5 shows the total system configuration. The output currents i_a, i_b, i_c are sensed and directed to a-b-c/d-q transform block where the signals are transformed to synchronously rotating d-q axis components i_d, i_q. The reference currents i_a^*, i_b^*, and i_c^* are also transformed to i_d^* and i_q^* through the same process. The d-q axis currents i_d, i_q are filtered and compared with reference currents i_d^*, i_q^* in the filtering and comparison block, and introduced to proportional and integral (PI) block and transformed again into three phase current errors ε_a, ε_b, ε_c in d-q/a-b-c transform block. These errors are sent to PWM and phase select block. The block decides which thyristor should be fired next and how much the duration time is. The output of the block goes through each base drive circuit of the selected thyristors.

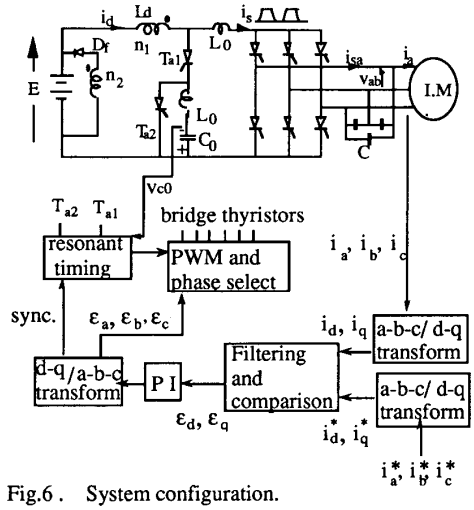


Fig.6 . System configuration.

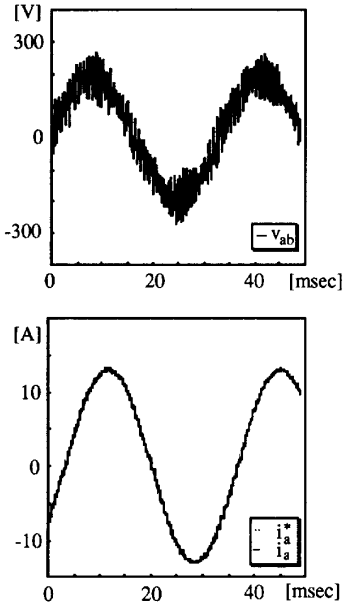
Another signal from d-q/a-b-c transform block to the resonant timing block is the synchronizing timing for the next firing.

The resonant timing block works sequentially to yield the starting and commutating signals of the main phase thyristors, but also the auxiliary signals to reverse the polarity of the capacitor charge by sensing capacitor voltage v_{C0}.

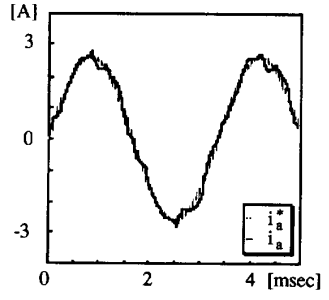
The adjustment of current i_d is fully automatically done depending on the need of the load currents. When the current increase of the output is initiated, the pulse width signal will increase, hence i_d will increase due to the longer duration time of i_S.

The current references i_a^*, i_b^* and i_c^* are usually given by field orientation control to achieve best control of induction motor for each electric vehicle. However, the voltage references v_a^*, v_b^*, v_c^* is also used instead of current references. For that purpose, line voltages v_{ab}, v_{bc}, v_{ca} are sensed instead of currents i_a, i_b, and i_c.

5. Simulated results



(a) f=30Hz



(b) f=300Hz

Fig. 7. Simulated waveforms for 30Hz and 300Hz.

Pulse freq.	50kHz
Ld	100 μH
Co	0.5 μF
Lo	10 μH
C	10 μF
E	400 v

Table 1. Circuit parameters.

Fig. 7a and b show examples of line-line voltages v_{ab} and line currents i_a calculated for f = 300Hz and 30Hz by using the parameters in Table 1. The ratings of the load induction motor are 3 phase, 60Hz, 200v, 3.75kw. The conditions used are slip frequency f_{slip} = 3Hz for figure 6a, and fslip = -3Hz for figure 7b with the voltages of 200v at f = 300Hz and 100v at f = 30 Hz, respectively.

The switching frequency (pulse frequency of is) is set to 50 kHz, the current i_a is well regulated to sinusoids both in 30Hz operation and in 300 Hz. The waveform of line-line voltages v_{ab} is rather peculiar. Because the system is working to confine the current to a limited error region even though the current fed by dc current i_d reaches at a maximum requirement, while other phase also is requesting i_d to adjust the current.

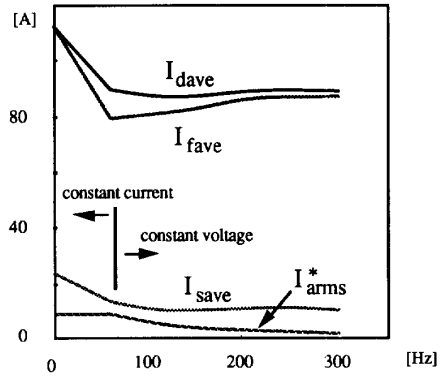


Fig.8 Idave,Ifave,Isave and Ia vs. f.

Fig. 8 shows the average values I_{dave} and I_{fave} of i_d and i_f, respectively, for the variation of output frequency f. The reference of output line-current i_a is also seen as I_{arms}^* in r.m.s. value. The frequency range 0-60Hz is of constant current, and 60 - 300Hz is constant voltage region.

6 Some Designing Considerations

The fundamental designing considerations about main static elements are presented below.

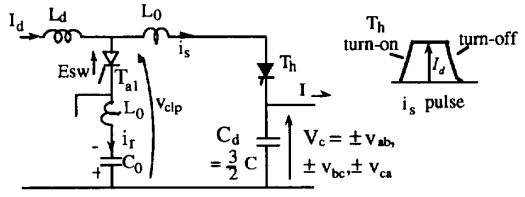


Fig. 9. Simplified equivalent circuit.

i) resonant circuit elements:

In this system, resonating current flows in mode (1) to turn off main thyristors. To estimate the resonant parameters, let us consider the basic equations.

a) mode(1): Fig. 9 shows the simplified equivalent circuit for mode (1). Thyristor T_h is equivalent to two phase-thyristors (e.g., T_a^+, T_c^-) of the inverter bridge in conduction. The voltage V_c is equal to the output line-line voltage across capacitors C in Fig. 1, and V_c is assumed to be constant during the commutating period. When T_{a1} is triggered, the voltage E_{sw} is impressed across the series resonant circuit with $2L_0$ and C_0. Then the equation in this mode becomes,

$$E_{sw} = -2 L_0 \frac{d i_r}{d t} - \frac{1}{C_0}\int_0^t i_r \, dt \qquad (1)$$

$$i_r = \frac{E_{sw}}{Z} \sin \omega_r t \qquad (2)$$

where,

$$E_{SW} = (v_{C0} - v_C)_{initial}$$

$$Z = \sqrt{2 L_0 / C_0}, \ \omega_r = 1 / \sqrt{2 L_0 C_0} \qquad (3)$$

In this equation Id(=I)=constant is assumed.
From eq.(3),

$$\omega_r C_0 Z = 1 \qquad (4)$$

$$i_s = i_d - i_r$$
$$= I_d - \frac{E_{sw}}{Z} \sin \omega_r t \qquad (5)$$

Main current i_s should reach zero with turn-off margins enough to turn off the main devices.

If the margin is assumed to 30% at $\sin \omega_r t = 1$, then,

$$i_s = -0.3 I_d \qquad (6)$$

Then, eq.(5) becomes

$$\frac{E_{sw}}{Z} = 1.3 I_d \qquad (7)$$

For example, ω_r depends on the switching period, and it would be adequate to place 20 μs for one cycle period to obtain 50kHz of pulse frequency. Then, ω_r is

$$\omega_r = \frac{2\pi}{20 \times 10^{-6}}$$
$$= 3.14 \times 10^5 \qquad (8).$$

If the assumption $C_0 = 1\mu F$ is made, then $Z = 1.0\Omega$ and $L_0 = 5\ \mu H$ are obtained.

If the system requires $I_d = 300A$, eq. (7) leads to

$$E_{sw} = 1.3 I_d Z$$
$$= 1.3 \times 300 \times 1.0 = 400v \qquad (9)$$

V_{C0} should have the peak voltage to ensure

$$E_{sw} > 1.3 I_d Z. \qquad (10)$$

b) mode(3)

The turn on period of main thyristors starts from the condition that the voltage Vclp in Fig. 9 is clamped to a certain voltage due to feed-back diode D_f in conduction. The main current i_s starts up linearly with the gradient of Vclp / L_0 until the dc inductance L_d restores I_d from feed-back coil.

c) initial starting period

The very initial starting period of the system, both I_d and i_f are zero, the current I_d must be introduced to establish the voltage v_{C0} across capacitor C_0 to an adequate level to turn-off the main thyristors in the mode (1) in Fig. 9. For this mode, charging up of C_0 is done through L_d, by the motive force of battery voltage E. Solving series L_d - C_0 circuit similar to eq.(1), the charging current i_i becomes,

$$i_i = \frac{E}{Z_i} \sin \omega_{ri} t \qquad (11)$$

where, $Z_i = \sqrt{L_d / C_0}$, $\omega_{ri} = 1 / \sqrt{L_d C_0}$

As the resonant frequency of ω_{ri} is usually low, the rising rate of i_i is approximately E / Z_i.

ii) L_d and C_d:

The purpose of L_d is mainly to clamp current i_s constant during the duration time. The existence of large inductance L_d, however, slows the system response down, especially in the starting mode, or sudden change of the load.

Accordingly, the inductance L_d is set to as small value as to maintain the current variation of I_d to specified allowance, e.g., 10-20% of allowable fluctuation during the pulse interval T. If the maximum voltage across L_d is assumed to 2E the current rise ΔI_d is roughly estimated to

$$\Delta I_d = 2E T / L_d \qquad (12).$$

If the fluctuation is assumed to κI_d, then putting $\Delta I_d = \kappa I_d$ in eq. (12), L_d is estimated as,

$$L_d = 2E T / \kappa I_d \qquad (13).$$

The output filter capacitor C (= 2/3 C_d) is also determined by considering the output voltage fluctuations to confine in an allowable limitations, even if the current fed is interrupted due to other phase requirement. The period may differ according to the cases, but the most likely design will be done by assuming the period is one pulse period T. For this case, the charge across the capacitor C_d equals to the flow-out charges to the load, and the next rough estimation become possible.

$$\sigma C_d V_{rat} = I_{rat} T \qquad (14)$$

where, σ is the allowance factor of output voltage fluctuation, and V_{rat} and I_{rat} are the rated output rms voltage and current, respectively.

Accordingly, estimated C_d becomes,

$$C_d = I_{rat} T / \sigma V_{rat} \qquad (15)$$

Assuming the required current I_d for i_a is three times of output current I_{rat},

$$I_d = 3 I_{rat} \qquad (16)$$

an example of designing the parameters can be achieved.

If the actual system is supposed to have E = 400v, T = 20 μs (pulse frequency f_c = 50 kHz), I_{rat} = 100Arms, κ = 0.3, L_d becomes

$$L_d = 2 \times 400 \times 20 \times 10^{-6} / 0.3 \times 300 = 178\ \mu H \quad (17).$$

In addition, if the allowance σ is provided as 0.2 at rated voltage $V_{rat} = 200v$, C_d and C are given as

$$C_d = 100 \times 20 \times 10^{-6} / 0.2 \times 200 = 50\ \mu F$$

$$C = \frac{2 C_d}{3} = 33.3 \mu F \quad (18)$$

7. Conclusion

In this paper, a basic circuit for electric vehicle drives with soft switched resonant dc link was proposed. The main features of this system are,

(i) low EMI with soft switching,
(ii) low acoustic noise by high frequency switching,
(iii) no electrolytic capacitor with high frequency switching,
(iv) excellent operation even in very low frequency output,
(v) smooth regenerative operation with automatic input current regulation, and that
(vi) constant pulse frequency makes the dc inductance L_d and filter capacitor C extremely small (approximate values become about 1/100 of L_d, 1/10 of C in comparison with the prototype system [3]).

In addition, this system eliminated the current i_d control which was essential in the proto-type series resonant converters.

Electric vehicles are one of the mandatory issues in the future, and this system would be expected as the powerful motive force for that purpose.

References

[1] M. J. Riezenman, "ELECTRIC VEHICLES," IEEE Spectrum, pp.18-24, pp.93-101, Nov./1992.
[2] J. He and N. Mohan, "Parallel Resonant DC Link Circuit - A Novel Zero Switching Loss Topology with Minimum Voltage Stresses," IEEE Trans. Power Electronics, vol. 6, no. 4, pp. 687-694, Oct. 1991.
[3] Y. Murai, T. A. Lipo: "High Frequency Series Resonant DC Link Power Conversion," IEEE IAS Annual Meeting Conf. Rec., pp. 772-779, 1988.
[4] H. Nakamura, Y. Murai, and T. A. Lipo, "Quasi Current Resonant DC Link AC/AC Converter," PESC'93 Conference Record, pp.279-283, 1993.