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Utility Interface Issues For Line Connected PWM Voltage Source Converters: A Comparative Study

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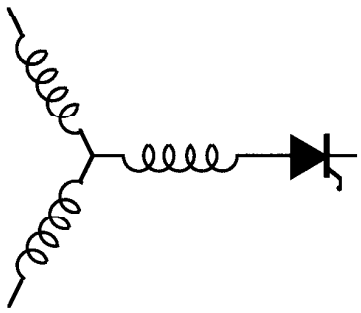

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Abstract - **This paper examines the interface issues which occur when pulse width modulated (PWM) Voltage Source Converters (VSCs) are connected to the utility. In particular, it investigates the line current Total Harmonic Distortion (THD) characteristics of various Current Regulated PWM (CRPWM) techniques with constraints on the converter average switching frequency (converter efficiency) and passive filter size (filter cost). Various CRPWM methods with proper filter and controller structures have been studied and evaluated by means of computer simulations for the utility interface with a variable speed wind turbine generating system.[1] Dynamic performance has been evaluated as well as the steady state light load, full load, leading, lagging and unity power factor operating conditions.**

1. INTRODUCTION

As a result of the continuous innovations in the power electronics and electric drives fields, applications of power electronic systems directly connected to the power grid have been significantly increasing. Increasing number of modern adjustable speed drives and other high power electrical or electromechanical energy conversion devices are presently interfaced with the three phase utility through Voltage Source Converters (VSCs) which utilize the modern switching devices such as the GTO and IGBT.

When utilized as controlled rectifiers, these VSCs can provide significantly improved converter output current waveform due to their wide switching device bandwidth. Hence, reduced converter output current Total Harmonic distortion (THD) and significantly reduced passive filter size can be achieved compared to the thyristor bridge rectifier. The line current THD limits which have been recently regulated by IEEE 519-1992 standards in order to eliminate the severe line harmonic pollution problem can readily be met by VSC based systems [1,2,10].

In addition to their high THD performance, the VSCs have improved DC bus voltage utilization, four quadrant power flow capability, and can improve the system reliability during transients if controlled properly. Their four quadrant fully controllable power flow capability make the VSCs the best choice for utility interfacing systems which have variable speed or variable voltage generation capability. Such systems are variable speed wind turbines, photovoltaic cells, etc.

Figure 1 shows the typical high performance configuration which utilizes a VSC for interfacing the load/source with the utility. Since the VSC and VSI are de coupled from each other by a sufficiently large DC bus capacitor, either side can be independently controlled except for the constraint of capacitor voltage regulation. The VSI, on the left side of the DC bus, may be connected to an induction motor/generator which can employ high performance control algorithms such as a field orientation controller in order to extract the best system performance. Interfacing the DC bus with the utility, the VSC, on the right side, modulates the DC bus voltage to achieve a high utility current wave form quality, and steer the power in the desired direction. This study mainly concerns the issues regarding the utility interface, and attention will not be paid to the left side of the system except for the need for DC bus capacitor voltage regulation.

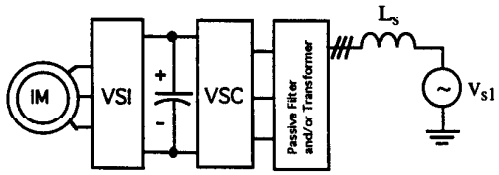

Fig. 1 A typical high performance utility interface configuration

Although the utility interfaced VSCs can utilize the PWM principles that are successfully employed in electric motor drives, the utility interface requirements differ from those for drives significantly. In utility interface applications, current regulated PWM methods are preferred to voltage PWM applications due to the high dynamic performance requirements. The constant output frequency requirement and access to the line voltage simplify the utility interface control algorithm. However, the THD requirements remain significant and they must be carefully examined when evaluating the conventional PWM methods for utility interface.

For a given average switching frequency constraint, (converter efficiency) the THD of the current injected to the utility is a function of the current regulation algorithm, and filter type and size. For systems with power ratings above tens of kilowatts and in particular above hundred kilowatt level, high converter and filter efficiency, low filter cost, and low THD requirement criteria are vital. This study addresses the above issues for such systems. Various high performance current regulated PWM algorithms with suitable filter structures have been considered for the utility interface system. As a case study, the utility interface of a 250 kVA variable speed wind turbine generation system has been evaluated. System time domain simulations and when possible analytical methods have been utilized to study and compare the various candidate

[1]Material discussed in this paper is covered by U.S. and foreign patents.

configurations. Various operating conditions such as unity power factor, leading and lagging power factor cases, full load, light load cases, steady state dynamic behavior etc. have been all investigated in detail in order to reach a complete conclusion.

2. CRPWM ALGORITHMS

The utility interface requires high steady state and dynamic performance CRPWM regulators with robust and simple to implement control algorithms.

Among the various well known CRPWM algorithms, are the delta current regulator for its simplicity and robustness, the Stationary Frame Ramp Comparison (SFRC) current regulator, known for its simplicity and good THD characteristics, the Stationary Equivalent Synchronous Frame Ramp Comparison (SESFRC) current regulator [3,4] for its high performance and good THD, and the Table Based Predictive Method (TBPM) [5] for its good overall performance. All of these current regulation schemes are candidates for this application.

A. Delta Current Regulator

Shown in Fig. 2, the delta current regulator has an extremely simple and robust structure, and excellent dynamic performance. The switching frequency is bounded by the sampling frequency. However, the steady state performance of the regulator is very poor. The harmonic content is large. The wide harmonic spectrum includes frequencies from the subsynchronous range to the sampling frequency range. The regulator can not effectively utilize the converter zero states and requires high sampling frequency, hence high average switching frequency.

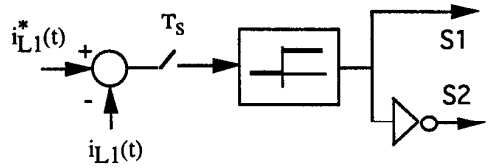

Fig. 2 Per phase delta current regulator structure

B. Stationary Frame Ramp Comparison Regulator

Shown in Fig. 3, the Stationary Frame Ramp Comparison (SFRC) current regulator has a simple structure and provides well defined harmonic spectrum. Because it operates on AC signals, the regulator has nonzero steady state error, and as long as the controller gain is not changed in the proper direction, the phase and magnitude error of the regulator degrades the performance as the operating point is varied.

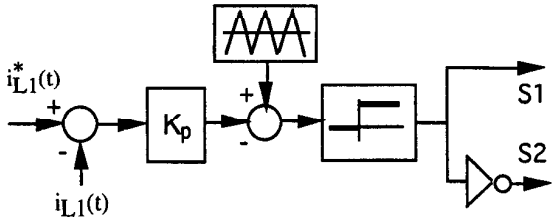

Fig. 3 Per phase SFRC current regulator structure

C. SESFRC Current Regulator

The SESFRC current regulator [3,4,9] overcomes the weakness of the above stationary frame regulator because it is equivalent to the synchronous frame regulator which has zero steady state error characteristics. As shown in Fig. 4, the regulator has a relatively simple structure and has implementation advantages over the synchronous frame regulator. The d-q reference voltage outputs of the regulator are converted to ABC variables and then compared with the triangular wave form as in the SFRC regulator case to extract the switch gate signals. The dominant harmonics of this regulator are the triangular wave carrier frequency side bands, and no significant low order harmonics are present. In this regulator the potential for failure under heavy dynamic operating conditions (the integrator may saturate) can be eliminated at the expense of increasing controller complexity [9].

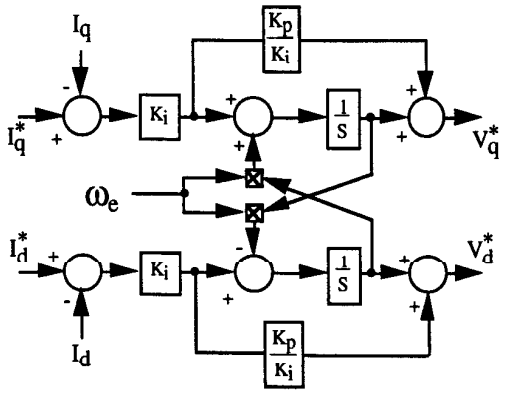

Fig. 4 The SESFRC curent regulator structure

D. Table Based Predictive Method Current Regulator

TBPM is a look-up table based current regulation method [5]. The steady state look-up table is a 6 x 6 integer table that takes in information concerning the rough location of the reference voltage vector and the current error vector, and outputs the next optimal inverter state. The reference voltage vector calculation requires the knowledge of the AC source/emf voltage which is easily accessible in the case of a utility interface. The zones for the reference voltage and current error vectors are shown in Fig. 6. Careful study shows that for each current error vector sector and voltage reference vector sector, there is only one inverter state that slowly reduces the error and provides only one switching at a time during steady state. Based on the given zone definitions, the look-up table is extracted as in Table I. It becomes obvious from this table that this regulator is an adjacent state regulator.

The angular information of the current error and reference voltage vectors are on-line calculated and whenever the current error exceeds the preset boundaries the angle information is converted to the zone information regarding the zone of operation. The table is then looked up and finally the optimal state is commanded to the inverter switches.

TBPM provides as good performance as the on-line predictive method proposed by Holtz[6], and due to its significantly simpler structure and significantly reduced computational requirements it is more attractive. Hence,

the space vector method of Ref. 6 is not examined in detail in this paper.

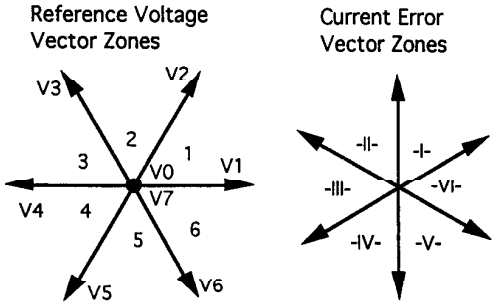

Fig. 5 TBPM reference voltage and current error zones

Table I TBPM steady state look-up table

Region of Veq \ Region of Current Error Vector	I	II	III	IV	V	VI
1	2	2	0,7	0,7	1	1
2	2	3	3	0,7	0,7	2
3	3	3	4	4	0,7	0,7
4	0,7	4	4	5	5	0,7
5	0,7	0,7	5	5	6	6
6	1	0,7	0,7	6	6	1

Performance of TBPM and the on-line optimal predictive method regulators have been compared by means of a computer simulation. An ideal VSI model has been simulated with 750 V DC bus voltage, 480 V, 60 Hz. line voltage with a 750 μH series inductance. Table II demonstrates the performance of the two regulators for 50 A RMS and unity power factor reference with 20 A error vector radius. The table shows that for the same average switching frequency the current THD of the two are practically equal. This result should not be surprising, because both methods fundamentally utilize the same switching pattern, namely the adjacent state voltage vector method in which voltage states are selected so that either the successive voltage vectors selected in Fig. 5 never differ by more than one or the zero vector is chosen.

Table II Comparisons between TBPM and the method by Holtz

	THD (%)	I(A) rms	Fsw(kHz)
TBPM	19.57	50.62	2.151
Holtz	19.42	50.54	2.144

3. FILTER REQUIREMENTS AND ACTIVE DAMPING

When interfacing a VSC with the utility, a shunt capacitive filter is required in order to suppress the high frequency harmonics generated by high frequency switching of the VSC. If the harmonics have a large component at the resonant frequency of the filter capacitance and line inductance, then large line current wave form oscillations can result due to resonance. Under such conditions, an active damping (derivative feedback method) [7,8] and/or a passive damping (passive resistor) mechanism can be utilized to improve the wave form quality.

It has been determined that the ramp comparison based regulators do not have significant low order harmonics so that choosing a small filter with a resonant frequency lower than the carrier frequency suffices. The TBPM and the delta regulator, do generate low order harmonics over a relatively wide frequency band which inevitably includes the filter resonant frequency. Therefore, these regulators require active and/or passive damping in order to achieve a good THD with small filter size.

As will be shown later, the results of this study suggest that an active damping method which simply utilizes the line current derivative as a feedback to the VSC reference currents is a very effective control method. Because the algorithm does not increase the converter average switching frequency noticeably, it therefore eliminates the need for bulky resistive components and their attendant losses. Therefore, series inductive and shunt capacitive AC filters with moderate size along with an active damping scheme are sufficient to meet the required THD limit. The capacitive filter design must be made at the light load operating point, because the THD appears to be the worst at this operating point. However, the RMS current rating of the capacitive filter must designed for the full load operating point.

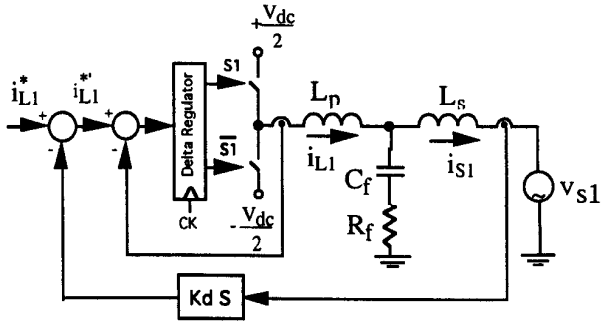

Fig. 6 Single phase actively damped, delta current regulator controlled system configuration.

The effectiveness of the active damping effect of the line current derivative feedback can be shown through simple analysis utilizing the single phase model of the system as shown in Fig. 6. The line current can be written as a function of the utility voltage and VSC output current in the La place domain in the following form;

$$I_s = \frac{1}{L_s C_f S^2 + C_f R_f S + 1}[(C_f R_f S + 1)I_L - C_f S V_s] \qquad (1)$$

The system resonant frequency and the system open loop damping are defined as follows;

$$\omega_o = \frac{1}{\sqrt{L_s C_f}} \qquad (2) \qquad \xi = \frac{C_f}{2 L_s \omega_o} \qquad (3)$$

Because the system is current regulated, the VSC and its series filter inductance can be modeled as a current source

with a finite gain while the harmonics can be assumed to be generated by the regulator as a disturbance;

$$I_L = K_a I_L^* + I_n = K_a(I_L^* - K_d S I_s) + I_n \quad (4)$$

Substituting (4) in (1) and re-arranging, the actively damped system equation can be found;

$$I_s = \frac{[K_a(\frac{R_f}{L_s}S + \frac{1}{L_s C_f})(I_L + I_n) - \frac{SV_s}{L_s}]}{(1 + K_a K_d \frac{R_f}{L_s})S^2 + (\frac{R_f}{L_s} + \frac{K_a K_d}{L_s C_f})S + \frac{1}{L_s C_f}} \quad (5)$$

The system damping with zero passive resistance is;

$$\xi' = \frac{K_a K_d \omega_o}{2} \quad (6)$$

Equation 5 clearly indicates that provided that the current regulator has a switching frequency capability that is several times higher than the system resonant frequency, the utility current wave form oscillations, and the low order harmonics can be significantly damped. However, the derivative gain reduces the converter gain for the fundamental component. Therefore it can not be made very large. The fundamental component magnitude and angle error caused by the derivative feedback can be corrected utilizing Eq. (5). The effect of the derivative feedback on the fundamental component can be eliminated by synchronous frame transformations at the expense of increasing the controller complexity.

In practice the derivative feedback loop is not very sensitive to the line inductance value and can function reasonably well within the normal range of inductance variations. The delta regulator based system with active damping requires a passive resistive filter in addition to the active damping feedback, because the delta regulator has a natural delay of one regulator sampling cycle. This delay affects the active damping feedback signal, hence the active damping feedback loop can, in this case, only partially function.

4. SYSTEM SIMULATION MODEL AND POWER FLOW CONTROL ALGORITHM

In order to compare the performance of the various candidate configurations an extensive computer simulation study has been conducted. As an example application, the utility interface for a variable frequency wind turbine generation system with 250 kVA, 480V, 300A, 60 Hz ratings has been considered. At this power rating, a 4 kHz converter average switching frequency was considered as acceptable. A 500 μH inductance per phase was connected in series with the VSC output. The system was interfaced with a 21 kV utility through a step up transformer. The equivalent line inductance at the low voltage side was approximately 250 μH per phase. The low voltage end of the transformer was rated at 480 V. The Short Circuit Ratio (SCR) of the utility at the common coupling point was assumed to be less than 20. Hence, according to the IEEE 519 standards the THD requirement is 5 % or less. The wind turbine generator is a field orientation controlled induction machine driven through a PWM VSI. The VSI and VSC were decoupled through a 27 mF DC bus capacitor.

When studying the utility interface issues, the portion of the system from the DC bus capacitor to the wind turbine can be modeled as a DC current source that charges/discharges the DC bus capacitor. The DC bus capacitor is sufficiently large to provide full decoupling of both sides. Hence, the system equivalent circuit diagram as shown in Fig. 7 results. The simulation model assumes ideal switching devices with no dead time delays. This assumption can be justified because the state of the art devices in this power rating have a dead time less than 10μs which is very small compared to a switching cycle.

As previously discussed, the filter structure adopted is an R-L-C type filter as shown in the figure and the resistive component value is set to zero except for the delta regulator. The line current derivatives are fed back to the current regulator as well as the measured current values. The derivative gain was set to zero except for the delta and TBPM regulator cases.

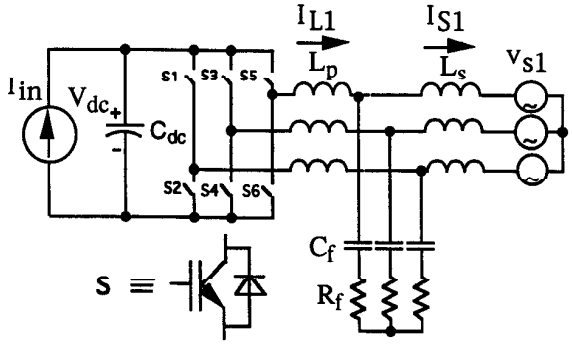

Fig. 7 System simulation model

The DC bus capacitor model of the above system requires that the energy input in to the capacitor be transferred to the output. A power flow algorithm was implemented to achieve this goal. As shown in Fig. 8, a Proportional plus Integral (PI) type regulator which operates on the DC bus voltage error generates the magnitude of the phase current reference component at the utility side which is in phase with the utility voltage. The desired reactive current, i.e. the current reference component of the utility which is orthogonal to the utility voltage, was operated on together with the in phase reference current component to extract the utility side reference current. By adjusting the reactive current reference, the system can be operated with constant VARs or with constant power factor. Due to the existence of the passive shunt filter and active damping feedback loop, the VSC current references are different from the utility side reference currents. A simple fundamental frequency phasor circuit analysis was utilized to calculate the VSC reference currents.

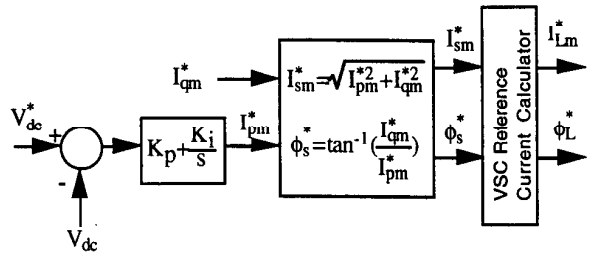

Fig. 8 System power flow control diagram.

5. FILTER SIZE OPTIMIZATION

The simulation study first involves the filter size determination for the candidate configurations. The filter parameters have been optimized for the light load operating condition (50 A RMS), which has the worst case THD. The filter parameters have been varied and the improvement directions noted for each simulation based on the smallest filter size, 5 % THD, and 4 kHz average switching frequency requirement criteria. The SESFRC CRPWM simulation assumes a 50 μF capacitor per phase and the SFRC regulator assumes a 100 μF capacitor. Both ramp comparison regulators assume a 4 kHz triangular carrier frequency. The delta regulator assumes a 25 kHz sampling frequency and uses a 500 μF capacitor. The table based predictive method assumes a 20 A vector hysteresis current error radius and 250 μF capacitors per phase. The inductive filter connected to the VSC output has a 500 μH value which was determined by the 4 kHz switching frequency limit of the power converter.

6. SYSTEM SIMULATION RESULTS

The simulation results for various steady state operating conditions are summarized for the four candidate configurations in Table III through Table VI. In the tables the current reference components which are in phase, and 90 degrees out of phase with the line voltage are termed Ip and Iq relatively. The power factor, the line current RMS value, the line current THD for the first 100 harmonics, the average switching frequency, and the filter resistive losses, when they exist, are recorded in the tables. Since in all the systems the individual low frequency harmonics (n<25) were substantially smaller than the specified IEEE-519 standard recommendations, ,the harmonic spectrum and the individual harmonic information was not considered in the evaluation.

The results summarized in Table III through Table VI suggest that the SESFRC scheme has the best overall THD and average switching frequency characteristics. With the exception of the converter saturation case which led the controller integrator to failure, the SESFRC system performs better than the other configurations at all the operating conditions. The regulator failure condition appears in Table III with 131% THD under a 200 A lagging current command.

As demonstrated in Table IV, the SFRCCR system performs well near unity power factor operating point. However under lagging PF operating conditions a very large THD and under leading PF a high switching frequency results. This is due to the steady state phase and

Table III SESFRC Simulation Data
(Cf=50μF/phase, Fc=4 kHz)

Ip(A) rms	Iq(A) rms	P. F.	Is (A)rms	THD (%)	Fsw (kHz)
50.0	0.0	1.0	51.11	4.04	2.98
50.0	50.0	0.707	78.52	4.24	2.88
50.0	-50.0	-0.707	63.75	2.6	3.2
50.0	200.0	0.24	322.0	131.5	0.4
50.0	200.0	-0.24	196.04	0.64	3.47
100.0	0.0	1.0	100.55	1.96	2.9
300.0	0.0	1.0	300.17	0.79	2.86

magnitude error of this regulator. Therefore, this configuration appears to be only suitable for systems which operate near unity power factor.

Table IV SFRCCR Simulation Data
(Cf=100μF/phase, Fc=4 kHz)

Ip(A) rms	Iq(A) rms	P. F.	Is (A)rms	THD (%)	Fsw (kHz)
50.0	0.0	1.0	50.57	5.97	3.09
50.0	50.0	0.707	75.56	8.61	2.63
50.0	-50.0	-0.707	65.86	1.2	3.87
50.0	200.0	0.24	205.94	15.32	1.07
50.0	-200.0	-0.24	199.28	0.3	3.88
100.0	0.0	1.0	101.04	3.56	3.01
300.0	0.0	1.0	303.47	1.77	2.39

Although it has slightly higher THD and larger average switching frequency than the SESFRC, the TBPM method is the only configuration that can compete with the SESFRC configuration. As Table V indicates, TBPM with active damping loop provides good THD and average switching frequency characteristics that do not vary significantly as the operating point changes. The switching frequency and THD values are within acceptable range, hence this configuration is attractive for the type of applications that the SESFRC configuration is not suitable due to the lagging current case failure. The delta regulator with active damping loop has poor THD at light and medium load levels for all the operating points. The resistive filter losses are large and not acceptable. These poor steady state operating characteristics of the delta regulator are the reason that this configuration is not feasible.

Table V TBPM Simulation Data
(Cf=250μF/phase, Δi=20A)

Ip(A) rms	Iq(A) rms	P. F.	Is (A)rms	THD (%)	Fsw (kHz)
50.0	0.0	1.0	49.77	6.08	3.61
50.0	50.0	0.707	71.59	6.18	3.38
50.0	-50.0	-0.707	70.98	2.88	3.74
50.0	200.0	0.24	188.92	10.91	2.85
50.0	-200.0	-024	206.74	1.37	4.1
100.0	0.0	1.0	100.06	2.75	3.68
300.0	0.0	1.0	299.29	1.16	3.5

All the configurations have the tendency to increase the switching frequency and reduce the THD as the inductive reactive power demand of the utility decreases. The degree of variation is the least with the SESFRC and the most with the SFRCCR. In order to make the average

Table VI Delta Regulated System Simulation Data
(Cf=500μF/phase, Rf=0.1 ohm/phase , Fsamp=25 kHz)

Ip(A)rms	Iq(A) rms	P. F.	Is (A)rms	THD(%)	Fsw(kHz)	Loss(W)
50.0	0.0	1.0	49.15	7.91	4.13	858.0
50.0	50.0	0.707	66.1	3.97	3.81	879.0
50.0	-50.0	-0.707	71.48	4.9	4.45	842.0
50.0	200.0	0.24	186.99	8.06	2.61	948.0
50.0	-200.0	-0.24	210.1	0.91	5.52	792.0
100.0	0.0	1.0	98.1	4.04	4.1	865.0
300.0	0.0	1.0	298.83	1.44	3.69	877.0

switching frequency independent from the power factor and magnitude of the reactive current, the magnitude of the triangle in the ramp comparison regulators and the radius of the error limit circle in TBPM must be varied. However, this increases the controller complexity significantly.

The dynamic behavior of all the configurations was then tested under a unity power factor operating condition. The system was first operated at light load (50 A RMS) for 30 ms. Then, the power input to the DC capacitor was linearly increased in 10 ms to full load value (300A RMS) and the tracking capability of the regulators was recorded. The simulation waveforms which demonstrate this dynamic behavior as well as the unity power factor light and full load operating conditions are shown for all the four candidate configurations in Fig. 9 through Fig. 13. The average switching frequency was calculated by counting the Total Number of Switching (TNSW) of all the converter switches and then averaging.

As shown in Fig. 9, the SESFRC current regulator based system has good tracking performance, and good DC bus voltage regulation capability in addition to the very low utility current THD and low average switching frequency. The initial waveform discrepancy is due to the zero initial inductor current assumption in the simulation. The slope of the total number of switching curve which estimates the average switching frequency does not change noticeably as the operating condition changes.

In Fig. 10 the SFRCCR based system simulations show that the DC bus regulation is poorer than the SESFRCCR case. The waveform distortion at light load is noticeable from the figure. However the waveform quality is still good for this operating condition.

Light load (50 A) unity power factor operating condition line side and converter output currents for the TBPM based system are shown in Fig. 11. The active damping feedback loop is not activated until t=30 ms. The active damping loop as shown in the figure improves the line side current waveform significantly. The line current THD is decreased from 33% to 6% by a very large margin. The inclusion of the active damping loop does not increase the converter average switching frequency noticeably. This can be clearly seen from the total number of switching curve which does not have a noticeable slope change.

The TBPM based system simulations including the tracking performance and full load operating conditions is shown in Fig. 12. As the waveforms indicate, the DC bus regulation is tight, and the line current waveform quality is good, particularly with the inclusion of active damping feedback loop. The output power waveform oscillations before the active damping loop is activated are due to the very low system damping.

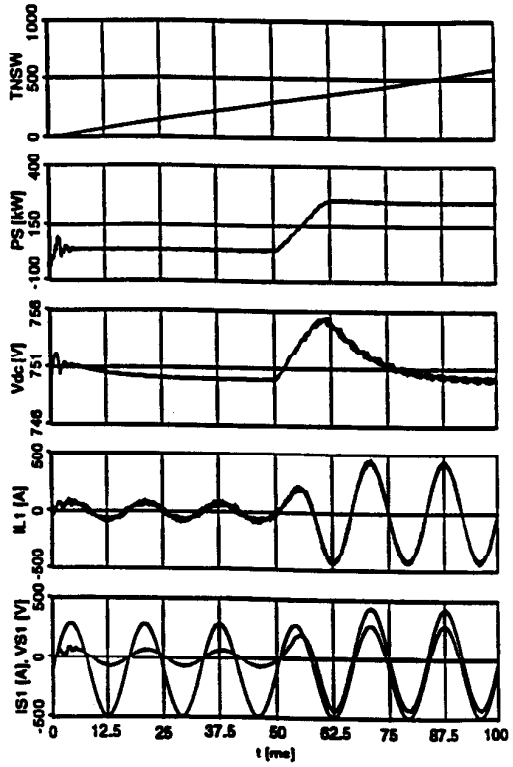

Fig. 9 SESFRCCR system simulation wave forms. Traces from the bottom to the top: line voltage and current, converter current, DC bus voltage, output power, and total number of switchings.

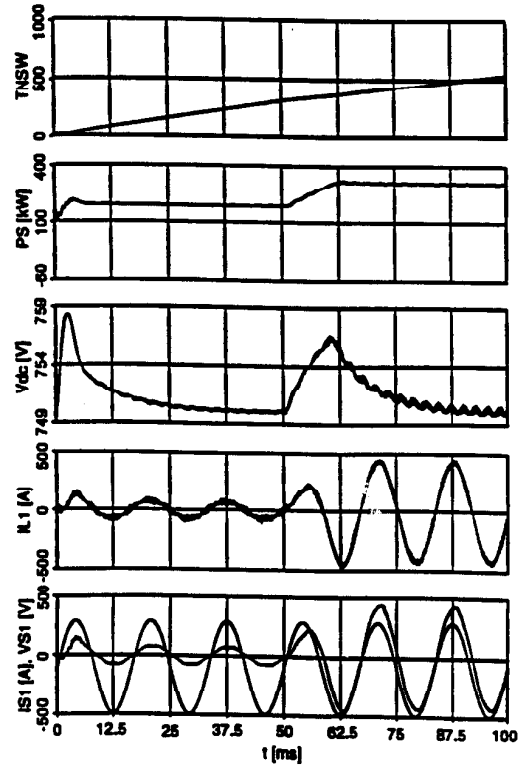

Fig. 10 SFRCCR system simulation wave forms. Traces from the bottom to the top: line voltage and current, converter current, DC bus voltage, output power, and total number of switchings.

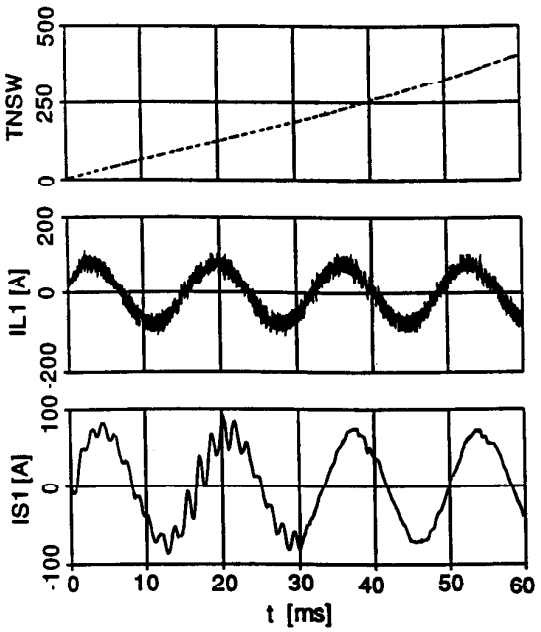

Fig. 11 TBPM system light load simulation waveforms. Traces from the bottom to the top: line current, converter current, and total number of switching. At t=30 ms the active damping feedback loop is activated.

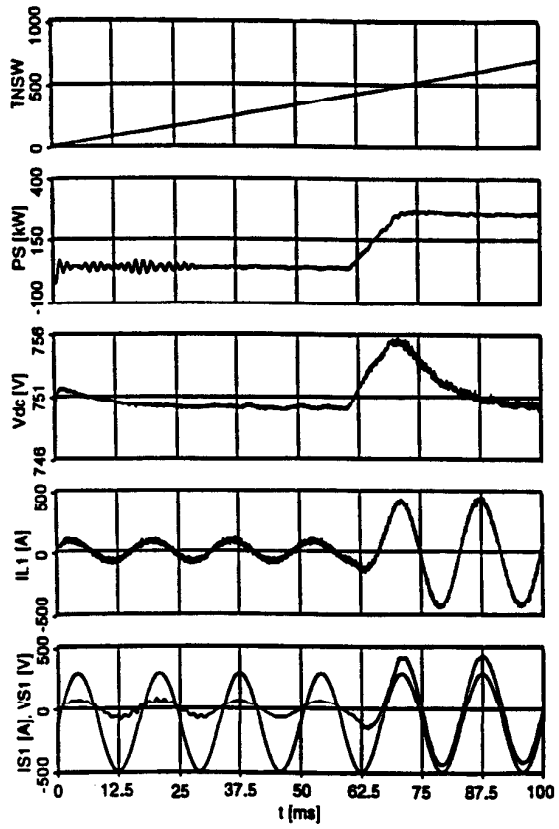

Fig. 12 TBPM simulation waveforms. Traces from the bottom to the top: utility voltage and current, converter current, DC bus voltage, output power, and total number of switchings.

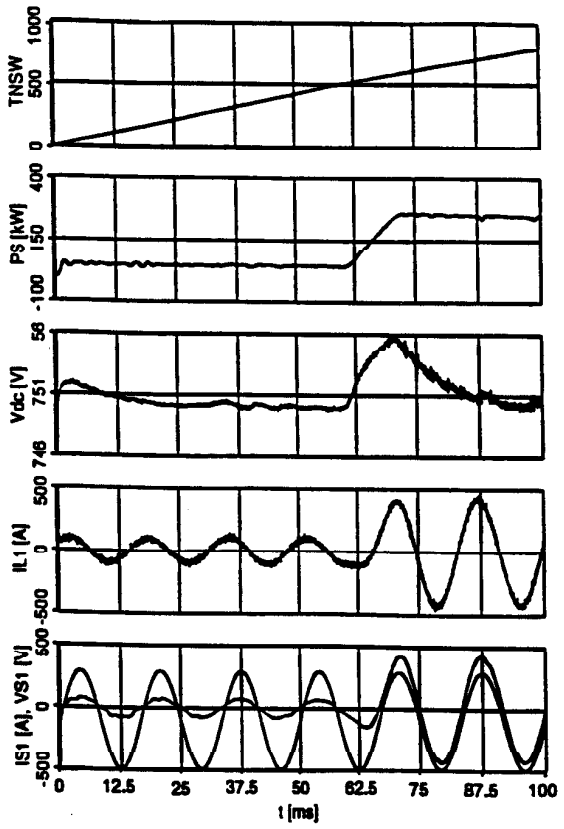

Fig. 13 Delta CR system simulation waveforms. Traces from the bottom to the top: line voltage and current, converter current, DC bus voltage, output power, and total number of switchings.

Shown in Fig. 13, delta regulator based system wave forms are reasonably good except for the light load operating region. However, the total number of switchings is significantly higher than the other candidate systems. The good tracking performance is clearly at the expense of reduced waveform quality not to mention the resistive filter losses. Also notice that the active damping loop (activated at t=30ms) improves the line current waveform as in the TBPM case. However, the combination of both active and passive damping is still insufficient to provide good filtering.

7. COMPARISONS

The overall merits of the four candidate schemes for the utility interfacing a VSC to a 250 kVA wind energy generation system are summarized in Table VII. The results of this research suggest that for a given average switching frequency value and filter size (and type), the THD is mainly dependent on the current regulation algorithm. Intelligent switching algorithms which provide a symmetric switching pattern (ramp comparison type) and the on-line optimal predictive methods (table based predictive method) which provide the best utilization of zero states in order to reduce the output current harmonic content have better characteristics than the delta type current regulator.

The filter size and type is very dependent on the current regulation method utilized. The filter can be smaller and simpler if the current regulator has a well defined harmonic content (ramp comparison type) or if it can switch in an intelligent manner that avoids creating harmonics at the system resonant frequency (active damping). Through detailed simulations, it has been shown that only a shunt capacitive filter is sufficient and a resistive damping component is not required for the ramp comparison regulators and the table based predictive method regulator with active damping. The ramp comparison current regulation algorithms require smaller filter capacitor size than the table predictive method with active damping. Hence, from the filter size minimization perspective, the SESFRC system is the most desirable candidate, because it requires a very small capacitive filter (50 μF/phase). The SFRCCR requires a smaller capacitor size than TBPM (100 μF/phase vs. 250 μF/phase). However, filter size minimization is not the only important criteria since equally important are the steady state and dynamic performance criteria.

Table VII Comparative evaluation of the candidate configurations for the utility interface of a wind energy generation system.

	SESFCR	SFRCCR	TBPM with Active Damp.	Delta with Active Damp.
THD	excellent	Operating Point Dependent	good	bad
Filter Size	small	moderate	large	very large
Filter Losses	zero	zero	zero	In order of kilowatts
Average Switching Frequency	< 4kHz	< 4kHz	< 4kHz	> 4 kHz
Dynamic Performance	moderate	moderate	excellent	excellent
Impementation Complexity	moderate	simple	moderate	very simple

The average switching frequency comparison is clearly in favor of SESFRCCR system and high efficiency systems should employ such a switching algorithm.

Implementation complexity is approximately equivalent in both SESFRC and TBPM configurations, and both are not very complex. There is no calculation burden in either case, and TBPM can be implemented with a simple microprocessor, or DSP, while the SESFRC method can be implemented by either hardware or software. The delta regulator and stationary frame ramp comparison regulators are extremely simple as well as inexpensive.

8. CONCLUSIONS

In this paper a detailed comparative study of four different high performance CRPWM configurations for utility interface of a 250 kVA VSC has been reported. The steady state and dynamic operating characteristics of each configuration has been studied for the optimized filter and controller parameters, through detailed simulations for various operating conditions. All the configurations were evaluated and compared under high efficiency, low cost, and good THD criteria.

The study suggests that SESFRC is the best candidate due to its small filter size, very good THD, low average switching frequency, and good tracking capability. For systems which mostly operate near unity power factor and at a fixed operating point, the SFRC regulator configuration can be preferred due to its simple structure, small filter size, and satisfactory performance.

If the dynamic behavior characteristics of the SESFRC regulator are prohibitive, then the TBPM based system which has larger filter size, but only slightly higher THD and slightly higher average switching frequency, may be preferred since the dynamic performance of the table based predictive method is excellent. The delta regulator performance has been found to be very poor and not feasible for the given average switching frequency constraint. The filter size requirement is very small due to the high converter bandwidth. The line current active damping feedback loop is very effective for damping the filter oscillations both in the TBPM, and delta regulator based configurations. In particular under a light load operating condition, this method provides significant line current harmonic reduction.

While experimental results have not been included in this paper for reasons of space allotment, an experimental study has been performed and results substantiate the conclusions reported in the paper.

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