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Fault Protection in a Multilevel Inverter Implementation of a Static Condenser

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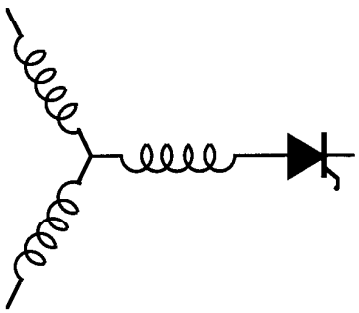

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Fault protection in a multilevel inverter implementation of a static condenser

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***Abstract*- Multilevel inverters are well suited for static condenser implementation in utility systems. With multilevel inverters, it is possible to realize low distortion voltage waveforms and keep losses low using suitable switching schemes. The complex topology of these inverters coupled with the large number of devices used increases the probability of device failure in a statcon. In this paper, the fault modes of a multilevel inverter are investigated with special emphasis on the five level inverter. The main focus of the paper is on device failure and the corresponding impact on the operating conditions and resulting stresses. The presence of redundant states offers the possibility of continuing operation with inferior bus and device utilization following a fault. Failure of some devices is more critical than the failure of others, thereby emphasizing the need for adding redundant devices.**

Nomenclature

Statcon	Static condenser
Vars	Volt-amperes reactive
R,S,T	Phases
RG1..RG8	GTO/force commutated switch in phase R
AD1..AD8	Antiparallel diodes
RCD1..RCD6	Clamp diodes in phase R
δ	delay angle
α_1, α_2	commutation angles
I_r, I_s, I_t	Line currents
E_{ro}, E_{so}, E_{to}	Inverter pole voltages w.r.t. DC bus midpoint
$V_{rs}, V_{st},$	AC system line voltages
X_l	Line reactance
C_1, C_2, C_3, C_4	DC bus capacitances
Q_{sys}	Reactive power flowing into AC system
V	Magnitude of AC system phase voltage
E	Inverter phase voltage fundamental magnitude.
V_{dc}	Voltage across each DC bus capacitor
X	Don't care switching state
THD	Total harmonic distortion

I. INTRODUCTION

In a utility system, var compensation is used for voltage support at critical loads. A static condenser is a shunt var compensator which provides reactive power without large reactive components [1]. Static condensers can be based on the current sourced converter, the hybrid current sourced system and the voltage source converter. In this paper, only the voltage source converter implementation is considered. Fig. 1 shows the one line schematic diagram of a static condenser linked to an AC system via a transformer. The system voltage and the fundamental inverter voltage can be represented as

$$V_{sys} = Ve^{j0} \quad ; V_{inv} - Ee^{j\delta}. \qquad ...(1)$$

The real and reactive powers delivered by the AC system is given by

$$P = \frac{V^2}{X_l}\left[\frac{E}{V}\sin\delta\right] \quad ; Q = \frac{V}{X_l}[V - E] \qquad ...(2)$$

The value of delay angle δ is usually low because the system has to supply only the inverter and linking reactor losses. When E > V, the static condenser is seen to provide capacitive vars to the system.

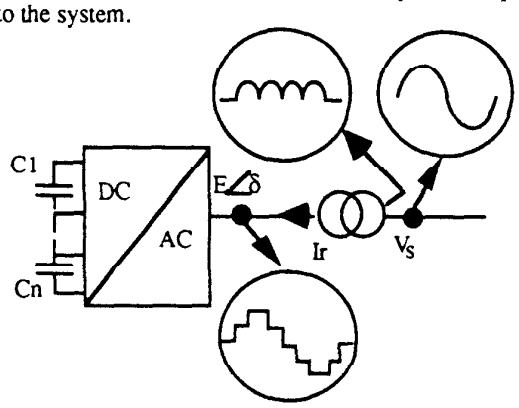


Fig. 1 Voltage source inverter based static condenser

The voltage sourced converter in a static condenser can be realized by a multilevel inverter which are based on the neutral point clamped inverter topology first proposed by Nabae et al [2]. Two distinct topologies have been proposed to realize an N level inverter for a static condenser application i.e. the diode clamped multilevel inverter (DCMLI) and the flying capacitor multilevel inverter (FCMLI). The relative merits of the topologies are discussed in [3] and attention is restricted to the diode clamped topology in this paper. A 5 level diode clamped inverter is shown in Fig. 2.

In an N level inverter, fundamental voltage control is achieved by delay angle δ, so that the (N-1)/2 degrees of freedom can be used for harmonic elimination. A typical pole voltage waveform developed by a 5 level inverter is shown in Fig . 3. The firing angles α are perturbed for voltage balancing on the DC bus [3]. In a 5 level DCMLI at most 4 contiguous switches are gated at any instant. For example, referring to Fig.

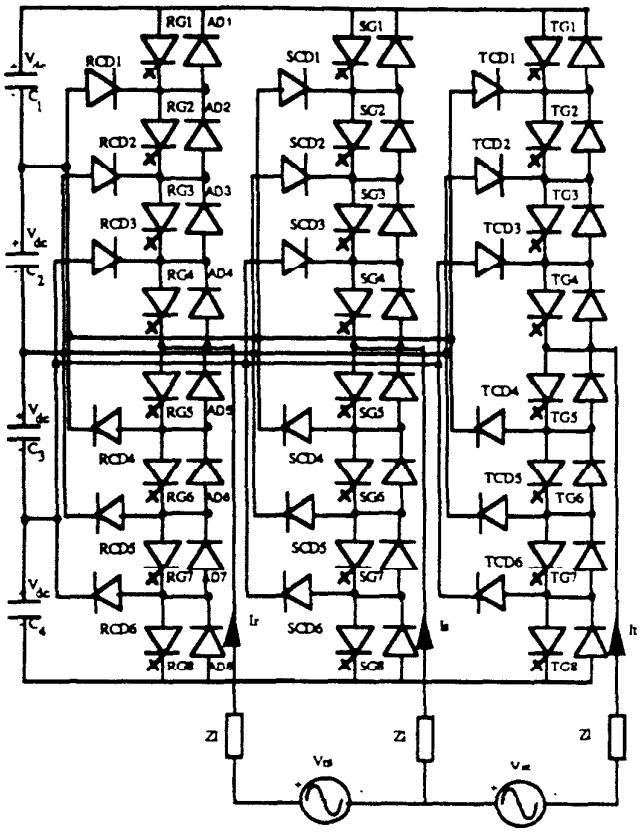


Fig. 2 A 5 level diode clamped inverter

3, in the interval $\alpha_1 < \omega t < \alpha_2$, GTOs RG3 through RG7 are gated on while RG1, RG2, RG7, and RG8 are gated off.

The advantages of a multilevel inverter over a conventional 6/12 pulse converter can be summarized as

(i) Low distortion voltages due to larger number of levels
(ii) Higher voltage levels can be achieved using available devices.
(iii) Lower losses in transformers, snubbers and gate drives
(iv) Reduced filter requirements.
(v) Robust voltage sharing across devices since each device's voltage is clamped by capacitors.
(vi) Reduced problems for dynamic voltage sharing
(vii) Possibility of eliminating transformer used for interfacing with AC system.

The last advantages offers a significant cost benefit in a utility system. However, the inverter topology and corresponding control schemes are more complex. The added device count contributes significantly to the increase in failure probability. Capacitor voltage balancing becomes an operational requirement which further complicates the control.

A 3 phase N level DCMLI has N^3 switching states. Therefore, a 5 level inverter has 125 switching states which can be represented as in the form (R=r, S=s, T=t) where r,s,t = -2,-1,0,1,2. (R=r, S=s, T=t) corresponds to the pole voltage (with respect to DC bus midpoint) $E_{r0} = rV_{dc}$, $E_{s0} = sV_{dc}$, $E_{t0} = tV_{dc}$. The number of redundant states in this instance is 64, so there

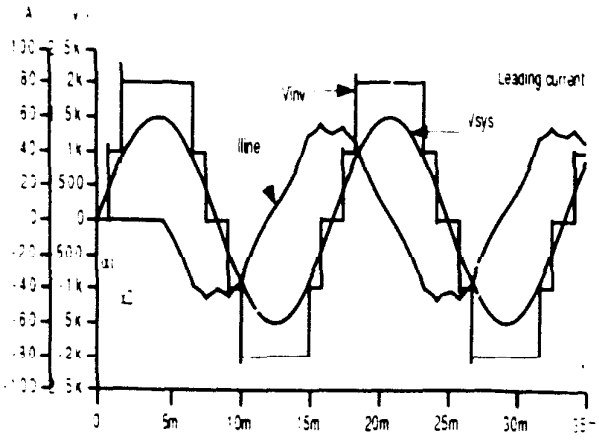


Fig. 3 Pole voltage in a 5 level inverter.

are only 61 distinct voltage vectors. Fig. 4 shows the dq plane representation of the switching states. By suitably selecting the switching states in order to generate a voltage vector, it is possible to balance the capacitor voltages and generate low distortion voltage waveforms.

In this paper, protection issues involved in the multilevel inverter implementation are discussed. The large number of devices used and the relatively complex topology as well as the utility setting of the application requires a careful description of the contingencies and protection measures since there is a cost penalty associated with a failure leading to a shutdown.

II. FAULT EVENTS

Of all the possible contingencies that the inverter has to be protected against, four have been identified for further discussion viz.

(i) Device failure
(ii) Inrush current and startup stresses
(iii) Disturbance in AC system
(iv) Severe DC bus unbalance

Of these, device failure and AC side faults are random events. A device or valve could fail short or open. The other two events are extreme operating conditions which could lead to a system failure. The primary protection in these cases should be effected through a suitable control scheme. In case of device failure, the primary system protection has to be built into the inverter design. The chief fault sensor in any 'event' is either a sustained overcurrent through or overvoltage across a device and DC capacitor overcurrent.

In the DCMLI topology, certain devices such as RCD3 (Fig. 2) are inherently subject to greater voltage stresses as compared to other devices viz. AD1. In addition, significant mismatches between device characteristics can lead to misoperations and cause outright failure of some devices. In the normal mode of operation, the power flow between the statcon and the AC system is essentially reactive. Under unbalanced conditions, there can be a real power flow between

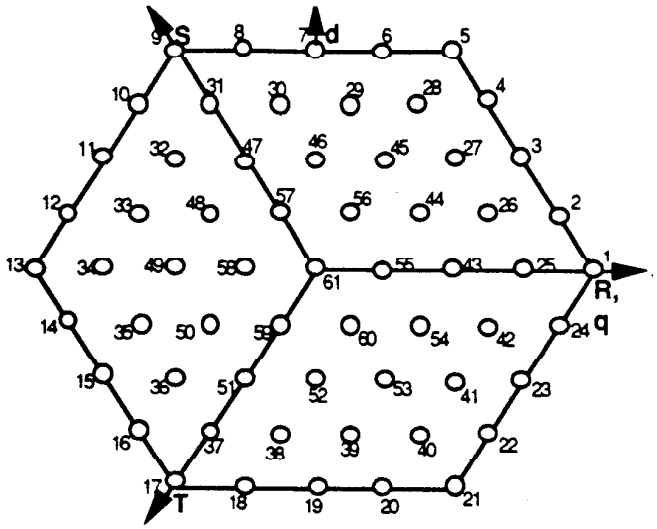


Fig. 4 Voltage vectors in a 5 level inverter

the statcon and the AC system. The devices have to be rated so as to handle the increased power flow.

There is a twofold objective to the protection function:

(i) To protect the inverter devices and components in any contingency. To achieve this goal, device stresses following a fault need to be anticipated and

(ii) To restore the greatest degree of normality to the inverter operation following an event. This provides the motivation for studying the impact of a fault on the normal operation of the inverter.

The following discussion relates to a 5 level inverter but most results can be extended other number of levels. GTOs are assumed to be used as the forced commutation devices. The GTO with its snubber is assumed to be as shown in Fig. 5.

III. DEVICE FAILURE

Device failure is the primary contingency from which the inverter has to be protected. The large number of devices used in the multilevel inverter increases the probability of a device failure event. Device misoperation event can be classified as

(i) Device short circuit (ii) Device open circuit

Both these conditions can arise due to a variety of reasons such as

(i) Failure of the gate drives

(ii) Excessive voltage and current stresses on the device.

(iii) Response to another fault event.

The effect of device misoperation is described in the subsequent sections.

(A) Device short circuit

The most common fault event of a device failure event is a device failing short. In a multilevel inverter, the impact of the short circuit of any device depends on the relative location of the device failing.

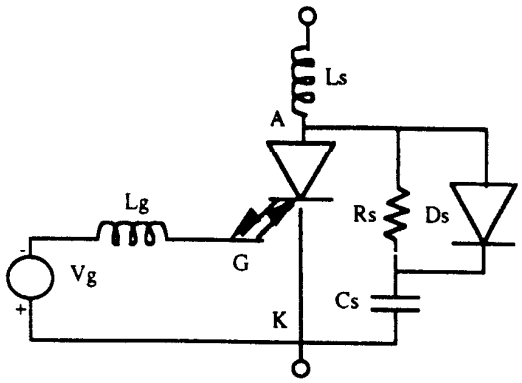


Fig. 5 GTO snubber circuit

First, short circuit of a switch is considered. Consider the short circuit of GTO RG1 in phase R,- the inverter phase leg then appears as in Fig. 6 and when RG2-RG5 are gated there exists a capacitor discharge path as shown . To avert this discharge, it is necessary to ensure that RG2 - RG5 are never 'on' simultaneously. Fig. 7 shows the pole voltages in this case.

When GTO RG2 fails short, there is a capacitor discharge path when RG3-RG7 are gated and hence the latter sequence of switches have to remain gated off. When RG3 fails short, it can be similarly seen that RG4-RG7 cannot be simultaneously on else C_3 discharges. When RG4 fails short, RG5-RG8 have to gated off else, C_4 discharges. Therefore, for each GTO short circuit, there is a corresponding capacitor which discharges when the usual switching scheme is continued.

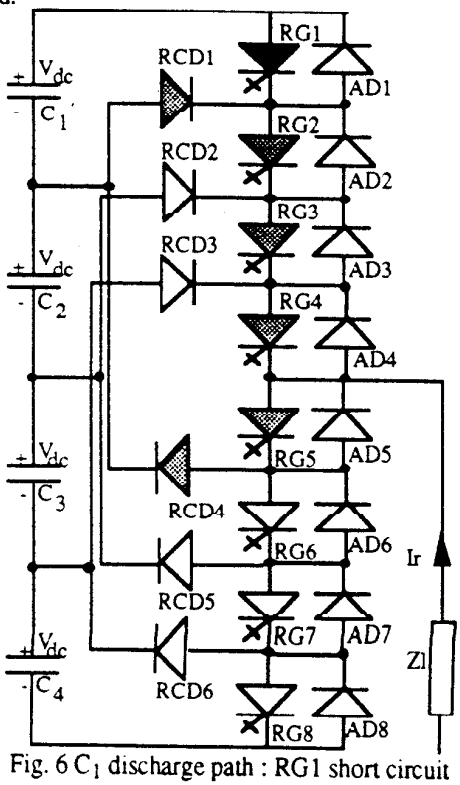


Fig. 6 C_1 discharge path : RG1 short circuit

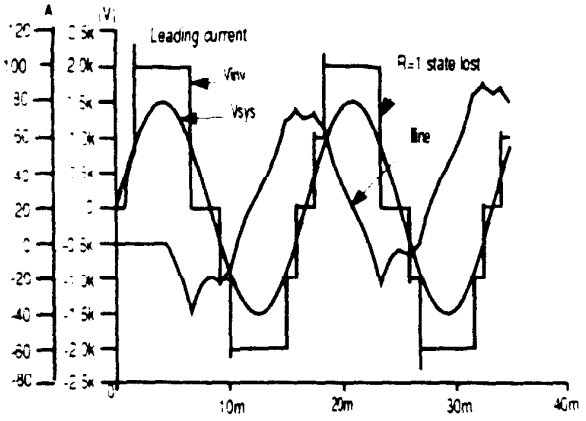


Fig. 7 Inverter, system voltages, line current: RG1 short circuit

When RCD1 fails short, it can be seen that RG1 must remain off, else C1 discharges. When RCD2 fails short, RG1 and RG2 cannot remain on simultaneously else C_1 and C_2 collectively discharge. Also, RG3-RG6 cannot be gated on together else C_2 discharges. Finally when RCD3 fails short, the following switch combinations cannot be gated on simultaneously : (i) RG1-RG3 else C_1,C_2,C_3 discharge , (ii) RG2-RG3 to prevent C_2 discharge. The impact of short circuits on the devices in the lower half of the phase legs is complementary to that discussed above. The most important issues relating to device short circuits are

(i) Fault sensing
(ii) Resulting voltage stresses
(iii) Impact on continued inverter operation

(A. i) Fault sensing

Sensing a device short circuit is of critical importance in preventing a cascade failure. Each short circuit event must be detected in an unambiguous manner so that timely action can be taken to prevent fault propagation. In case of device short circuits, by measuring the voltage across each device and current through the DC bus capacitors, a unique set of conditions can be identified with each device short circuit depending on the switching state of the inverter at the instant of the fault.

If the inverter state is (2,X,X), i.e. RG1-RG4 are conducting, RG1 short circuit cannot be detected till the inverter moves to the state (1,X,X) i.e. when RG5 is gated on. At the turn-on event of RG5, there is an overcurrent through capacitor C_1. Similarly, if RG1 fails short when RG2-RG5 are conducting, only a C_1 overcurrent detects the short circuit of RG1. When RG3-RG6 are conducting, RG1 short circuit causes a voltage = $2V_{dc}$ to appear across RG2. Similarly, if RG1 fails short when RG4-RG7 are conducting, a voltage = $1.5V_{dc}$ appears across RG2 and RG3 each. When RG5-RG8 conduct, a voltage = $1.33V_{dc}$ appears across RG2, RG3 and RG4 each. To prevent a C_1 discharge, when the inverter state is (1,X,X) we need to ensure that RG2 remains gated off whenever RG1 short circuit is detected. In a similar manner, the short circuits at other devices can be detected. Table 1 summarizes the strategy for detecting the short circuit of each device.

The voltage stresses were verified by Saber simulations and Figs. 7 shows the inverter and voltage and line current when RG1 is short circuited and RG2 is gated off to prevent capacitor discharge. Also, as is evident from Figs. 8 and 9, the device stresses are substantially higher than the nominal values whenever there is a short circuit for both leading and lagging currents respectively.

(A. ii) Resulting voltage stresses

Following the short circuit of certain device, there is an increase in the voltage stress of the remaining devices. For example, when RG1 fails short, RG2 and AD2 have to hold off a voltage = $2V_{dc}$ when inverter switching state is (0,X,X). If the inverter switching state is (-1,X,X) and assuming that voltage divides equally between valves in series, a voltage = $1.5V_{dc}$ appears across RG2 and RG3. When RG2 fails short, RG3 and AD3 have to hold off a voltage = $2V_{dc}$ when the inverter switching state is (-1,X,X). Proceeding in a likewise manner, the peak voltage stresses across each device can be worked out for all devices. These results are also summarized in Table 1.

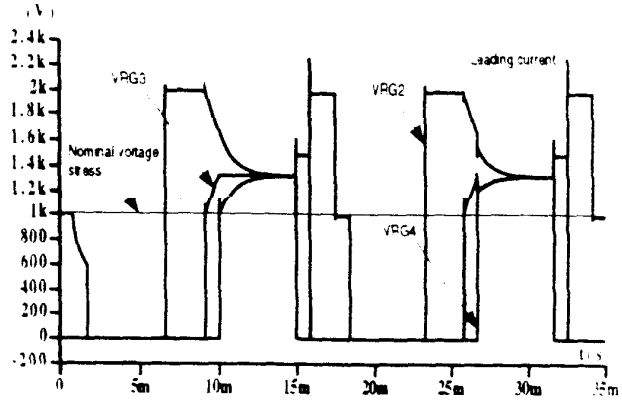


Fig. 8 Voltage across RG2, RG3, RG4 : RG1 short circuit

There is no fault related stress at any device when a clamp diode is short circuited and the corresponding protection measure employed as per Table 1. These stresses are in addition to the transient overvoltages which may result due to the parasitic inductances in the circuit. As an illustration, consider RG1 short circuit when RG2-RG5 are conducting. In this case, capacitor C_1 tries to discharge through RG1-RG5. This produces a large di/dt which in turn causes a large reverse voltage to appear across the switches leading to device breakdown. One solution to prevent device breakdown due to overvoltage stresses is to add redundant devices in series but this can lead to an increase in the cost.

(A. iii) Impact on inverter operation

Following a device short circuit, it is evident that some switching states cannot be realized. The number of lost

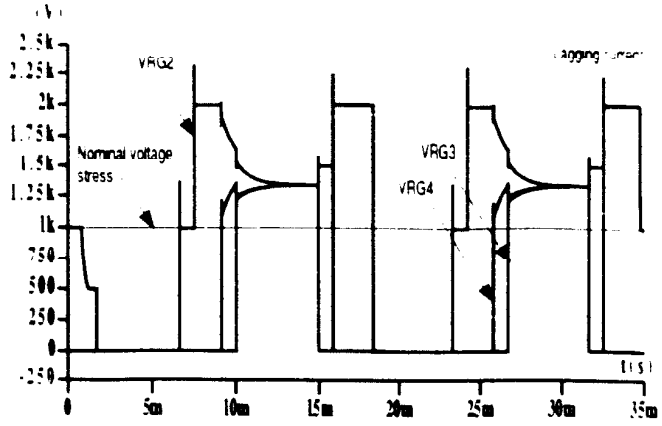


Fig. 9 Device stresses : RG1 short circuit; Lagging current

switching states and voltage vectors lost depends on the device failing short. In case of GTO RG1 failing short, 25 switching states out of 125. The distribution of the lost switching states in the dq plane as shown in Fig. 10. Thus the effect RG1 short circuit on generated voltage THD is mitigated though loss of 25 switching states makes the voltage balancing on the capacitors more difficult to accomplish. In Fig. 10, it can be seen that the darkly circled nodes represent the voltage vectors completely

Device SC	Inverter state	Sensor	Protecuon
RG1	R=2	$V_{RG1}=0$	-
	R=1	$V_{RG1}=0$, I_{C1} overcurrent	RG2=off
	R=0	$V_{RG2}=2V_{dc}$	RG2=off
	R=-1	$V_{RG2}=V_{RG3}=1.5V_{dc}$	RG2=off
	R=-2	$V_{RG2}=V_{RG3}=V_{RG4}=1.33V_{dc}$	-
RG2	R=2	-	-
	R=1	-	-
	R=0	$V_{RG2}=0$, I_{C2} overcurrent	RG3=off
	R=-1	$V_{RG3}=2V_{dc}$	RG3=off
	R=-2	$V_{RG3}=V_{RG4}=1.5V_{dc}$	RG3=off
RG3	R=2	-	-
	R=1	-	
	R=0	-	
	R=-1	I_{C3} overcurrent	RG4 = off
	R=-2	$V_{RG4}=2V_{dc}$	RG4=off
RG4	R=2	-	-
	R=1	-	-
	R=0	-	-
	R=-1	-	-
	R=-2	I_{C4} overcurrent	RG8 = off
RCD1	R=2	I_{c1} overcurrent	RG1 = off
	R=1	-	-
	R=0	-	RG1 = off
	R=-1	-	RG1 = off
	R=-2	-	RG1=off
RCD2	R=2	I_{C1}, I_{C2} overcurrent	RG3=off
	R=1	I_{C2} overcurrent	RG3=off
	R=0	-	-
	R=-1	-	-
	R=-2	-	-
RCD3	R=2	I_{C1}, I_{C2}, I_{C3} overcurrent	RG3 , RG1 = off
	R=1	I_{C2}, I_{C1} overcurrent	Rg2, RG3 = off
	R=0	I_{C3} overcurrent	RG3 = off
	R=-1	-	-
	R=-2	-	-

Table 1 Short circuit detecuon and protecuon

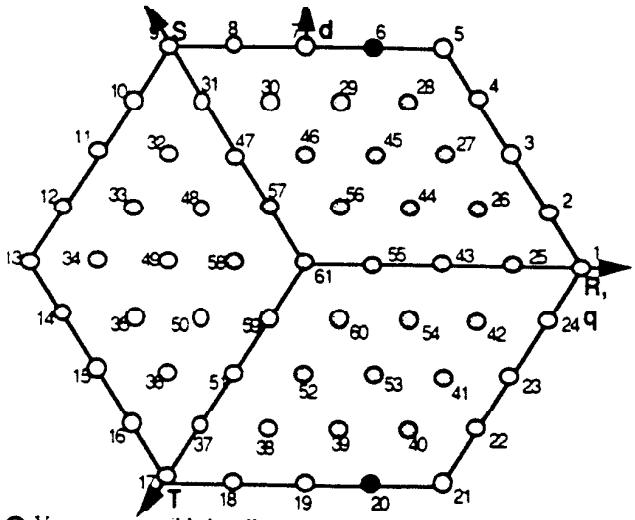
Device SC	Peak device stresses
RG1	VRG2=2Vdc,VRG3=1.5Vdc,VRG4=1.33 Vdc
RG2	VRG3 = 2Vdc, VRG4=1.5Vdc
RG3	VRG4 = 2Vdc
RG4	-
RCD1	-
RCD2	-
RCD3	-

Table 2 Steady state stresses following a short circuit

lost whereas the partially shaded nodes represent vectors which cannot be realized by at least one switching state. These vectors are however accessible because of the redundant states. For example, vector 25 is accessible though switching state (1,-2,-2) is lost because (2,-1,-1) is still available. But when switching state (1,2,-2) is lost, there are no redundant states to realize vector 6. The distribution of the lost switching states indicates that when RG1 fails short, all switching states of the type (1,X,X) are lost.

When RG2 fails short, all switching states of the form (0,X,X) are lost. Therefore, again 25 switching states are lost although only two voltage vectors are lost. The switching states lost are concentrated in the center of the dq hexagon which is rich in redundant states as seen in Fig. 11. When RG3 fails short, switching states of the form (-1,X,X) are lost. Again 25 switching states and 2 voltage vectors are lost although the relative locations of the lost switching states is displaced towards the negative q or R axis When RG4 fails short, switching states of the form (-2,X,X) are lost. Again, only two vectors # 9 and #17 are lost (Fig. 13).

When RG5 fails short, the switching states lost are of the form (2,X,X) and the distribution of the lost switching states is obtained by taking the mirror image about the d-axis of the distribution of switching states lost when RG4 fails short.



○ Vectors accessible by all constituent switching states
● Vectors not accessible by any constituent switching state
○ Vectors not accessible by at least 1 constituent switching state

Fig. 10 RG1 short circuit

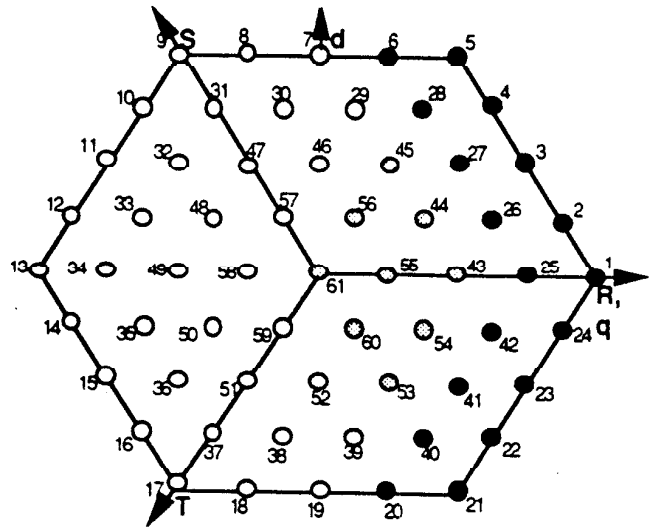


Fig. 15 RCD2 short circuit

Device SC	No. of lost states	Lost Switching states	No. of lost vectors
RG1	25	(1,X,X)	2
RG2	25	(0,X,X)	2
RG3	25	(-1,X,X)	2
RG4	25	(-2,X,X)	2
RCD1	25	(2,X,X)	9
RCD2	50	(2,X,X), (1,X,X)	18
RCD3	25	(-2,X,X)	9

Table 3 : Lost switching states due to device short circuit

(B). Open circuit event

Open circuit misoperation refers to the event where a switch fails to turn on due to gate drive failure.. Open circuit of diode could be representative of the situation when there is a delay in the turn-on of the diode (which may be replaced by a thyristor having zero nominal delay), or a fuse blowout resulting from a transient overcurrent. In this case, a turn-on

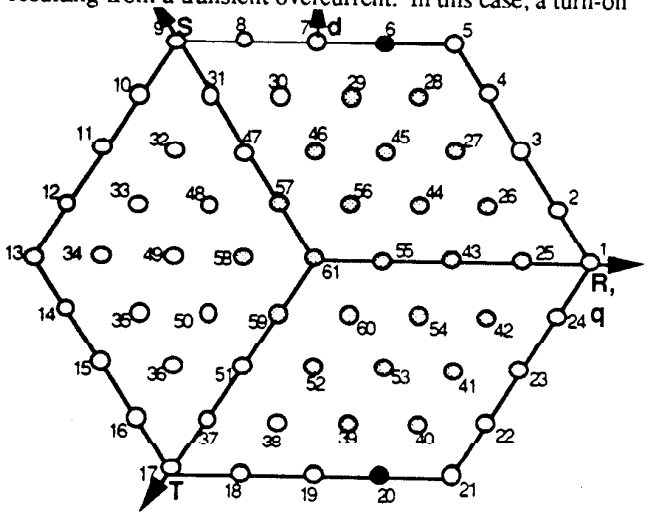


Fig. 16 RCD3 short circuit

Device Open	Inverter states lost	Sensor	Protection
RG1	R=2 ;I_r<0	V_{RCD1}=0; $I_{RCD1} = I_R$	RG5=on
RG2	R=2,1;I_r< 0	V_{RCD2}=0, $I_{RCD2} = I_R$	RG6=on
RG3	R=2,1,0;I_r<0	V_{RCD3}=0; $I_{RCD3} = I_R$	RG7=on
RG4	R=2,1,0,-1; I_r<0	V_{RCD4}=-3V_{DC}; V_{RCD5}=-2V_{DC}; V_{RCD6}=-V_{DC}	RG8=on
RCD1	R=1; I_r<0	V_{RCD1}=0; I_{RCD2}=I_R	RG6=on
RCD2	R=0; I_r<0	V_{RCD3}=0; $I_{RCD2} = I_R$	RG5, RG6=on
RCD3	R=-1; I_r<0	V_{RCD4}=-3V_{DC}; V_{RCD5}=-2V_{DC}; V_{RCD6}=-V_{DC}	RG5 RG8=on
AD1	R=2; I_r>0	V_{RG1} << -V_{DC}	RG5=on
AD2	R=2; I_r>0	V_{RG1}, V_{RG2} << -V_{DC}	RG5=on
AD3	R=2; I_r>0	V_{RG1},V_{RG2},V_{RG3} << -V_{dc}	RG5=on
AD4	R=2; I_r>0	V_{RG1},V_{RG2},V_{RG3},V_{RG4}<< -V_{dc}	RG5=on

Table 4 : Open circuit misoperation event

delay of a diode would be strictly classified as a transient event. As an illustration consider the case when RG1 has a delayed turn on (RG5 - RG8 are 'off'). So long as the line current is negative, RCD1 is forward biased and carries the line current. If the load current is positive, antiparallel diode AD1 carries the load current. There are no additional voltage stresses caused by the open circuit event at RG1. All switching states of the form (2,X,X) are lost when $I_r < 0$. When RG2 fails open, all states (1,X,X) and (2,X,X) are lost when the load current is positive. Similarly, when RG3 fails open, states of the form (2,X,X), (1,X,X) and (0,X,X) are lost. RG4 failing short causes a loss of all states except those of the form (-2,X,X). When RCD1 or RCD5 fail open (1,X,X) states are lost when load current is negative or positive respectively. When RCD2 or RCD5 fail open, (0,X,X) states are lost depending on the polarity of the load current. (-1,X,X) states are lost when RCD3 or RCD6 fail open.

Device Open	No. of switching states lost	Switching states lost	No. of voltage vectors lost	Voltage vectors lost
RG1	25 (I_r < 0)	(2,X,X)	9	1-5, 21-24
RG2	50 (I_r < 0)	(2,X,X), (1,X,X)	18	1-6, 20-24, 25-28, 40-42
RG3	75 (I_r < 0)	(2,X,X), (1,X,X), (0,X,X)	27	1-7,19-29, 39-45, 53,54
RG4	100 (I_r <0)	(2,X,X), (1,X,X), (0,X,X), (-1,X,X)	36	1-8, 18-24, 25-30, 38-46, 52-56, 60
RCD1	25 (I_r < 0)	(1,X,X)	2	6,20
RCD2	25 (I_r < 0)	(0,X,X)	2	7,19
RCD3	25 (I_r < 0)	(-1,X,X)	2	8, 18
AD1	25 (I_r > 0)	(2,X,X)	9	1-5,21-24
AD2	25 (I_r > 0)	(2,X,X)	9	1-5, 21-24
AD3	25 (I_r > 0)	(2,X,X)	9	1-5, 21-24
AD4	25 (I_r > 0)	(2,X,X)	9	1-5, 21-24

Table 5 : Loss of switching states : open circuit misoperation

There is an equivalence between open circuit misoperation of a device in the upper half of a phase leg and the short circuit of its complementary device in the lower half of the phase leg. For example, open circuit at RG1 causes the loss of the same switching states that the short circuit at RG5 produces. Hence, effects of open circuit misoperation can be summarized in Table 4. The number and distribution of

switching states lost due to open circuit misoperation is summarized in Table 5.

IV. EXTERNAL EVENTS

So far only device failure events were considered. There can be events external to the switching circuit from which the inverter needs to be protected. These are briefly discussed in the following sections

(A.) AC side line overcurrent

AC line breakers provide the primary protection in case of severe near faults. Gating off at least the internal GTOs (RG3-RG7, SG3-SG7, TG3-TG7) serves as a back-up protection. However, the voltages across the devices is now virtually uncontrolled and could lead to overvoltage stresses on the devices. Distant faults will not have a significant impact because of the linking reactors which serve to limit the fault current.

(B) DC capacitor voltage swings

Severe capacitor overvoltage can be controlled by adding a crowbar switch across each capacitor - this leads to a structure for the DC bus as shown in Fig. 17

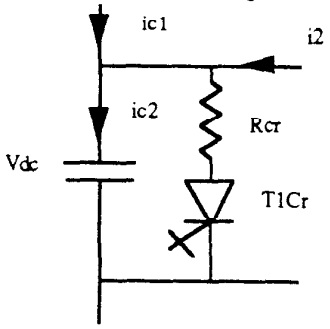


Fig. 17 Crowbar switch

By using a GTO as a crowbar switch it is possible to control capacitor overvoltage. As a back up protection it can be seen that individual capacitor voltages can be held constant by a particular selection of switching states. For example, if capacitor C1 voltage has to be maintained constant, it is evident that the net current through capacitor C1 has to be zero. This can be accomplished by simply ensuring that only those switching states are selected which cause the line currents to circulate on the same side of the capacitor C1. Thus, a switching state (2, 2, 2) causes no net current to flow through C1. In addition, a switching state of the form (1,0,-1), (0,1,-2) etc. also causes no net current to flow through C1. Thus, the constraint of constant capacitor voltage causes a partition of the set of switching states. This method works for controlling the overvoltage on any one capacitor. Used for balancing more than one capacitor voltage reduces the number of switching state that can be used so that the harmonics in the generated voltage increase. All capacitor voltages cannot be simultaneously maintained constant by any switching states except by the zero vector i.e. (R=S=T=-2,-1,0,1,2) i.e. when all the line voltages are identically zero. Table 6 thus summarizes the switching states which maintain constant capacitor voltage.

DC bus capacitor	Switching states for constant voltage
C1	(R,S,T=-2) or (R,S,T=1,0,-1,-2)
C2	(R,S,T=2,1) or (R,S,T = 0,-1,-2)
C3	(R,S,T = 2,1,0) or (R,S,T=-1,-2)
C4	(R,S,T=2,1,0,-1) or (R,S,T=-2)

Table 6 : Switching states for maintaining capacitor voltage

V. CONCLUSIONS

Device failure constitutes the most significant contingency in a multilevel inverter. Not all device failures have the same impact on the inverter operation. Loss of certain devices for instance the inner clamp diodes constrains the inverter operation more severely than the loss of other devices viz. outer GTOs. Failure probability can be reduced by connecting devices in series but at increased cost.

Following a fault, the generated voltage THD as well as DC capacitor voltage ripple is increased because some switching states are lost. If among the switching states lost there are no states that need to be used for voltage balancing of the DC bus capacitors, the inverter can continue to operate at reduced DC bus utilization. The multilevel inverter topology thus offers a degree of robustness with respect to device failure.

VI. ACKNOWLEDGMENTS

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