Design and Implementation of a Passively Clamped Quasi Resonant DC Link Inverter

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Abstract - The passively clamped quasi resonant dc link (PCQRL) inverter is a novel soft switched inverter topology proposed to solve two major problems associated with the conventional passively clamped resonant dc link inverter: the high clamp factor problem and the lack of PWM capability. This paper deals with design and control of a three phase PCQRL inverter. Major design issues are discussed. Successful operation of this novel PCQRL inverter based on a prototype design is demonstrated. The results show that this novel converter can reduce the clamp factor from the value of 2.0 p.u. obtained in previous circuits to around 1.25 and add the PWM capabilities to the conventional passive clamp resonant dc link. Several results are presented to illustrate the performance of the proposed inverter topology.

1. Introduction

The emergence of soft switched topologies for electrical power conversion has brought new perspectives to high performance inverter design. The resonant dc link converter [1-5], which promises to be the next generation of industrial drives, has lately received considerable research attention. A more recent trend seems to an evolution from continuously resonant to quasi resonant strategies owing to the benefits regarding resonant link design and control, device rating requirements and compatibility to PWM and other conventional modulation and drive control techniques [6-12].

A new type of soft switched voltage source inverter - the passively clamped quasi resonant link (PCQRL) inverter had been proposed in reference [13]. The PCQRL topology is aimed at solving two major problems of the conventional passively clamped resonant dc link inverter: the high clamp factor problem and the lack of PWM capability. The circuit has the advantages of low clamp factor, simple resonance control, guaranteed zero link voltage conditions and true PWM capability.

A detailed analysis, simulation and performance characterization of the PCQRL circuit were presented in reference [13]. This paper is concentrated on the design and implementation of the inverter and modulation strategies, as well as experimental verification of system operation and performance.

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2. Inverter Operation Principles

A circuit diagram of the passively clamped quasi resonant dc link (PCQRL) inverter is shown in Fig. 1. The circuit is realized by adding a small switched inductor L_2 to the conventional passively clamped resonant dc link (PCRL) inverter. In contrast to the conventional PCRL [5], the clamp transformer, T, is designed to have a clamp factor, K, equal to 1.1-1.3 instead of more than 2. For current reset purposes, the switched inductor L_2 is realized by two auxiliary switches S_1 and S_2, which are driven by the same gating signal, and two diodes D_1 and D_2. The primary magnetizing inductance of the passive clamp transformer, T, serves as the main resonant inductor L_1.

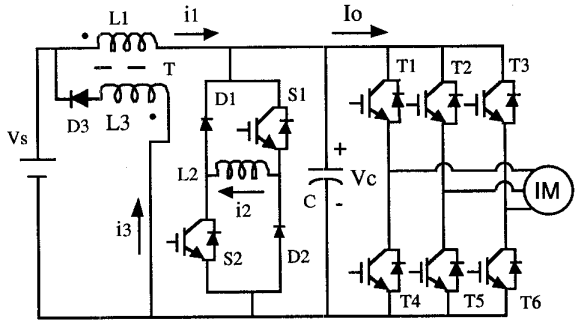


Fig. 1 Passively clamped quasi-resonant DC link inverter.

Inverter operation is illustrated by the link waveforms shown in Fig. 2. Five operating modes can be identified. M_0 corresponds to the pseudo steady state conditions with link voltage equal to V_s and inductor L_1 current equal to link load current I_o. When the auxiliary switches S_1 and S_2 are turned on in a zero current switching (ZCS) manner as a consequence of a switching command from the modulation strategy adopted, the inverter enters mode M_1. During mode M_1, the resonance between L_1, L_2 and C drives the link voltage towards a negative value. Mode 2 starts

when the link voltage reaches zero, and the link voltage is clamped to zero by the anti-parallel diodes of the inverter switches. The states of inverter switches can then be changed under zero voltage conditions. After the inverter switches change state, switches S_1 and S_2 are then turned off in a zero voltage switching (ZVS) manner and the sequence proceeds to mode 3. In mode 3, the link voltage is raised towards $2V_S$ until it hits the clamped voltage KV_S, while the current i_2 decays to zero. The clamping mode M4 corresponds to the clamp period during which time D_3 conducts and the excessive energy in inductor L_1 is fed back to the dc source. After the clamping interval, the link returns to the pseudo steady state M_0 and the cycle repeats for the next switching command.

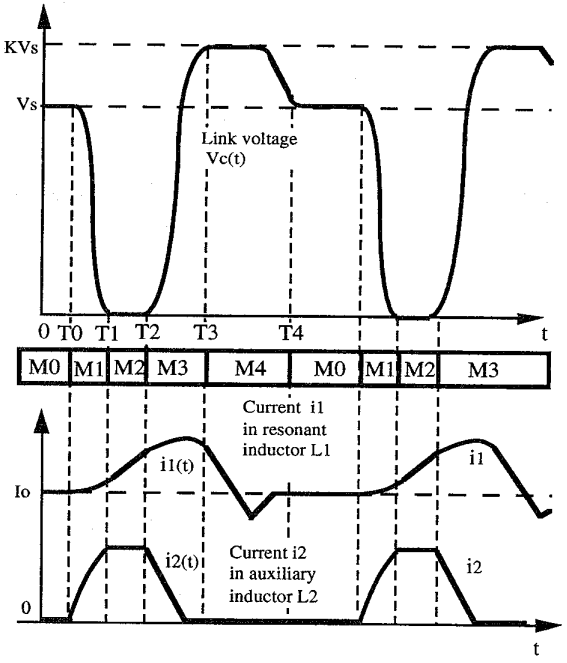


Fig. 2 Illustration of PCQRL operating modes.

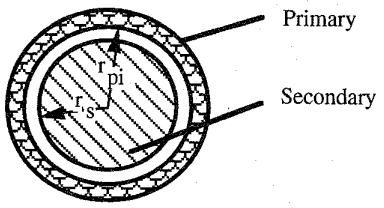
3. Link Design and Control Scheme

The main component in the resonant link is the clamp transformer, T, with its primary magnetizing inductance serving as the resonant inductance L_1, and its secondary as the clamp winding. The turns ratio of the transformer must be designed to be equal to 1:5 for a clamp factor of 1.2. To ensure clamping, the leakage inductance of the clamp transformer must be minimized. The coaxial winding transformer proposed in [15, 16] provides such a means for leakage inductance control.

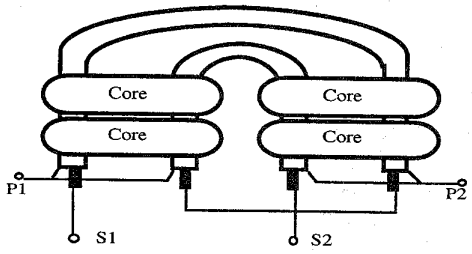
The first approach to control the leakage inductance is through the design of the coaxial winding cross section. For a coaxial coil cross section shown in Fig. 3a), the leakage inductance in the primary (outer wire) is theoretically equal to zero, while the leakage inductance in the secondary (inner wire) equals to

$$L_{leak}=\frac{N_s^2\mu_o}{8\pi}[1+4\ln(\frac{r_{pi}}{r_s})]\ \text{H/m} \qquad (1)$$

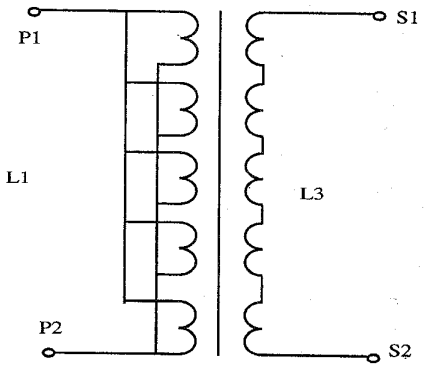
where r_{pi} is the inner radius of the primary braided litz wire (outer conductor), r_s the radius of the secondary litz wire, and Ns the number of secondary turns. Therefore, to minimize the leakage it is desirable to minimize the space between the inner and outer wires.



a) Coaxial winding cross section



b) Split windings for reducing leakage inductance



c) Winding Connection for a 1:5 turn ratio

Fig. 3 Clamping transformer.

The second means to control leakage is based on the so-called winding splitting technique. Assume here that a single coaxial winding has a secondary leakage inductance equal to L_{ls}. Instead of using a large single coaxial winding, one can split this single

coaxial winding into n sub-coaxial windings (electrically insulated between all sub-windings) and then connect, respectively, the primary terminals and secondary terminals of all sub-coaxial windings in parallel. The current carrying capability and the winding inductance will remain the same. However, the total leakage inductance is reduced to L_{ls}/n. This reault is due to the fact that there is no mutual leakage inductance between any two sub-coaxial windings. Thus, when all windings are connected in parallel, all leakage inductances are simply in parallel which yields a total leakage inductance equal to L_{ls}/n.

The same technique applies to the leakage reduction in the design of a clamp transformer with a turns ratio of 1:5. For a split winding configuration as shown in Figs. 3b and 3c, if all the primary terminals of each sub-coaxial winding are connected in parallel while all the secondary terminals are connected in series, a 1:5 turn ratio will be produced. Assuming that the secondary leakage inductance in each coil shown in Fig. 3b equals to L_{ls}, the total secondary leakage inductance of the clamp transformer assembly is equal to $5L_{ls}$. However, by referring to the primary the total leakage becomes equal to $L_{ls}/5$. For the inverter clamp transformer, the measured leakage inductance from the primary is less than 80nH; sufficiently small to produce a good clamping effect.

The link parameters L_1, L_2 and C can be calculated based on specification of the link waveform parameters such as dv/dt and di/dt. Although there are many choices for link parameters to satisfy the waveform requirements, an optimal solution is preferred in that sense that only minimum resonant energy should circulate inside the inverter to achieve soft switching. The theoretical background has been addressed in reference [13] which provides all formulas needed for the calculation. For a 320 V DC bus and a clamp factor of 1.2, a reasonable design of resonant link parameters is shown in Table 1. These parameters lead to peak currents in inductors L_1 (ac component) and L_2 equal to 29.0 A and 28.5 A, respectively.

Table 1. Inverter resonant link parameters

Clamp transfomer:		
turns ratio 1:5		
primary magnetizing inductance	L_1	29.5 μH
secondary inductance	L3	737.5 μH
leakage inductance measured from primary		80 nH
Inductor L_2		14.3 μH
Capacitor C		60.0 nF

Inverter control is implemented based on the link operation requirements that is, whenever a switching is commanded, the auxiliary circuit must first be turned on to initiate a resonant transient. When the link voltage reaches zero, the inverter switches. A block diagram for a generic control scheme is shown in Fig. 4. The circuit is applicable to most of the modulation schemes, including PWM. The edge detector detects the desired state change before the switching command is passed to the inverter switches. The detected edges are used to trigger the turn-on of the auxiliary circuit, while the switching command is synchronized with the link zero voltage condition to ensure zero voltage switching. The hardware is simple with only minor changes from classical modulation schemes for three phase inverters.

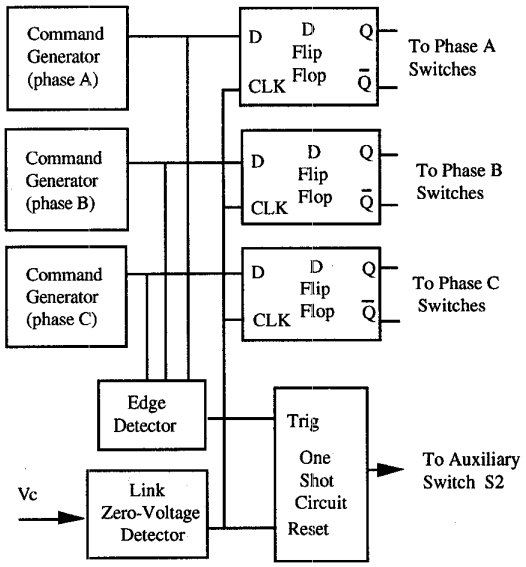


Fig. 4 Inverter control circuit block diagram.

The topology studied in the paper realizes a stable resonant link mode having $V_C = V_S$ and $i_1 = I_O$ (pseudo steady state mode M_0). This fact suggests that it is possible to keep a desired inverter switch state (or output voltage vector) for any desired period of time, leading to a true PWM capability. From the basic waveforms shown in Fig. 2, it is seen that some limitations still exist, as also observed in other quasi-resonant topologies presented in the literature. That is, a finite amount of time is required to build up certain conditions in the resonant circuit, and no inverter switchings can take place during this time. This period is usually associated to the storage of a minimum energy in the resonant circuit to guarantee proper operation and it is normally a function of the load current. In the PCQRL inverter topology, such a period of time is related to the reset of

inductor L_1, corresponding to the clamping period (mode M4). In Fig. 2, it is seen that during the clamping period the inverter switch state cannot change state and it is not possible to drive the dc link voltage down to zero by triggering the auxiliary switches. This fact limits the range of the modulation index in which PWM operation can be obtained. Such a limitation is minimized if the inverter switching period remains large compared to the clamping interval.

Any modulation or drive control strategy that implies fixed or variable frequency operation can be implemented, provided the limitations stated above are respected. Delta modulators with fixed switching frequency, for instance, can be easily implemented with this topology. In this case, the clamping interval limits the maximum switching frequency.

4. Experimental Results

Experimental tests have been performed on the PCQRL inverter prototype supplying a three phase induction machine. A constant Volts/Hertz scheme was adopted. A sigma-delta modulator with a sampling frequency of 20 kHz was employed. The results were obtained with the inverter prototype driving a 3HP, 230V three phase induction machine under rated load. The results were obtained for a converter dc link voltage equal to 335V, slightly higher than the rated value (320V).

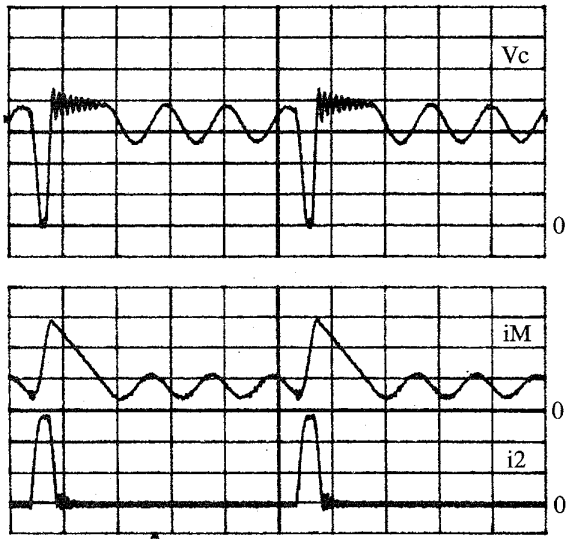


Fig. 5. Resonant DC link waveforms
V_C: 100V/div.; i_M, i_2: 10A/div.
T/div.: 10 μs

Fig. 5 shows the resonant link waveforms: link voltage (V_C), DC bus current ($i_M = i_1 - i_3$) and the auxiliary inductor current (i_2) from top to bottom, respectively. It is seen that a clamping factor close to 1.25 has been achieved. Although the clamping transformer was designed to have a clamp factor equal to 1.2, the clamp action cannot take place immediately after link voltage reaches $1.2V_S$ due to the presence of the leakage of the clamping transformer. In practice, the clamping process is characterized by a ringing caused by the resonance between the transformer leakage inductance and the resonant capacitor C. Thus, for a lower clamp factor, a lower leakage or a larger turns ratio transformer should be used.

Fig. 6 also shows a more detailed view of the same resonant link waveforms depicted in Fig. 5. All the waveforms are in good agreement with the simulation results reported in reference [13]. The ringing of the auxiliary inductor current waveform (i_2) is caused by reverse recovery of the feed back diodes D_1 and D_2.

As is also pointed out in reference [13], although the topology requires two additional switches S_1 and S_2, to realize resonance control, the current ratings of those two switches are very small which is determined only by the DC bus voltage V_S, link capacitor C, inductance L_1 and L_2. For the prototype inverter, only 30A peak current is required. Another important feature is that the currents ratings of the auxiliary switches are independent of inverter load current which makes this topology attractive for high power applications. A reduction of auxiliary switch count from two to one is also possible which is discussed in reference [14].

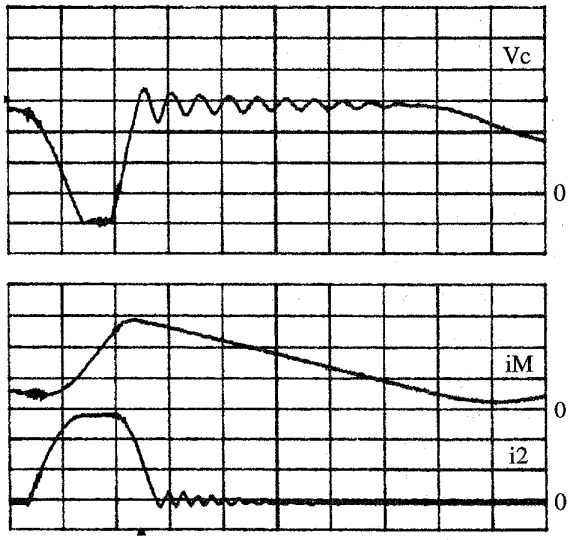


Fig. 6. DC link waveforms. Vc: 100V/div.;
i_M, i_2: 10A/div.; T/div.: 2μs

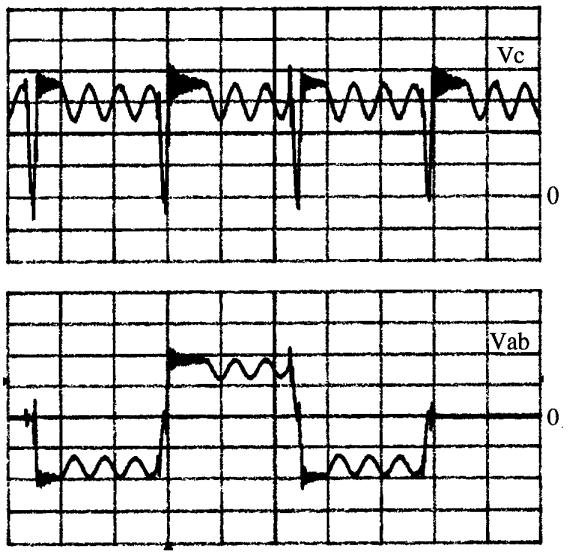


Fig. 7. DC link and output voltages. V_c,V_{ab}: 100V/div.; T/div.: 20μs

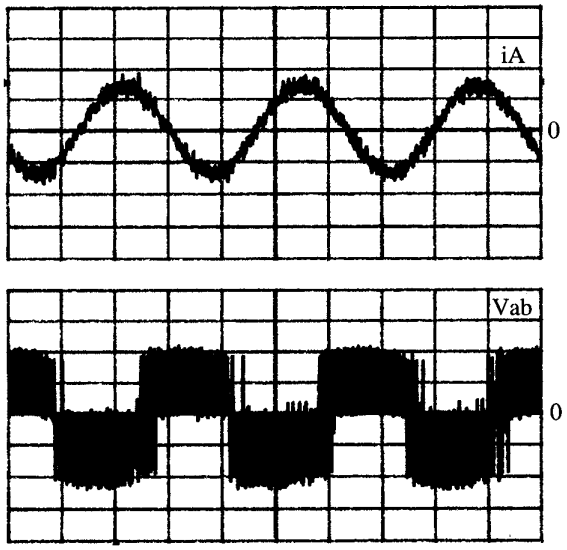


Fig. 8. Output current and voltage waveforms. Phase i_A: 5A/div.; Line to line voltage V_{ab}: 200V/div.; T/div.: 5ms

Fig. 7 shows dc link and output line-to-line voltages, from top to bottom. The synchronism between the zero voltage instants at the dc link and the inverter switching is clearly seen, and soft switching is achieved. Output voltage and current are shown in Fig. 8. The output line to line voltage and load current waveforms have a fundamental frequency close to 60 Hz. It is observed that these waveforms are almost the same as hard switched inverter operated under the same conditions.

4. Conclusion

This paper deals with the practical implementation of the new passively clamped quasi resonant dc link inverter. Operating principles and design issues have been discussed. Successful operation of this novel PCQRL inverter based on the prototype design has been illustrated. The results have demonstrated that this novel converter can reduce the clamp factor from previous values of 2 p.u for resonant link converters to rougly 1.25 and improve modulation capabilities of the conventional passive clamp resonant dc link inverter.

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