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# A Matrix Converter Using Reverse Blocking NPT-IGBT's and Optimized Pulse Patterns

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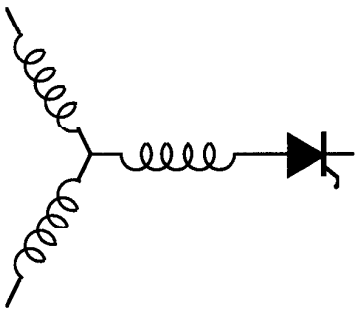

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# A Matrix Converter Using Reverse Blocking NPT-IGBT's and Optimized Pulse Patterns

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***Abstract*—The paper compares three-phase to three-phase IGBT matrix converters in which the required four-quadrant switches are realized by conventional common collector configurations and reverse blocking NPT-IGBT's respectively. A sophisticated semiconductor loss model is used to compute the converter losses for both switch configurations. New pulse patterns are derived to minimize the input current harmonics.**

## I. INTRODUCTION

In recent years the three-phase to three-phase matrix converter (MC) has received considerable attention as an alternative to hard and soft switching dc-link converters. The topology was first investigated in 1976 [1] and then more recently by Venturini [2], [3]. Reference [3] proposes a scheme which generates sinusoidal input currents at unity power factor and increases the voltage transfer ratio to the maximum possible value of $q=v_i/v_o=0.866$. Since then various control principles including space vector modulation (e.g. [4], [5], [6]), and optimized pulse patterns (e.g. [7]) have been proposed overcoming most of the limitations of the matrix converter.

Nine four-quadrant switches (4QSW's) are arranged so that any input phase can be connected to any output phase at any time (Fig. 1). Since the MC operates between a voltage source and a current source there must be always exactly one switch in each of the three switch groups ($s_{1j}$/ $s_{2j}$/ $s_{3j}$; j=1,2,3) closed to avoid short circuits at the input and open phases at the output.

The MC topology has some distinct advantages over conventional hard switching PWM-rectifier /dc-link/ inverter structures. For example the MC does not require a dc-link capacitor due to its single stage power conversion. Furthermore it is expected that the MC generates substantially less switching and total losses than the comparable dc-voltage link topology, because the average commutation voltage of the MC (line-to-line-voltage) is distinctly lower than that of the dc-link topology (dc-link-voltage). On the other hand the dc-link converter requires only 24 semiconductors (12 IGBTs, 12 diodes) and the MC needs 36 semiconductors (18 IGBTs, 18 diodes) if conventional IGBT's in a common emitter or common collector configuration are applied (Table I). However, the use of forward and reverse blocking NPT-IGBT's reduces the number of semiconductors in the MC by 50% bringing the converter in a real competitive position to the well known dc-link topology.

The paper presents a description of the stress of the four-quadrant switches of a hard switching MC for conventional

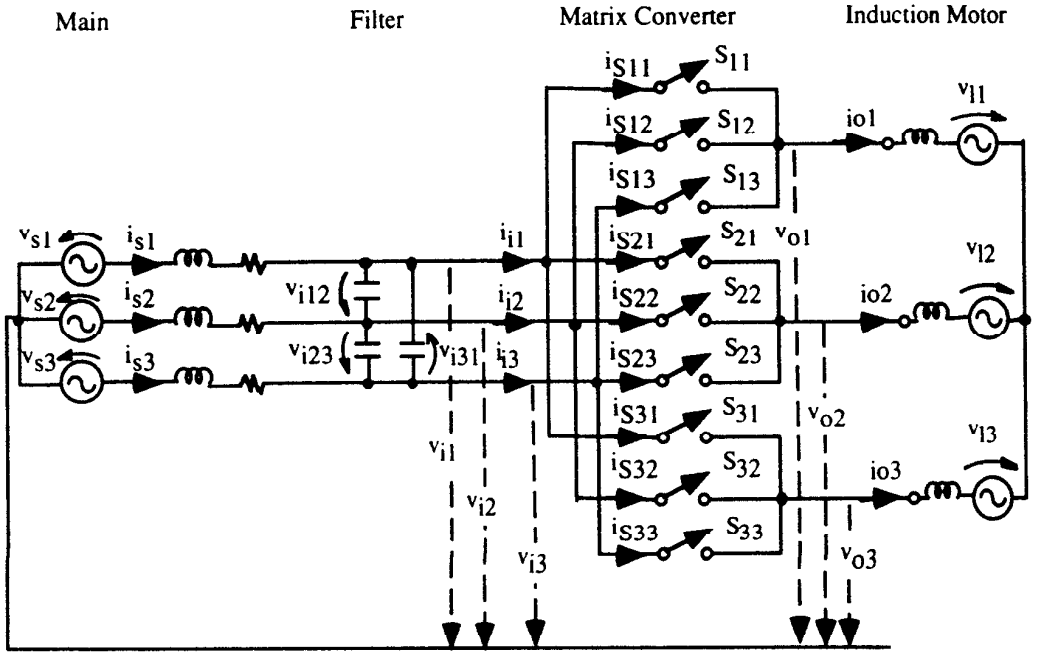



Fig. 1: Circuit configuration of a three-phase MC

common collector switch configurations (CCC's) and switch implementations with reverse blocking NPT-IGBT's (RB-NPT-IGBT's). The switching and on-state losses of both switch implementations are measured in a suitable test circuit. The results achieved are the basis for an estimation of the total converter losses using a new power semiconductor loss model. Optimized pulse patterns which considerably reduce the input current harmonics are proposed.

## II. FUNDAMENTAL COMMUTATIONS OF A MATRIX CONVERTER

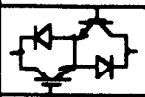
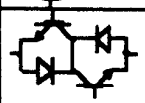
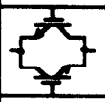
The commutation of an output phase current from one switch to another in each of the three switch groups can be described by the equivalent commutation circuit presented in [8]. In this case the load current corresponds to the motor phase current under consideration, the commutation voltage represents the effective line-to-line voltage at the input and the minimum values of the commutation inductivity and the commutation capacity are given by the stray inductance of the circuit and the output capacitance of the semiconductors respectively. Corresponding to the power of the load, two fundamental types of commutations can be distinguished - the so called inductive commutation and the capacitive commutation [8]. The inductive commutation is initiated by a hard turn-on transient of a 4QSW (IGBT) and completed by the passive turn-off transient during the interruption of the reverse current. In contrast to this the capacitive commutation is characterized by a hard turn-off transient (IGBT) and a low loss passive zero voltage turn-on transient.

Because both the commutation voltage (line-to-line input phase voltage) and the load current (motor phase current) change the polarity during the operation of the matrix converter the switches in Fig. 1 must be forward and reverse blocking bi-directional current conducting switches (4QSW's).

## III. PRACTICAL IMPLEMENTATIONS OF FOUR-QUADRANT SWITCHES ON THE BASIS OF IGBTS

The switches of a MC should be realized on the basis of IGBT's for medium breakdown voltages (600 V$\leq v_{BR} \leq$1700 V) and switching frequencies (5 kHz$\leq f_S \leq$40 kHz). The most important IGBT-switch configurations of a MC and of the conventional hard switching dc-voltage-link converter are depicted in Table I for comparison purposes. Configurations 1 and 2 show how a back to back arrangement of IGBT's may be used to implement the required bi-directional switch. The two diodes are used to provide the reverse voltage blocking capability. The diodes are also effectively placed in parallel with the IGBT by use of the short at the mid point of the two branches. These arrangements are preferable to the analogous configurations without a short at the mid point as they prevent a possible avalanche breakdown of the IGBT's during the interruption of the reverse current. Furthermore both the common emitter and the common collector configuration allow the use of single modules reducing the costs of assembly substantially. Because the common collector arrangement requires the minimum number of isolated gate drives this switch configuration is the cheapest and also technically preferable implementation of all back-to-back configurations on the basis of conventional PT- or NPT-IGBT's. A comparison of the number of the required semiconductors shows that the matrix converter needs

TABLE I
SWITCH CONFIGURATIONS OF A MATRIX CONVERTER

| | Variant | Switch Configuration | Driver | IGBTs/ Diodes/ Total |
|---|---|---|---|---|
| Matrix Converter | 1 |  | 9 | 18 / 18 / 36 |
| | 2 |  | 9 | 18 / 18 / 36 |
| | 3 |  | 6 | 18 / 0 / 18 |
| DC-Voltage-Link Converter | |  | 7 | 12 / 12 / 24 |

6 IGBTs and 6 diodes more than the comparable PWM dc-voltage-link converter if the CCC is used as 4QSW (Table I). In spite of these different numbers of required semiconductors, a detailed investigation of the switch ratings has shown that the installed total switch power of both circuits is generally the same due to the possible reduction of the current ratings of the switches in the matrix converter by one third [4].

The expense of semiconductors can be reduced even more if one uses the capability of NPT-IGBT's to block both forward and reverse voltages. The saved series diodes and the possible reduction of the current ratings of the IGBT's are the reason therefore, that in this case the installed total switch power of the matrix converter can be distinctly lower than that of the dc voltage link converter.

## IV. BEHAVIOR OF FOUR-QUADRANT SWITCHES ON THE BASIS OF COMMON COLLECTOR CONFIGURATIONS AND REVERSE BLOCKING NPT-IGBTS

To illustrate the advantages of the matrix converter over the dc voltage link converter, measured on-state and switching losses of CCC's and RB-NPT-IGBT's will now be discussed. The CCC's were realized using the NPT-IGBT BUP 304 (1000V, 25A) and the fast epitaxial diode BYP 103 (1000V, 45A). The 4QSW with RB-NPT-IGBT's used the same IGBT BUP 304 but without additional diodes. In contrast to the CCC a gate voltage of $v_{GE}$=+15V was applied in the reverse blocking state of the RB-NPT-IGBT to minimize the leakage current and the stationary reverse blocking losses [9], [10].

The measured on-state voltages of both switch arrangements are to be seen in Fig. 2. Because of the additional voltage drop across the series diode the resulting on-state voltage of the CCC is about 40% higher on average than that of the RB-NPT-IGBT.

Detailed investigations of the switching losses of 4QSW's showed that nearly all switching losses are caused by the active turn-on transient of the IGBT's ($W_{ON-T}$), the turn-off losses during the reverse recovery process of the diodes ($W_{OFF-D}$) and the RB-NPT-IGBT's ($W_{OFF-NPT}$)

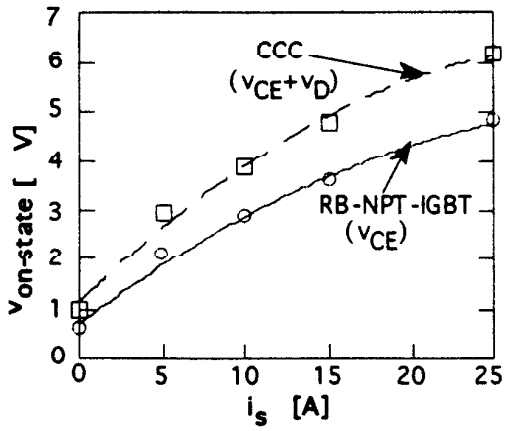



Fig. 2: On-state voltages of CCC's and RB-NPT-IGBT's (BUP 304; BYP 103; $T_j$=125° C)

respectively and the active turn-off transient of the IGBT's ($W_{OFF\text{-}T}$). Fig. 3 shows the measured switching losses of both types of switch configurations in a hard switching buck converter which was used as a simple equivalent circuit to determine the losses in the MC. Obviously the IGBT turn-on losses $W_{ON\text{-}T}$ are distinctly higher than the turn-off losses $W_{OFF\text{-}T}$ of the IGBT's. Even more important is the fact that the reverse recovery losses of the RB-NPT-IGBT ($W_{OFF\text{-}NPT}$) are drastically higher than those of the fast epitaxial diode ($W_{OFF\text{-}D}$) because of the unfavorable charge carrier distribution and the high carrier lifetime in the NPT-IGBT. However, it must be taken into account that the investigated currently produced NPT-IGBT's are not designed for the passive turn-off transient. A substantial improvement of the poor reverse recovery behavior of the NPT-IGBT appears to be possible by a reduction of the carrier lifetime and an increase in the emitter efficiency.

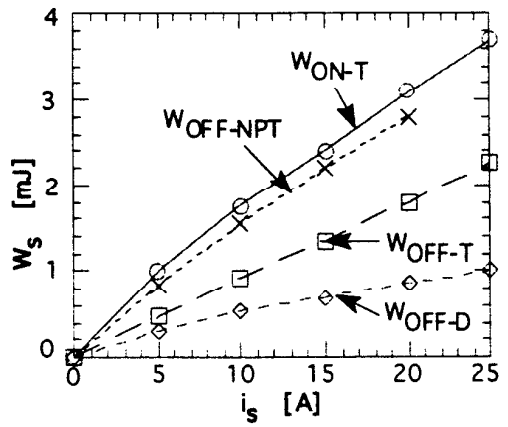



Fig. 3: Switching losses of CCC's and RB-NPT-IGBT's (BUP 304; BYP 103; $T_j$=125° C; $v_C$=600V)

## V. A NEW MODEL FOR THE SEMICONDUCTOR LOSS ESTIMATION IN THE MATRIX CONVERTER

A new semiconductor loss model has been developed to determine and to compare the losses in a matrix converter for different switch implementations. The basis of the model is the analytical description of the measured switching losses and on-state voltages at junction temperatures of $T_j$=25° C and $T_j$=125°C by the following equations :

$$v_{CE} = \left(v_{0T} + r_{0T} \cdot i_S^{B_{conT}}\right) \cdot \left(1 - \frac{125°C - T_j[°C]}{100°C} C_{conT}\right)$$

$$v_D = \left(v_{0D} + r_{0D} \cdot i_S^{B_{conD}}\right) \cdot \left(T_j[°C] - 125°C\right) C_{conD}$$

$$W_{ONT} = \left(A_{ONT} \cdot i_S^{B_{ONT}}\right) \left(1 - \frac{125°C - T_j[°C]}{100°C} C_{ONT}\right) \cdot F$$

$$W_{OFFT} = \left(A_{OFFT} \cdot i_S^{B_{OFFT}}\right) \left(1 - \frac{125°C - T_j[°C]}{100°C} C_{OFFT}\right) \cdot F$$

$$W_{OFFD} = \left(A_{OFFD} \cdot i_S^{B_{OFFD}}\right) \left(1 - \frac{125°C - T_j[°C]}{100°C} C_{OFFD}\right) \cdot F$$

$$F = \left(1 - \frac{600V - |v_C[V]|}{600V}\right)$$

where $v_C$ : Commutation voltage
$i_S$ : Switch current
$T_j$ : Junction temperature
$v_0$ : Bias voltage at $T_j$=125° C
$r_0$ : Dynamic resistance at $T_j$=125° C
A,B,C : Curve fitted constants at $T_j$=125° C, ($v_C$=600V)

The fitting of the on-state voltages and switching losses for the IGBT BUP 304 and the diode BYP 103 with "Mathematica" subsequently generated the constants given in Table II.

TABLE II
FITTED PARAMETERS FOR LOSS SIMULATION

| | BUP 304 | BYP 103 |
|---|---|---|
| $v_{0T/D}$ | 0.6 | 0.4 |
| $r_{0T/D}$ | 0.72 | 0.18 |
| $B_{conT/D}$ | 0.53 | 0.53 |
| $C_{conT/D}$ | 0.2 | 0.00365 |
| $A_{ONT}$ | 0.43 | |
| $B_{ONT}$ | 0.64 | |
| $C_{ONT}$ | 0.37 | |
| $A_{OFFT}$ | 0.1 | |
| $B_{OFFT}$ | 0.97 | |
| $C_{OFFT}$ | 0.27 | |
| $A_{OFFD}$ | 0.23 | 0.09 |
| $B_{OFFD}$ | 0.84 | 0.74 |
| $C_{OFFD}$ | 0.27 | 0.73 |

In addition to this analytical approximation of the occurring losses, the model contains an algorithm which determines the type of each switching transient and distributes the losses to the active semiconductors of the 4QSW's.

As an example Fig. 4 shows the computed on-state voltages of the active IGBT's and diodes of the switch $s_{11}$.

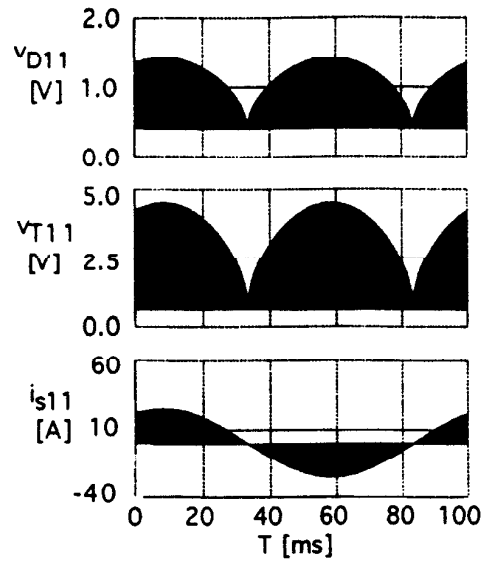



Fig. 4: Simulated switch current and on-state voltages of a CCC (BUP 304; BYP 103; 480V main; $i_{omax}$ =25 A; $f_i$ = 60 Hz; $f_o$= 10 Hz; q=0.166; $f_s$= 20 kHz; $T_j$= 125° C)

The line-to-line voltage $v_{i31}$, the switch current $i_{s11}$ and the instantaneous turn-on losses of one IGBT of the switch $s_{11}$ are to be seen in Fig. 5.

Because on the one hand the switching and on-state losses are computed at each integration step and on the other hand also the fitted functions closely approximate the measured losses, the developed loss model should describe the semiconductor losses of an actual matrix converter very accurately.

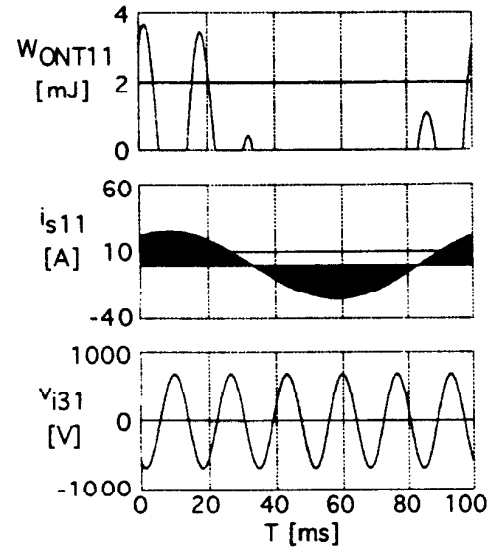



Fig. 5: Simulated line-to-line voltage, switch current and turn-on losses of an IGBT in a CCC (BUP 304; BYP 103; 480 V main; $i_{omax}$= 25 A; $f_i$= 60 Hz; $f_o$= 10 Hz; q= 0.166; $f_s$= 20 kHz; $T_j$=125°C)

## VI. LOSS COMPARISON OF A MATRIX CONVERTER WITH COMMON COLLECTOR SWITCH CONFIGURATIONS AND REVERSE BLOCKING NPT-IGBT'S

Figures 6 and 7 show the simulated semiconductor losses of a MC as a function of the switching frequency if the MC is operated at an 480V and 230V main (60 Hz) respectively.

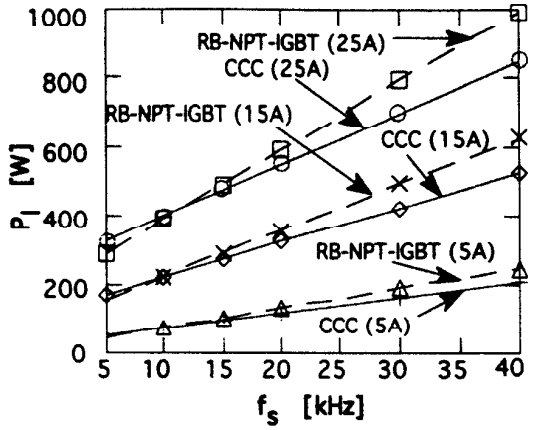



Fig. 6: Simulated matrix converter losses for RB-NPT-IGBT's and CCC's (BUP 304; BYP 103; 480V main; $i_{omax}$=5A/15A/25A; $f_i$ = 60 Hz; $f_o$= 30 Hz; q = 0.5; $\varphi_i$ = 0°; $\varphi_o$ = 30° ; $T_j$ = 125° C)

It is obvious that the MC with RB-NPT-IGBT's halves not only the number of the required switches but generates also less losses than MC with conventional CCC's up to cross-over switching frequencies of $f_{scr}$ = 6 kHz ($i_{omax}$ = 5 A), 10 kHz ($i_{omax}$ = 15 A), 12 kHz ($i_{omax}$ = 25A) [480 V-main] and $f_{scr}$ = 12kHz ($i_{omax}$ = 5 A), 20 kHz ($i_{omax}$ = 15 A), 25 kHz ($i_{omax}$ = 25A) [230V-main] respectively. For $f_s$>$f_{scr}$ the excellent reverse recovery behavior of the fast epitaxial diode selected and the resulting low diode turn-off losses $W_{OFF-D}$ are the reason therefore that the CCC realizes lower

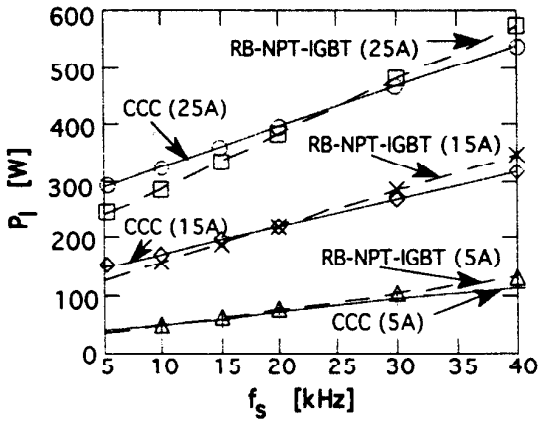



Fig. 7: Simulated matrix converter losses for RB-NPT-IGBT's and CCC's (BUP 304; BYP 103; 230V main; $i_{omax}$=5A/15A/25A; $f_i$=60Hz; $f_o$=30Hz; q=0.5; $\varphi_i$=0 °; $\varphi_o$=30 ° ; $T_j$=125 ° C)

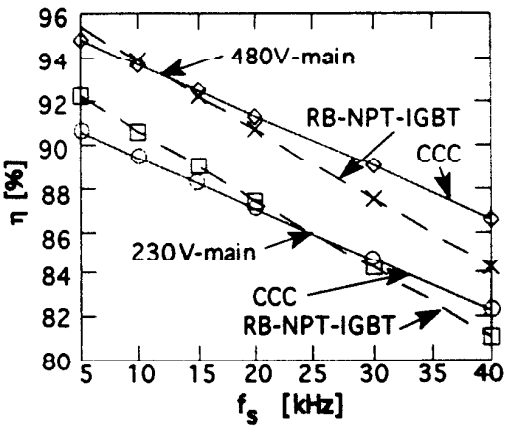



Fig. 8: Simulated matrix converter efficiency for RB-NPT-IGBT's and CCC's (BUP 304; BYP 103; $i_{omax}$=25A; $f_i$=60Hz; $f_o$=30Hz; q=0.5; $\varphi_i$=0 ° ; $\varphi_o$=30 ° ; $T_j$=125 ° C)

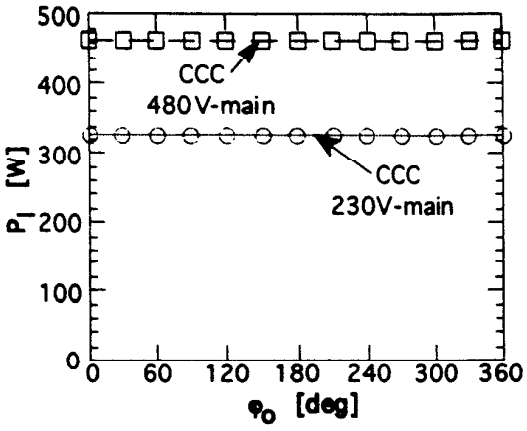



Fig. 10: Simulated matrix converter losses for CCC's (BUP 304; BYP 103; $i_{oRMS}$=15A; $f_i$=60Hz; $\varphi_i$=0 ° ; $f_o$=30Hz; q=0.5; $f_s$=20kHz; $T_j$=125 ° C)

losses than RB-NPT-IGBT's despite the additional voltage drop across the diodes. Because of the different average commutation voltages of the two considered mains, the cross-over switching frequencies of a MC at 230 V are approximately twice as much as that of the MC at 480 V.

The resulting efficiency η of the MC with both switch configurations is depicted in Fig. 8 for $i_{omax}$ = 25 A. As expected the converter efficiency goes up with increasing voltage utilization of the switches.

Fig. 9 shows the distribution of the losses of a MC with a

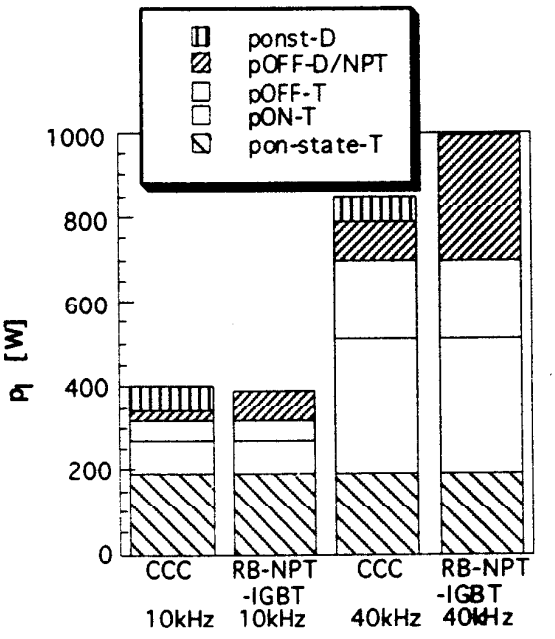



Fig. 9: Loss distribution in a matrix converter for RB-NPT-IGBT's and CCC's (BUP 304; BYP 103; 480V main; $i_{omax}$=25A; $f_i$=60Hz; $f_o$=30Hz; q=0.5; $\varphi_i$=0 ° ; $\varphi_o$=30 ° ; $T_j$=125 ° C)

480V main supply for switching frequencies of $f_s$ = 10 kHz and $f_s$=40 kHz. The on-state losses are roughly so high as the switching losses at $f_s$=10 kHz (CCC : $P_s$=0.37·$P_l$; RB-NPT-IGBT:: $P_s$=0.51·$P_l$). However the switching losses dominate clearly at $f_s$=40 kHz (CCC : $P_s$=0.7·$P_l$; RB-NPT-IGBT : $P_s$=0.81·$P_l$). Although the simulations show, that both switch arrangements can be operated at switching frequencies of $f_s$>40 kHz the substantial switching losses and low converter efficiencies at high switching frequencies limit the switching frequency to about 20 kHz - 25 kHz.

The dependence of the converter losses of the phase shift $\varphi_o$ at the output and the voltage ratio $q=v_o/v_i$ can be seen in the Figures 10 and 11. In contrast to the PWM-voltage source inverter, where the losses are strongly dependent on the modulation index and the phase shift $\varphi_o$ due to the different on-state voltages of IGBT and diode [11], the losses of the MC are independent of the phase shift $\varphi_o$ and the voltage ratio q because of the symmetrical structure of the 4QSW's.

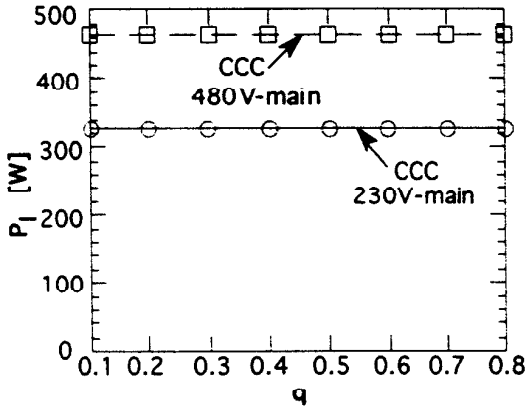



Fig. 11: Simulated matrix converter losses for CCC's (BUP 304; BYP 103; $i_{oRMS}$=15A; $f_i$=60Hz; $f_o$=30Hz; ; $f_s$=20kHz; $\varphi_i$=0 ° ;$\varphi_o$=30 °;$T_j$=125 ° C)

## VII. AN OPTIMIZED PULSE PATTERN TO MINIMIZE THE INPUT CURRENT HARMONICS

Each output phase of a three-phase to three-phase matrix converter is connected to each input phase for a certain time period during each switching interval where each time period is determined so that each output voltage is to be an average voltage of three input voltage pulses. For example, the output phase 1 is connected to the input phase 1 for a time interval $t_{sw11}$, to the input phase 2 for a time interval $t_{sw12}$, and to the input phase 3 for a time interval $t_{sw13}$, where $t_{sw11} + t_{sw12} + t_{sw13} = T_s$ and the switching interval $T_s = 1/f_s$ ($f_s$ is the switching frequency). When the switching frequency $f_s$ is 10 kHz the switching interval $T_s = 100$ µsec. The output phase 2 is connected to the input phase 1 for a time interval $t_{sw21}$, to the input phase 2 for a time interval $t_{sw22}$, and to the input phase 3 for a time interval $t_{sw23}$, where $t_{sw21} + t_{sw22} + t_{sw23} = T_s$. The output phase 3 is connected to the input phase 1 for a time interval $t_{sw31}$, to the input phase 2 for a time interval $t_{sw32}$, and to the input phase 3 for a time interval $t_{sw33}$, where $t_{sw31} + t_{sw32} + t_{sw33} = T_s$. The three phase output voltages can be described as,

$$v_{o1} = v_{i1} * \frac{t_{sw11}}{T_s} + v_{i2} * \frac{t_{sw12}}{T_s} + v_{i3} * \frac{t_{sw13}}{T_s}$$

$$v_{o2} = v_{i1} * \frac{t_{sw21}}{T_s} + v_{i2} * \frac{t_{sw22}}{T_s} + v_{i3} * \frac{t_{sw23}}{T_s}$$

$$v_{o3} = v_{i1} * \frac{t_{sw31}}{T_s} + v_{i2} * \frac{t_{sw32}}{T_s} + v_{i3} * \frac{t_{sw33}}{T_s}$$

There is no restriction on the sequence of the three time intervals, that is, the output phase 1 can be connected to the input phase 2 first and then phase 3 and phase 1, or to the input phase 3 first and then phase 1 and phase 2. The average value of the output voltage $v_{o1}$ remains the same in either switching sequence combination. It can be shown that there exist 216 different switching sequence combinations for a nine-switch three-phase to three-phase matrix converter to produce a specific three-phase output voltage. The matrix converter input current characteristics depends on the switching sequence combinations while the output current characteristics are not significantly affected by the change of the switching sequence combinations.

A switching sequence combination was developed to obtain a balanced three-phase input current characteristics of the matrix converter (the combination #1). With the combination #1, the output phase 1 is connected to the input phase 1 first and phase 2 next and then phase 3, the output phase 2 is connected to the input phase 2 first and phase 3 next and then phase 1, and the output phase 3 is connected to the input phase 3 first and phase 1 next and then phase 2. The three phase input currents are well balanced with combination #1.

To reduce the total rms value of the input currents another switching sequence combination was developed (combination #2). With the combination #2 the output phase 1 is connected to the input phase 1 first and phase 2 next and then phase 3, which is same as the combination #1, however, both the output phase 2 and phase 3 are connected to the input phase 1 first and phase 2 next and then phase 3 in the same manner as the output phase 1, which is illustrated in Fig. 12. As shown in Fig. 12, during the time period of $t_{sw11}$ the input phase 1 is connected to all the output phases, that means that $i_{i1} = i_{o1} + i_{o2} + i_{o3} = 0$. Also $i_{i1} = 0$ during the

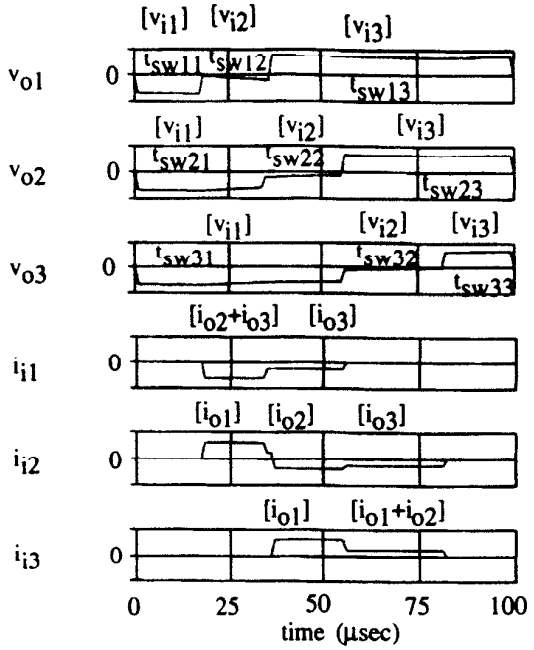



Fig. 12: Illustration of the switching scheme #2 for one period of the switching sequence

time period $t_1 = T_s - t_{sw31}$ because no output phases are connected to the input phase 1. The input phase 2 current $i_{i2} = 0$ during the time periods $t_2 = t_{sw11}$ and $t_3 = t_{sw33}$ because no output phases are connected to the input phase 2. During the time period $t_{sw33}$ the input phase 3 is connected to all the output phases, which means $i_{i3} = 0$, and also $i_{i3} = 0$ during the time period of $t_4 = T_s - t_{sw13}$. The simulation result shows that the rms current of the input phase 1 with the combination #2 is 39 % less than the one with the combination #1. The rms values of the input phase 2 and 3 currents with the combination #2 are 17 % and 39 % less than the ones with the combination #1, respectively. The rms current of the input phase 2 is 34 % larger than the input phases 1 and 3.

The switching sequence combination #3 is defined to have all the three phase outputs connected to the input phase 2 first and phase 3 next and then phase 1. The rms currents of the input phase 1, 2 and 3 with the combination #3 are 39 %, 39 % and 17 % less than the sequence with combination #1, respectively. All the three-phase outputs are connected to the input phase 3 first and phase 1 next and the phase 2 with the switching sequence combination #4. The rms values of the input phase 1, 2 and 3 currents with the combination #4 are 17 %, 39 % and 39 % less than the ones with the combination #1, respectively.

The switching sequence combination #5 was developed to obtain the minimum and balanced three phase input currents. The combination #5 uses the three switching sequence combinations #2, #3 and #4. The switching sequence combinations #2, #3, and #4 create less input harmonic currents, though one input phase has more harmonic current than the other two phases while each phase current has the same fundamental component. The switching sequence combination #5 alternates the combinations #2, #3 and #4 every sampling period. The rms values of the input currents

TABLE III

RMS VALUES OF THREE-PHASE INPUT CURRENTS FOR SIX SWITCHING SEQUENCE COMBINATIONS

| switching sequence combination | rms value of input phase 1 current (%) | rms value of input phase 2 current (%) | rms value of input phase 3 current (%) |
|---|---|---|---|
| #1 | 100 | 100 | 100 |
| #2 | 61 | 83 | 61 |
| #3 | 61 | 61 | 83 |
| #4 | 83 | 61 | 61 |
| #5 | 69 | 69 | 69 |
| #6 | 69 | 69 | 69 |

are well balanced and 31 % less than the ones with the combination #1. Because of the alternation of the three switching sequence combinations, this scheme creates low harmonic frequency components, that is, every one third of the switching frequency.

The lower frequency components of the harmonic currents are harmful because the harmonic currents are amplified near the frequency of the resonance between the filter capacitance and the main source inductances. To avoid the spread of harmonic current components, the switching scheme combination # 6 has been developed. Combination #6 alternates the three switching sequence combinations #2, #3, and #4 with low frequency, that is, for example, applying the switching sequence combination # 2 for 50 milliseconds and then the # 3 for the next 50 milliseconds and the # 4 for the next 50 milliseconds and then repeating the sequence. In this manner the lowest major harmonic current components are limited in the frequency range of 100 Hz below the switching frequency. The developed switching sequence combination #6 is an optimum switching sequence combination for the three-phase to three-phase matrix converter to obtain the minimum and balanced three-phase input current characteristics. The rms values of the input currents with the combination #6 are well balanced and 31 % less than the ones with the combination #1.

Table III summarizes the rms values of three phase input currents for the six switching sequence combinations that are described in this section, where the rms values are relative values to the one with the switching sequence combination #1.

## VIII. CONCLUSIONS

This paper compares IGBT-MC's with conventional common collector switch configurations and reverse blocking NPT-IGBT arrangements. It is shown that by the use of reverse blocking NPT-IGBT's the number of the required semiconductors can be halved in comparison to conventional switch implementations. A new semiconductor loss model was used to compute the losses in a matrix converter for conventional switches and reverse blocking NPT-IGBT's. The comparison of the converter losses shows that reverse blocking NPT-IGBT's realize lower losses up to cross-over switching frequencies of $f_{SCr}$= 6 kHz - 25 kHz. In contrast to PWM voltage source inverters the losses of a matrix converter are independent of the phase shift at the output and the voltage transfer ratio. In addition a new pulse pattern is proposed which minimizes the input current harmonics. This work suggests that matrix converters bear careful consideration as a possible alternative to a conventional dc link PWM rectifier/inverter.

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