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Current-Clamped, Modified Series Resonant DC-Link Power Converter and Control Strategies

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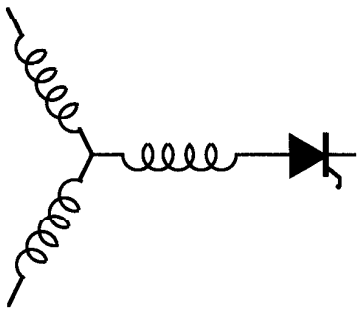

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Abstract - A new AC/AC power converter topology, in which all the switches operate in a resonant fashion to reduce switching losses, is proposed. The topology enables conduction-period control of individual current pulses, whereby PWM has been achieved. The scheme implements current peak (resonant) limiting by a simple diode clamp. Improved switch utilization (voltage· current) and reduced part-count could be cited as the merits of the circuit over the previous soft-switched, current-sourced AC/AC configurations. Moreover a simple controller, that generates "PWM current-controlled, AC output voltages " is introduced, and experimental results are presented. In the scheme an indirect current feed-forward scheme which makes the system robust is introduced; scheme results in smooth controllable motor currents. Therefore, its applicability for a V/F drive is highlighted. For cases where PWM is not possible, an alternative, current-controlled *voltage*-synthesizing method is introduced and simulation results are presented.

1. Introduction

Soft switching schemes are gaining popularity due to their characteristic feature of markedly reduced switching losses. However, soft switching AC/AC topologies generally lack duty-ratio control, and the Pulse Density Modulation (PDM) has been the eventual modulation scheme [1], [2]. The comparison-results of hard and soft switch operation on GTO [3], shows that as high as twenty-fold (20:1) frequency gain could be achieved with the soft switching, but for a comparable spectral content at the output (and to get rid of *sub-harmonic beating*) "PDM" requires much higher switching frequencies compared to Pulse Width Modulation (PWM); as a result, somewhere in the frequency scale, switching loss-reduction achieved by soft-switching could be offset, unless due care is given to the switching frequency.

The topology introduced in this paper facilitates PWM control with soft switching. It simply uses an additional thyristor-diode combination to facilitate PWM, compared to the prototype [1] of PDM control. The PWM capability achieved, helps operating in much lower switching frequencies and yet results in almost comparable spectral performance as much as with the hard-switched current-source converter [4]. Moreover the topology constitutes a current-sourced power converter that competes favorably where lower dv/dt is crucial; lower dv/dt helps reducing the leakage current in the stray capacitance of the motor.

The inverter-controller uses PWM current feed-forward, together with an inner voltage feed-back loop. The scheme has the control-over output *voltage*. Moreover, the inherent current limiting capability of the topology is noticeable. Therefore the system has the favorable characteristics required in implementing a constant Volt per Hertz (V/F) drive, which is the aim of this paper.

1. 1 Overview of the Proposed Power-Converter

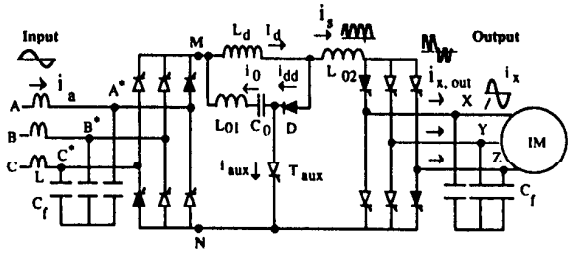


Fig. 1 Proposed Power Circuit Topology.

The proposed AC/AC power-converter topology is drawn in Fig. 1. It generates unity power factor line currents at the input, and harmonically optimized sinusoids at the output. Typical current-pulses seen by bridge thyristors are represented as *pulse-current* i_s in Fig. 1. These pulses are distributed among phases to synthesize reference sinusoids. The width of the current pulses i_s is adjustable, and the adjustment can be assigned to either output or input controller. PWM has been assigned to the output controller in this paper.

1. 2 Circuit Description

Input line impedance L and small filter capacitors C_f in Fig. 1 constitute the low-pass filter at the input, whereas, motor leakage inductance and C_f form the filter at the output. Small inductance L_{01}, L_{02} and capacitor C_0 form the resonant circuits. In addition to being a current source of current I_d, the inductor L_d($>>L_{01}$, L_{02}) plays the role of the energy balancing element of the DC Link.

The converter makes series of resonant current pulses, which are distributed among the input and output phases. When current (i_s) reaches zero at the end of each pulse, bridge-thyristors select new input and output phases. In the process, different voltage values are applied between the points "M" and "N" of the DC side of the input bridge (see Fig. 1). This is used to maintain the average current of I_d, in L_d, at the given reference $I_{d,ref}$; i.e. positive voltage at MN can be used to increase I_d while the negative voltage doing the reverse; moreover the input bridge synthesizes unity power factor line currents. The diode "D" clamps the resonating current i_s flowing in to the load at I_d. The auxiliary thyristor "T_{aux}" adjusts the pulse-width of i_s.

2. Principle of Operation

2.1 Equivalent Circuit

Filter capacitors C_f are considered to be constant voltage sources over the period of a single current-pulse of i_s, because i_s is of higher frequency compared to the input and output waveforms. Therefore, for analytical purposes, the mono-phase equivalent circuit can be drawn as shown in Fig.2. Thyristor T_{equ} in black represents for thyristors

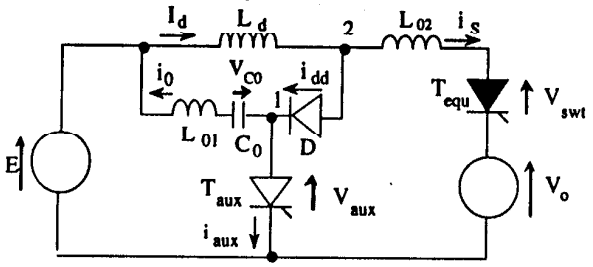


Fig. 2 Mono-Phase Equivalent Circuit.

conducting in series at a time(ex. black thyristors in Fig. 1). E and V_o stand for the input and output voltages-being selected from the input and output phases, in generating a single current pulse. Principle of operation is explained by means of Fig. 2. In an operating cycle the circuit assumes five states which are drawn in Fig. 3; thick black lines represent the current path for each case.

The *time domain* waveforms for the circuit states are drawn in Fig 4 (refer to Fig. 2 or Fig. 3 for relevant parameter locations).

2.2 Current Pulse Generation

1) State 1 : Assume that a DC current of value I_d exists in the inductor L_d. Fig. 3 [1] represents the state-1, where all the thyristors are off and D circulates I_d charging C_0 up linearly. V_{c0} and V_{swt} in Fig. 4 represent the voltage variations across C_0 and T_{equ} respectively. As C_0 gets charged up, the forward voltage of T_{equ}, V_{swt}, builds up until it reaches a defined threshold V_{thm} at t_0, where the state 1 ends.

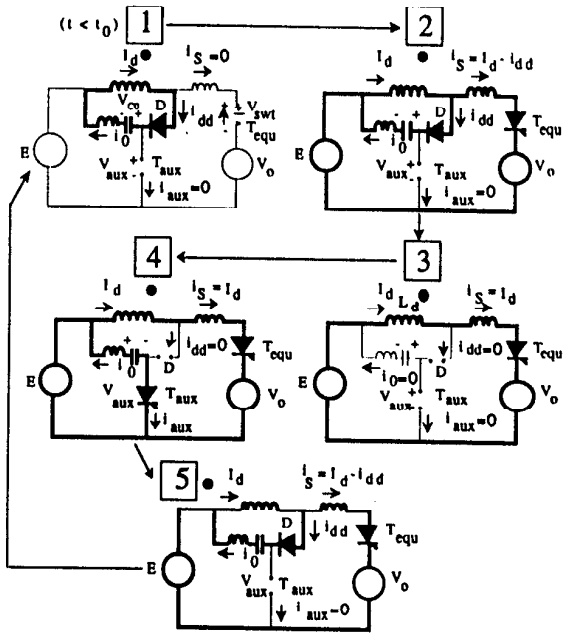


Fig. 3 Circuit States.

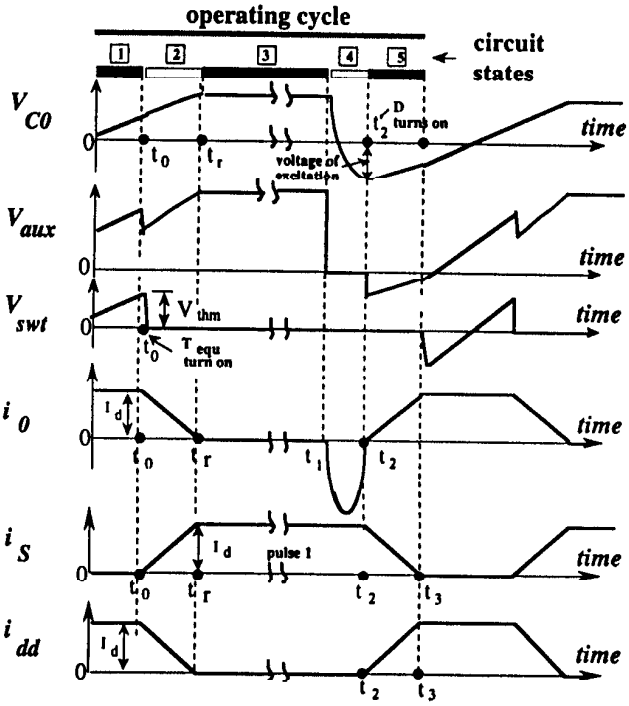


Fig. 4 Voltage and Current Waveforms.

2) State 2 : State 2 is illustrated in Fig. 3 [2] (T_{equ}, D conducting). At $t = t_0$, when $V_{swt} = V_{thm}$, T_{equ} is gated on and i_s starts flowing; i_s can be expressed as,

$$i_s = I_d(1-\cos\omega_0 t) + \frac{V_{swt}(t_0)}{Z_0}\sin\omega_0 t. \quad (1)$$

Where, $Z_0 = \sqrt{(L_{01}+L_{02})/C_0}$, $\omega_0 = \sqrt{1/(L_{01}+L_{02})C_0}$.

i_s is of resonant nature, and it starts growing at t_0 (see plot i_s, Fig. 4). To see the behavior of i_{dd}, node 2 in Fig. 2 is considered, which gives the relation,

$$I_d = i_s + i_{dd}. \quad (2)$$

I_d is constant, therefore, to compensate for increasing i_s, i_{dd} starts to fall and goes to zero at t_r where D turns off and i_s gets clamped to I_d to satisfy (2) (see plot i_s Fig.4).

3) State 3 : Fig. 3 [3] represents the state 3 (T_{equ} - on). The clamped i_s continues to flow through the load as a flat-topped current pulse ($i_s = I_d$), and its width is controllable. State 3 is considered to be the powering mode of the converter.

4) State 4 : The state 4 is drawn in Fig. 3 [4]; T_{aux} is turned-on to reverse the polarity of C_0. The resonant circuit for the case is formed by C_0 and L_{01}. When T_{aux} turns on at t_1, i_0 starts to flow. T_{aux} turns-off at t_2, having reached the current zero (see Fig. 4, plot i_0).

5) State 5 : Soon after T_{aux} has turned-off at t_2, state 5 (Fig. 3 [5]) begins. The reversed C_0 forward bias the D at t_2 (see Fig. 4, plot V_{C0} for tank re-exciting voltage) and re-excites the tank of C_0 and $L_{01}+L_{02}$. The current i_{dd} starts to grow towards I_d, and i_s starts reducing to satisfy the current equation at node-2 ($I_d = i_{dd} + i_s$). i_s reaches zero at t_3, and T_{equ} turns-off marking the end of a single current pulse. Repeating the above procedure current pulses are generated.

3. PWM Current-Controlled Voltage Generation

The *inverter* controller uses current feed-forward and voltage feed-back to generate the commanded voltage. Before going to the details of control, the PWM technique adopted is explained.

3.1. PWM Method

Fig. 5(a) shows two phasor sets, 30° shifted to each other, namely the set $\mathbf{I}_x^*$, $\mathbf{I}_y^*$, $\mathbf{I}_z^*$ and $\mathbf{I}_{xf}$, $\mathbf{I}_{yf}$, $\mathbf{I}_{zf}$. PWM current pulses relevant to the latter phasor-set is generated by this method; Fig. 5(c) shows the generated PWM pulses for the phasor $\mathbf{I}_{xf}$.

i_x^*, i_y^* and i_z^*, are assumed to be the time domain representation of the phasors $\mathbf{I}_x^*$, $\mathbf{I}_y^*$ and $\mathbf{I}_z^*$ respectively. The time domain quantities i_x^*, i_y^* and i_z^* are re-drawn as *difference-sinusoids* (ex. $i_x^* - i_y^*$ etc.) in Fig. 5(b). For instance in Fig. 5(b), between points ⓪ to ①, triangular carrier crosses $i_z^* - i_y^*$ at "M" and $i_x^* - i_y^*$ at "N". The length thus formed, MN, is equivalent to $i_{xf}(= i_x^* - i_z^*)$; therefore, MN is used to generate the pulse ① of the current i_{xf} (of phasor $\mathbf{I}_{xf}$). Digitized form of i_{xf} is marked as i_{xf}^d. Black boxes in Fig. 5(c) represent the zero current vectors. These vectors represent the zone of no-power-exchange between the load and the inverter. The box 1, 2 represents the zero-vector coming between pulses ① and ②; this occurrence of zero-vectors between consecutive pulses of i_{xf} is advantageous, because the converter requires time to charge C_0 in state-1, during which a zero vector is imposed by the converter it self. When the state-1 of the converter does not coincide with the zero vectors prescribed by PWM scheme, an error in zero vector occurs; this error is compensated by using the zero vectors coming in between consecutive pulses of a phase. DSP TMS 320C25 is used in the implementation.

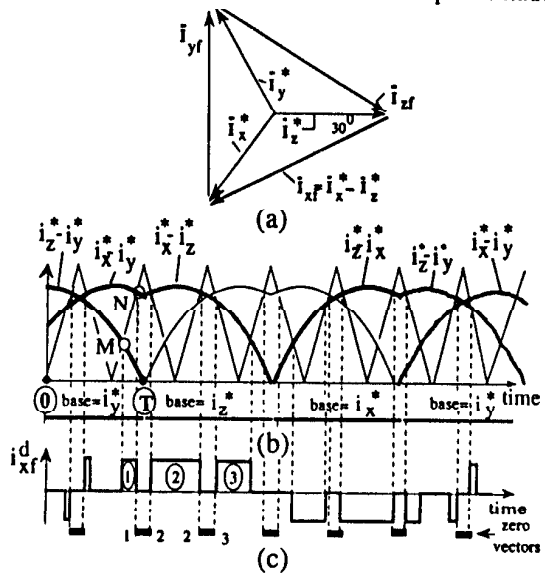


Fig. 5 PWM Method.

3.2 Overview of the Output Control

The output controller implements a current-controlled voltage source. The system-diagram for phase X is illustrated in Fig. 6. A PWM pulse-pattern of sinusoidal reference-current i_{xf} [i_{xf}^d -see Fig. 5(c)], and a sinusoidal voltage reference "$V_{x,ref}$" are stored in a ROM. To start off, the pulse-pattern for reference currents, are used to turn-on the bridge-switches; the voltages V_x, V_y and V_z at terminals X, Y and Z will appear then. Note that the voltage-amplitude is not controlled yet. The amplitude control of the voltage is achieved by a voltage feed-back loop. The reference voltages $V_{x,ref}$, $V_{y,ref}$ and $V_{z,ref}$ are synchronized to respective actual voltages V_x, V_y and V_z, to keep track of the error voltages; ex. the error voltage ΔV_x for phase X, then modifies the duty of the i_{xf}^d, and $i_{x,in}^d$ is formed to fire the output bridge thyristors. For ex. if ΔV_x is positive, voltage V_x is less than the reference, therefore, the duty factor of $i_{x,in}^d$ becomes greater than i_{xf}^d. The experimental pulse-current $i_{x,out}$ resulted from this control is shown in Fig. 8 (b).

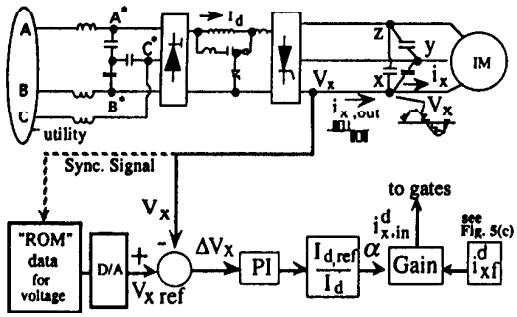
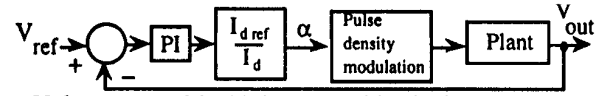
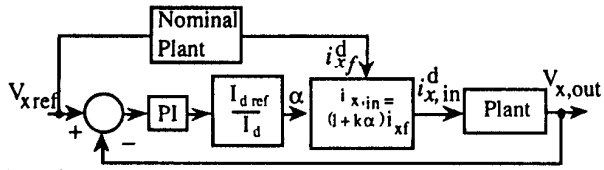


Fig. 6 Output Voltage Control by PWM Current Pulses.

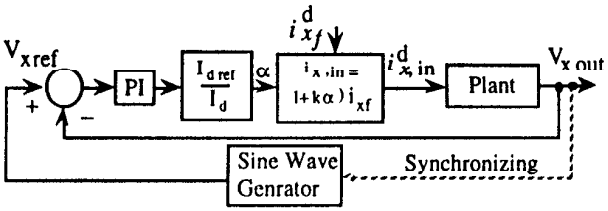
3. 2. 1 Direct and Indirect Current Feed forward



(a) Voltage control by Voltage Feed-back alone



(b) Direct Current Feed-forward, Voltage Feedback



(c) Indirect Current Feed-forward, Voltage Feed-back

Fig. 7 Control Block Diagrams of Output Voltage Control

Fig. 7 (a) and (b) gives an insight into the proposed control. Control for phase X is considered. $V_{x,out}$ is the actual output voltage, and $V_{x,ref}$ is the reference voltage. In Fig. 7(a), voltage control is achieved by the voltage feed-back. No current reference is present for PWM generation, therefore, current-pulses generated by the current-source converter are not synchronized to any external PWM. Only PDM has to be adopted. But PDM yields poor spectral content compared to PWM. The controller in Fig. 7(b) uses a PWM current pattern i^d_{xf} as a template for firing signals; Current feed-forward is used, assuming the plant (filter+motor) model. When the reference voltage $V_{x,ref}$ is given, using the plant model i_{xf} is derived. Next the PWM pattern, i^d_{xf} is obtained. The error-voltage modifies the duty of i^d_{xf}, and $i^d_{x,in}$ is formed; thereby, PWM is performed and the reference voltages are generated. Link current (I_d) variations are compensated by the factor, $I_{d,ref}/I_d$. However, the above scheme uses nominal plant-model in the process; this makes the system parameter dependent. To obtain much simpler and robust system, the controller is modified to the one shown in Fig. 7 (c). The system overview is given in section 3. 2. Here the plant model is avoided by the *voltage synchronization* scheme. i^d_{xf} is used to fire the thyristors, then $V_{x,ref}$ is synchronized to *actual* output voltage $V_{x,out}$; the rest of the controller is similar to the schemein Fig 7(b). This is an indirect current feed-forward scheme where the plant model is emulated. The factor k in Fig. 7(b) controls the gain. Current pulses are synchronized to external PWM algorithm. As seen in Fig. 8 satisfactory motor current and voltage are obtained.

3. 3 Experimental Results

Fig. 8 represents the experimental results. As Fig. 8(a) shows both, motor voltage and current are smooth. Fig. 8(b) shows the actual PWM current pulses $i_{x,out}$ (see Fig. 6, Fig. 1 for $i_{x,out}$) flowing in to phase X. Fig. 8(c) shows the experimental waveforms of voltages v_{c0}, v_{aux} and currents i_0, i_s, shown in Fig. 2.

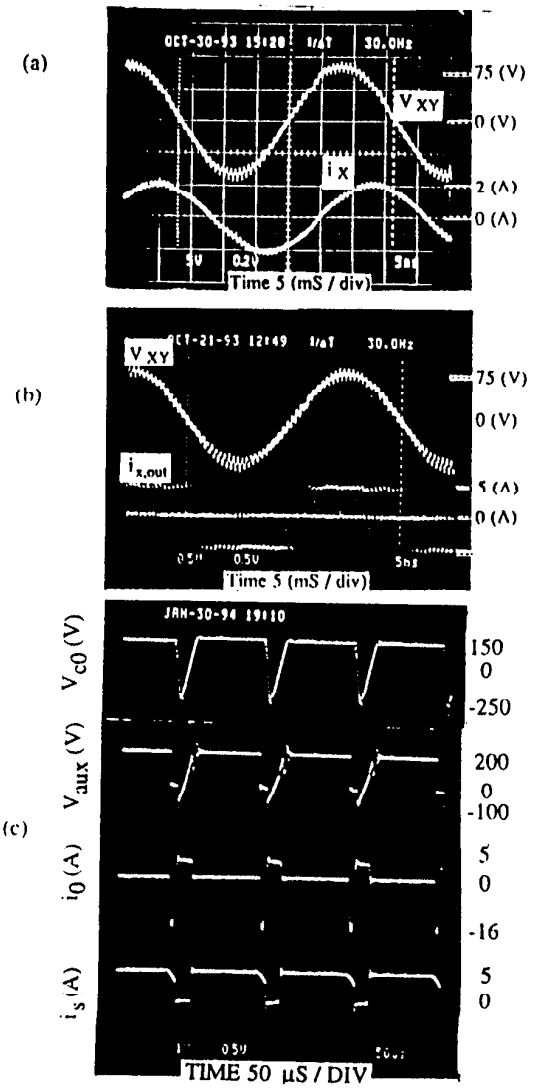


Fig. 8 Experimental Waveforms

(a) Motor Voltage V_{xy} and Current i_x

(b) Motor Voltage V_{xy} and Current $i_{x,out}$

(c) Voltage and Current Waveforms marked in Fig. 2

3. 3. 1 Parameters - Experimental Threephase System

$C_0 = 0.3\ \mu F$, $L_{01} = 40\ \mu H$, $L_{02} = 45\ \mu H$, $L_d = 20mH$
$I_{d,ref} = 5A$, $C_f = 25\ \mu F$;
PWM carrier 1.5 kHz, output frequency 30 Hz.

Switching Devices:

Thyristors; (Toshiba) SH 50L13A, $t_q = 15\ \mu S$
$V_{RRM} = 1000\ V$

Diode; (Fuji Electric) ERG27-10, $t_{rr} = 0.5\ \mu S$
$V_{RRM} = 800\ V$

Motor load: 0.75 kW, 2P, 200 V, 3ϕ

4. PDM Current-Controlled Voltage Generation

As applied to the input line-current control of the converter, the method is explained. *Converter* cannot perform PWM , because current pulses are already synchronized to *inverter* PWM scheme. Therefore PDM is adopted for input control.

4. 1 Integral - hysterisis Voltage Compensation

Input converter in Fig. 1 regulates the current in L_d (I_d) to form a current-source; moreover it synthesizes sinusoidal line currents at a given power factor. The scheme is illustrated in Fig. 9. Control for phase A is illustrated. It uses Integral-Hysterisis voltage compensation method.

Fig. 9(b), represents the blown-up view of the input converter. In the scheme, the active output power is referred to the utility terminal to find reference line currents (ex. $i_{a\,in}$ phase A) of input frequency. Next the reference-line currents are used to establish the reference voltages at points A^*, B^* and C^*; when the line inductance L is known this can be achieved. Actual voltage is sensed and compared with the reference to generate error voltage. Fig. 9(a), represents the "Hysterisis-Integral compensation of voltage at the filter. As shown in the diagram it uses variable hysterisis bands depending on the error. Assume that the Point "P" in Fig. 9(c) represents the point where the actual voltage V_{a^*}(at A^*) lies just before the shaded current pulse occurs; the voltage error at "P" is ΔV_H. During the next/shaded current pulse effort is taken to compensate the error ΔV_{a^*} ($=\Delta V_H + \Delta V_I$) which raises the voltage trajectory to the point Q, as shown in Fig. 9(c). ΔV_H in Fig. 9(c) represents the contribution from the hysterisis part and ΔV_I represents the contribution from integral part. The Hysterisis-Integral compensator is important because it gives fast response without the derivative control [5].

The aim is to compensate errors (ΔV_{a^*} etc.) in all threephases at a time. But since this is a current-sourced converter, only two input thyristors are conducting at a time, therefore, we have to select the input phases conducting, based on an optimization technique. A mode controller is introduced for this purpose and will be discussed. It has been noticed that the controller is less prone to L, C_f related oscillations.

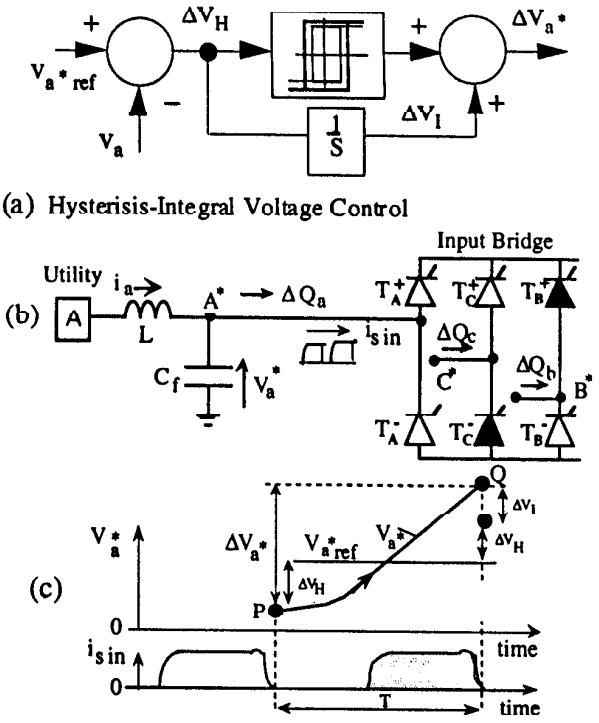


Fig. 9 Illustrations for Input Mode Controller.

4. 2 Mode Controller and Input Switch Selection

A hypothetical converter is assumed to introduce the concept, where all three-phases can conduct at a time. When the shaded current pulse [see Fig. 9(c)] of the DC link is distributed among input phases, the voltage errors of the input filters (C_f's) are assumed compensated. The charge-drawn by the terminals A^*, B^* and C^* in the process is taken to be ΔQ_a, ΔQ_b and ΔQ_c as given in Fig. 9(b). During the period "T", C_f connected to phase A^* draws charge amount of $C_f \cdot \Delta V_{a^*}$. The line current i_a is sinusoidal and assumed constant over the period-T of the current pulse. The charge supplied from the line current of phase A^*, thus become $i_a T$. Now the charge flow at point A^* in Fig. 9(b) would yield,

$$\Delta Q_a = i_a \cdot T - C_f \cdot \Delta V_{a^*}. \qquad (3)$$

ΔQ_b and ΔQ_c can be derived in a similar way. Since there is no neutral conductor, it can be written that,

$$\Delta Q_a + \Delta Q_b + \Delta Q_c = 0. \qquad (4)$$

(4) depicts that the three charge quantities always yield a charge set of mixed (both + and -) polarity. The direction of charge flow is such that, for instance, if ΔQ_a is positive the flow is in the same direction-shown in Fig. 9(b); therefore the upper thyristor on the arm A^*, T_A^+, must be conducting, whereas if ΔQ_a is negative charge flow is in the opposite direction-to that shown in Fig. 9(b), and the

bottom thyristor T_A^- should be conducting. Table 1 summarizes the selection criterion for the input bridge thyristors; "+" and "-" signs represent the polarity of the charge quantities. It follows from the above explanation that "+" and "-" necessarily represent the top and bottom thyristors respectively. Based on the polarity of ΔQ_a, ΔQ_b and ΔQ_c, six unique vectors can be distinguished, The row 1 through 6 in the Table 1 represent them.

However, the converter proposed in this paper is a current-sourced type, which in general permits the selection of only two switches from the input bridge, at a time. Given the above constraint, each of the six vectors could be sub-divided in to two vectors. The division is carried out depending on the magnitude of the charge quantities; for clarification of the fact note that, the vector 1 has sub-divisions depending on the inequality $\Delta Q_a \lesseqgtr \Delta Q_b$. The selected thyristors for each sub-row are tabulated in the last column of the Table 1. The thyristors relevant to maximum and minimum charge quantities are selected for firing; for instance, first row of vector-1 shows

Table 1.

vector	ΔQ_a ⇩	ΔQ_b ⇩	ΔQ_c ⇩	selected switches
1	+	< +	—	T_C^- T_B^+
	+	> +	—	T_C^- T_A^+
2	—	< —	+	T_C^+ T_A^-
	—	> —	+	T_C^+ T_B^-
3	$+^{(\Delta Q_a > \Delta Q_c)}$	—	+	T_B^- T_A^+
	+	—	$+^{(\Delta Q_c > \Delta Q_a)}$	T_B^- T_C^+
4	—	+ > +		T_A^- T_B^+
	—	+ < +		T_A^- T_C^+
5	+	— < —		T_A^+ T_B^-
	+	— > —		T_A^+ T_C^-
6	$-^{(\Delta Q_a < \Delta Q_c)}$	+	—	T_B^+ T_A^-
	—	+	$-^{(\Delta Q_c < \Delta Q_a)}$	T_B^+ T_C^-

the relation," $\Delta Q_b > \Delta Q_a > \Delta Q_c$ ". $\Delta Q_c < 0$ and $\Delta Q_b > 0$, accordingly thyristors in black in Fig. 9(b), marked T_B^- and T_c^-, is the selection for this row.

4. 2. 1 Performance of the Input Mode Controller

Digital simulation has been done at a power of 5 kW. Circuit parameters used are; input line impedance(L) 1 mH, L_d 50 mH, peak line voltage 400 V, $I_{d,ref}$ 50 A. As shown in Fig. 10, fairly smooth line currents of unity power factor can be obtained with smaller fluctuations in I_d. The initial transients die down quite rapidly which justifies the quickness of response of the input controller.

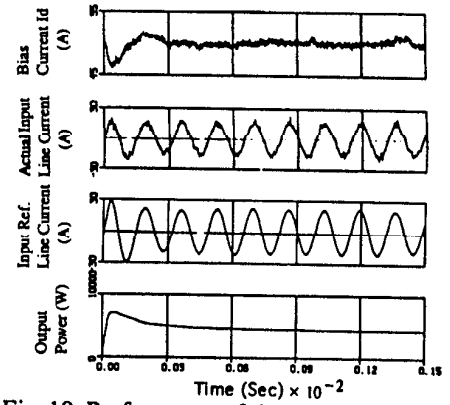


Fig. 10 Performance of the Mode Controller

5. Conclusion

The topology is easy to operate and of smaller part-count; therefore, it constitutes an economically viable system. Output control scheme is robust and it synthesizes commanded output voltage waveforms using PWM current pulses. Therefore the system can be used to implement constant Volt per Hertz operation. Moreover the current source nature of the power converter yields an inherent current limiting capability, which is essential for a V/F controlled motor drive. The *indirect* current feed-forward scheme avoid the requirement of a *nominal plant model.* The system is simple enough to apply for a general purpose V/F drive. The mode-controller uses Hysterisis-Integral control and the system response is fast; it constitutes a good method for PDM-current-controlled voltage generation.

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