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A Four Level Rectifier-Inverter System for Drive Applications

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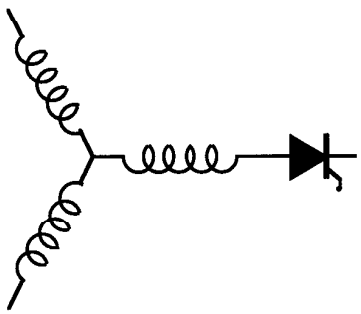

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***Abstract*— Mulitlevel converter technology has been receiving increased attention in the recent past especially for high power applications. In particular, three level drive systems have been extensively reported. In this paper, a four level rectifier-inverter system is investigated for drive applications. A dynamic control algorithm is described which balances the voltages on a 4 level rectifier-inverter drive system primarily from the rectifier. The proposed control method can also generate unity power factor currents at the utility interface. The inverter modulation is relatively unconstrained and modified to implement a zero sequence compensation for added voltage balancing. Simulation results are used to verify the efficacy of the control algorithm.**

I. INTRODUCTION

Multilevel converters are based on the neutral point clamped inverter topology proposed by Nabae et. al. [1]. Subsequently, Bhagwat and Stefanovic [2] demonstrated the possible advantages of a multilevel converter topology. However, by using DC power supplies i.e. batteries, voltage balancing of the DC link capacitors was not demonstrated for possible drive applications. Three distinct topologies have been proposed so far to realize the multilevel inverter (MLI) [3], [4] viz. the diode clamped MLI, the *'flying capacitor'* MLI and MLIs with separate DC sources. So far, attention has been largely restricted to high power, high voltage applications such as static VAR compensation [5] in which the voltage balancing of the DC capacitors is less difficult. However, recently three level rectifier inverter drive system was investigated in [6,7,8] and a partially active 3 level rectifier topology was proposed in [9]. A 5 level inverter using separate DC sources with an induction motor load has been discussed in [10]. Sine triangle PWM of a 4 level inverter, but with a DC voltage source across the DC bus has been demonstrated for limited modulation depths [11].

Based on overall kVA ratings, the device count and ratings of the three topologies, the diode clamped topology is most suitable for drive applications and is the only topology discussed further. An n level diode clamped inverter is characterized by n distinct pole voltage levels and $2n-2$ switches per phase. Also, the n level inverter has $1 + 3n(n-1)$ nominally distinct voltage vectors. The large number of voltage vectors is a significant advantage in regulation and control schemes.

MLIs have a significant distinguishing feature - most voltage vectors in an n level inverter have one or more constitutive switching states for a total of n^3 states for a 3 phase inverter. Therefore, an n level inverter has 1 vector of $(n-1)$ redundancy, 6 vectors of $(n-1)$ redundancy, 12 vectors of $(n-2)$ redundant states etc. The large number of switching states offers a potential means for balancing the DC capacitor voltages and minimizing switching frequency.

Multilevel converters offer several advantages over the conventional 2 level converters such as - (i) Increased number of voltage levels leads to better voltage waveforms and reduced voltage THDs. (ii) Switching dv/dt stresses are reduced. This is advantageous for reducing some of the EMI problems. (iii) Higher voltage levels can be attained by using devices of lower ratings. The diode circuits in this case clamp the voltages across each switch.

The primary disadvantage of an MLI is the increased overall kVA rating due to large device count. However, for a given rated utility and load voltages, the kVA rating of the MLI is much less than the kVA rating of the inverter obtained by scaling a 2 level inverter to the corresponding number of levels. Devices of lower current ratings can be used in each phase at the pole extremities. For large drives, the higher voltages translate to a reduction in current ratings which is highly desirable since it directly leads to cost savings.

MLIs have an additional problem with voltage balancing of the DC bus capacitors. In the absence of an explicit control strategy, the capacitor voltages in an MLI topology tend to deviate from their nominal rated values. Typically, the DC capacitor voltages can be balanced by using the redundant states. This approach has so far been incorporated in a 3 level drive control largely by the use of lookup tables. As compared to a two level inverter, the MLI control is more complex. Reducing the control complexity would clearly serve to make the MLI based drive more feasible.

A drive environment is substantially different from a static VAR compensation application of an MLI. Whereas in static VAR compensation, only reactive power flows between the converter and the system, in a motor drive, the converters must be able to handle bi-directional real power flow. So far, DC voltage balancing has not been satisfactorily discussed for the case when real power is drawn from the inverter. This paper addresses the control issues involved in a drive

application. DC capacitor voltages are balanced for both motoring and regenerating modes of the inverter-motor system. In addition, DC voltages can be balanced even during motor startup with the associated large overcurrents.

II. A FOUR LEVEL INVERTER BASED MOTOR DRIVE

A. The four level inverter

As stated earlier, the *n* level inverter is characterized by a large number of voltage vectors and switching states. In particular, a four level inverter has 37 nominally distinct voltage vectors and 64 switching states. These vectors and switching states are represented in the *dq* plane as shown in Fig. 1. The relative locations of the voltage vectors and the switching states plays a significant role in the control scheme employed. Fig. 2 illustrates the rectifier, inverter pole voltage, DC capacitor voltage and current nomenclature. The inverter switching state shown is $(h_a=3, h_b=2, h_c=0)$ which results in pole voltages given as $V_{ao} = V_{c1} + V_{c2} + V_{c3}$; $V_{bo} = V_{c1} + V_{c2}$; $V_{co} = 0$. More compactly, the inverter pole voltages can be written in terms of switching functions as:

$$V_{abco} = H_{abc} V_C \text{ where } V_C = [V_{c1} \quad V_{c2} \quad V_{c3}]^T \qquad (1)$$

$$H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} \\ h_{b1} & h_{b2} & h_{b3} \\ h_{c1} & h_{c2} & h_{c3} \end{bmatrix}; \quad V_{abco} = \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix}; \text{ and}$$

$$h_{a1} = \delta(h_a - 1) + \delta(h_a - 2) + \delta(h_a - 3)$$

$$h_{a2} = \delta(h_a - 2) + \delta(h_a - 3); \; h_{a3} = \delta(h_a - 3); \quad h_a = 0,1,2,3$$

Here, h_a is the inverter phase A switching function and $\delta(.)$ is the delta function defined as:

$$\delta(x) = 1 \text{ if } x = 0; \; \delta(x) = 0 \text{ if } x \neq 0$$

Thus, if phase A is connected to the top of the DC bus, $h_a = 3$; if connected to node 1 (Fig. 2) $h_a = 2$ etc. Similarly, the rectifier pole voltages can be written as:

$$V_{uvwo} = H_{uvw} V_C \qquad (2)$$

$$\text{where } H_{uvw} = \begin{bmatrix} h_{u1} & h_{u2} & h_{u3} \\ h_{v1} & h_{v2} & h_{v3} \\ h_{w1} & h_{w2} & h_{w3} \end{bmatrix} \text{ and } V_{uvo} = \begin{bmatrix} v_{uo} \\ v_{vo} \\ v_{wo} \end{bmatrix}$$

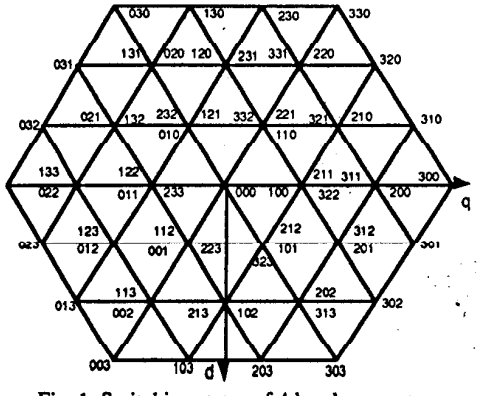

Fig. 1 Switching states of 4 level converter

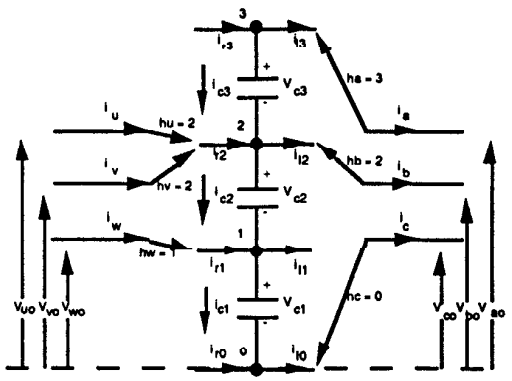

Fig. 2 Pole voltage and DC capacitor voltage

The rectifier switching functions are defined analogously to the inverter switching functions. Eqs. (1), (2) are written in terms of the capacitor voltages to bring out the explicit dependence of individual capacitor voltages on the switching functions chosen. Using duality, the dc currents can then be expressed as:

$$I_L = H_{abc}^T I_{abc} \qquad (3)$$

$$\text{where } I_{abc} = [i_a \quad i_b \quad i_c]^T; \; I_L = [i_{l1} \quad i_{l2} \quad i_{l3}]^T$$

$$I_R = H_{uvw}^T I_{uvw} \qquad (4)$$

$$\text{where } I_{uvw} = [i_u \quad i_v \quad i_w]^T; \; I_R = [i_{r1} \quad i_{r2} \quad i_{r3}]^T$$

The capacitor currents are then given by

$$i_{c3} = i_{r3} - i_{l3} \qquad (5.a)$$

$$i_{c2} = i_{r2} - i_{l2} + i_{c1} = i_{r2} + i_{r3} - (i_{l2} + i_{l3}) \qquad (5.b)$$

$$i_{c1} = i_{r1} - i_{l1} + i_{c2} = i_{r1} + i_{r2} + i_{r3} - (i_{l1} + i_{l2} + i_{l3}) \qquad (5.c)$$

Referring to Fig. 1, it can be observed that 6 vectors can be realized using 3 switching states each (2 redundancy), 12 vectors can be realized using 2 switching states each (1 redundancy) and 18 vectors can be realized by a unique switching state (0 redundancy). However, each switching state produces a unique set of capacitor charging currents. For example, inverter states (210) and (321) produce the same voltage vector (under balanced conditions) but while state (210) leads to $i_{c1} = i_c$, $i_{c2} = -i_a$, $i_{c3} = 0$, state (321) leads to $i_{c1} = 0$, $i_{c2} = -i_c$ and $i_{c3} = i_a$ (neglecting rectifier currents). Thus, the capacitor voltages are affected differently depending on the switching state chosen. It should also be noted that the two switching states (210) and (321) also produce different zero sequence voltages.

B. Control objective of proposed drive.

As stated earlier, the control of the integrated system is the most critical part of the drive. There are 3 primary objectives of the control strategy:

(i) The function of the inverter is primarily to supply the load with the required excitation so that the motor operation is optimized. This defines a modulation scheme on the inverter consistent with the load performance viz. constant V/f operation, current regulated PWM etc. The MLI has to be

capable of any or all of these standard modulation schemes. In case of a 3 level inverter, field oriented control and sine triangle PWM have been successfully implemented [7,8,12].

(ii) The rectifier serves primarily to maintain the required DC voltage for stable inverter operation. By using force commutated devices, the rectifier can be made to regulate the DC bus voltage and also generate unity power factor currents at the utility interface. In addition, the active rectifier also permits bi-directional real power flow, which allows a four quadrant operation of the drive. For this reason a 4 level inverter is used in the rectifying mode. Hysteresis current control has been demonstrated for a partially active 3 level rectifier in [6, 9].

(iii) The 4 level system has to be able to balance the DC capacitor voltages. In an MLI, the capacitor voltages tend to drift in the absence of explicit control which then degrades the rectifier, inverter and consequently the motor performance finally leading to a device failure or motor burnout. This is an additional constraint which was incorporated in the overall control strategy. Again, in case of 3 level drives, the DC voltage balancing has been adequately achieved from the inverter using lookup tables. [13] used a combination of common mode voltage modification of sine triangle PWM and lookup tables. Due to the large number of switching states, a lookup table approach becomes less feasible for higher number of levels.

Based on the control specification described above, a suitable control strategy has been devised which achieves the desired objectives. It is shown that DC voltage balancing can be achieved from the inverter or the rectifier or both depending on the load and bus conditions. The control strategy is completely dynamic and utilizes no lookup tables and capable of handling bi-directional real power flow.

C. Control of the 4 level drive.

C. i. Rectifier based voltage balancing.

Fig. 3 shows the overall schematic of the control scheme used. The rectifier is the means for effecting primary control of the DC bus voltage balancing and regulation. In addition, the rectifier is used to draw unity power factor currents from the utility. Of all the schemes available for realizing this end, a modified version of the hysteresis current control was devised. The rectifier currents are given by:

$$L_s \frac{d\bar{I}_{qds}}{dt} + R_s \bar{I}_{qds} = \bar{E}_{qds} - \bar{V}_{qds}(k) \qquad (6)$$

where L_s, R_s are system line inductance and resistance respectively, $\bar{I}_{qds} = I_{qs} - jI_{ds}$ is the line current vector in the stationary dq frame. Similarly, $\bar{E}_{qds} = E_{qs} - jE_{ds}$ is the utility phase voltage vector in the stationary reference frame and $\bar{V}_{qds}(k) = V_{qs}(k) - jV_{ds}(k)$ is the rectifier phase voltage with respect to the utility neutral. k is the index of the voltage vector that the rectifier can produce and corresponds to each node in the hexagon of Fig. 1. $(1 \le k \le 37)$ The utility phase voltages are assumed to form a balanced set and are given as:

$$E_{un} = E_m \cos(\omega t) \qquad (7.a)$$

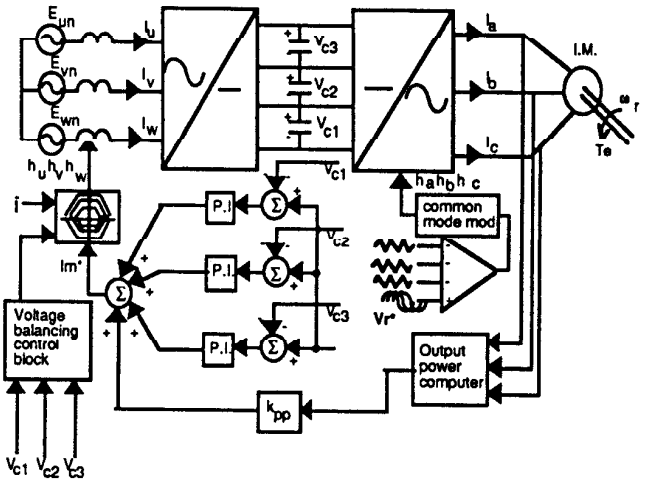

Fig. 3 Control scheme of 4 level drive system

$$E_{vn} = E_m \cos(\omega t - 2\pi/3) \qquad (7.b)$$

$$E_{wn} = E_m \cos(\omega t + 2\pi/3) \qquad (7.c)$$

Thus, $E_{qs} = E_m \cos(\omega t)$ and $E_{ds} = -E_m \sin(\omega t)$. Note that since the currents are always continuous, the rectifier phase voltages with respect to the utility neutral are related to the rectifier pole voltages as

$$V_{uvwn} = TV_{uvo} \qquad (8)$$

where $T = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix}$; $V_{uvwn} = [V_{un} \quad V_{vn} \quad V_{wn}]^T$

and the pole voltages are given by Eq. 2. Further, it can be observed that corresponding to each vector index k, there may be more than one constitutive switching states. The current error vector is governed by

$$L_s \frac{d\Delta\bar{I}_{qds}}{dt} + R_s \Delta\bar{I}_{qds} = \bar{V}(k) - \hat{E}_{qds} \qquad (9)$$

$$\text{where } \hat{E}_{qds} = \bar{E}_{qds} - R_s \bar{I}^*_{qds} - L_s \frac{d\bar{I}^*_{qds}}{dt}; \text{ and } \Delta\bar{I}_{qds} = \bar{I}^*_{qds} - \bar{I}_{qds}$$

The reference current is given by

$$\bar{I}^*_{qds} = I^*_m \cos(\omega t) + jI^*_m \sin(\omega t) \qquad (10)$$

where a reference magnitude I_m^* is multiplied by a sinusoidal template co-phasal with the utility phase voltages for unity power factor phase current references. The reference current magnitude I_m^* is derived from two sources:

(i) Each capacitor voltage is regulated by a PI loop. The output of all PI loops forms one part of the reference.

(ii) An inverter output power feedforward term provides the other part of the reference current. Therefore,

$$I^*_{m_1}(t) = \sum_{j=1}^{3} \alpha_j \left(k_p (V^*_{dc}/3 - V_{c_j}) + k_i \int_0^t (V^*_{dc}/3 - V_{c_j}) d\tau \right) \qquad (11)$$

$$I^*_m(t) = I^*_{m_1}(t) + k_{ff} P_{out}(t) \qquad (12)$$

Unequal values of the constants α_j in Eq. 11 serves to bias the reference in the direction of a particular capacitor voltage deviation. A value of $\alpha_j = 1$ was found to be satisfactory. An important consequence of combining the regulated outputs of the capacitor voltages in this manner is that the rectifier response to voltage deviations becomes more sluggish since the effect of a positive capacitor voltage deviation in Eq. 11 is canceled by a negative deviation of some other capacitor voltage. However, transient response is improved by the addition of the load feedforward term in the reference. In the steady state, the capacitor voltages are regulated to their nominal values. The phase current references are thus given as

$$i_u^* = I_m^* cos(\omega t) \quad i_v^* = I_m^* cos(\omega t - 2\pi/3) \quad i_w^* = I_m^* cos(\omega t + 2\pi/3)$$

In order to concurrently balance the DC link capacitor voltages and regulate utility phase currents, a modified hysteresis control method was devised to schedule the rectifier switching events. Fig. 4 shows the scheme implemented. Two tolerance bands are defined around the phase current reference. The inner band schedules a switching event of the rectifier when the rectifier control has to select a vector, $V(k)$, such that the resulting capacitor currents drive the voltage deviations to zero. If the same switching state can also drive the input current towards the reference, current regulation is also achieved. This scheme is implemented by first evaluating the resulting capacitor currents from Eqs. 3, 4, 5. A dead band of magnitude 2δ is introduced around the nominal capacitor voltages disabling the voltage balancing if all deviations are within tolerances. Thus,

$$\Delta V_{c_j} = V_{c_j} - V_{dc}^*/3 \qquad j = 1,2,3 \;\&\; if \;\; |V_{c_j} - V_{dc}^*/3| > \delta \quad (13)$$
$$= 0 \qquad \text{otherwise}$$

The desirability of choosing a state k, is determined by evaluating the incremental real power that would flow through each capacitor p_{cj} for state k.

$$p_{c_j}(k) = i_{c_j}(k) \times \Delta V_{c_j} \; ; \; j = 1,2,3 \quad (14)$$

A state k is ideal for balancing the voltages if it results in negative values of $p_{c1}(k)$, $p_{c2}(k)$ and $p_{c3}(k)$. For example, referring to Fig. 5, if $\Delta V_{c2} < -\delta$ and $\Delta V_{c3} > \delta$, $|\Delta V_{c1}| < \delta$, then voltages can be balanced if we could find a state such

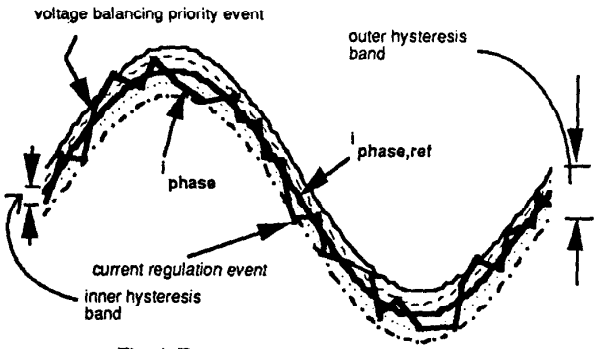

Fig. 4 Double hysteresis band regulation

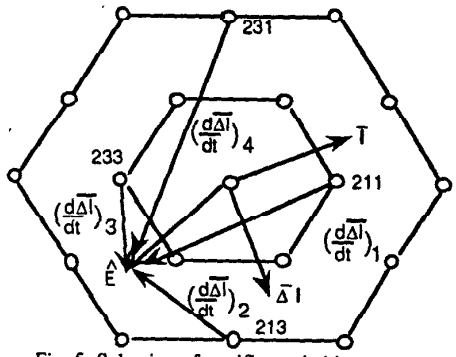

Fig. 5 Selection of rectifier switching states

that it produces a current $i_{c3} < 0$ and $i_{c2} > 0$. If $i_u > 0$, $i_v < 0$, $i_w < 0$, the switching state (213) and (231) will produce desirable capacitor currents. Also, state (211) and (233) will drive ΔV_{c2} and ΔV_{c3} respectively towards 0. Whether these states also regulate the input current can be determined by evaluating the dot product $Real\{(\Delta\bar{I}_{qds})^*(\bar{V}(k) - \hat{E}_{qds})\}$. A negative dot product would result in the selection of a state which not only regulates input currents but also drives the capacitor voltages towards their nominal values. If no such state is found, that state is chosen which minimizes the maximum of the individual capacitor voltage deviations. In this case, states (213) or (233) can be chosen.

It was found that most state selections occur in the innermost hexagon because it guarantees that at least one capacitor voltage deviation is minimized. If the DC bus voltage is relatively low, none of the vectors in the innermost hexagons may reduce the current error. To achieve current regulation, an outer hysteresis band regulation scheme is imposed. This band is wider than the inner band and rectifier switching is initiated when an intersection of a phase current with the outer band occurs. In this case, driving the current error vector to the origin is the priority. Of the states so identified by this requirement (again found by evaluating the dot product), those states are chosen which minimize the deviations. It was observed that the most optimum regulation occurred when the outermost 6 states (300), (330), (030), (033), (003) or (303) were chosen since each of these states have the following two properties:

(i) Resulting capacitor charging currents and consequent capacitor voltage deviations produced by the rectifier are the same for each capacitor.

(ii) The magnitude of the voltage developed by the rectifier is the maximum, so these have the maximum effect on driving the current error vector to the origin.

C. ii. Inverter modulation.

Open loop synchronous sine triangle PWM based on [14], was used on the inverter to drive the induction motor. Fig. 6 shows the carrier waves and the phase voltage reference. All the carrier waves are in phase with each other and phase A reference voltage. The switching functions are determined by the comparators which compare the phase reference with the

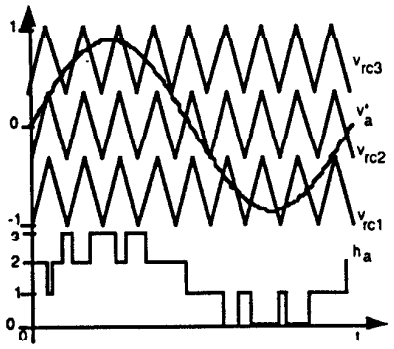

Fig. 6 Four level sine triangle PWM

carrier waves. For example inverter phase A switching function is determined according to

$$\begin{aligned} h_a &= 0 \quad \text{if } v_a^* < v_{rc1} \\ &= 1 \quad \text{if } v_{rc1} \le v_a^* < v_{rc1} \\ &= 2 \quad \text{if } v_{rc2} \le v_a^* < v_{rc3} \\ &= 3 \quad \text{otherwise} \end{aligned} \tag{15}$$

From Fig. 6, it is evident that the intersection of the reference with each triangle carrier wave corresponds to modulation across the corresponding capacitor. Note that pulse dropping occurs for $m_a > 1.0$. The modulation depth has a significant impact on the DC voltage balancing strategy. For $m_a < 1.0$, the innermost capacitor C_2 tends to discharge rapidly whereas the outer capacitors C_1 and C_3 uniformly charge up when the rectifier is used to regulate the DC bus voltage since $\Delta V_{c1} + \Delta V_{c2} + \Delta V_{c3} \approx 0$. So, $i_{c2,avg} \approx -(i_{c1avg} + i_{c3avg})$. By symmetry, the outer capacitors have the same polarity of charging currents and the inner capacitor current has the opposite polarity.

In sine triangle PWM, if the phase reference voltages are shifted relative to the carrier waves by the subtraction or addition of a common mode voltage, the relative polarity of the capacitor currents can be changed since the switching functions are modified (Eq. 15). This is illustrated by the control block shown in Fig. 7. Suppose the load current vector is such that $i_a > 0$, $i_b < 0$, $i_c > 0$; the capacitor voltage deviations are $\Delta V_{c1} > \delta$, $\Delta V_{c2} < \delta$ and $\Delta V_{c3} > \delta$ and the sine triangle comparator yields (211). Then, the output of the common mode voltage modulation block is (100) if $\Delta V_{c1} > \Delta V_{c3}$ and (322) otherwise. This modulation offers a consistent way of selecting the right redundant states which charge the DC link capacitors appropriately.

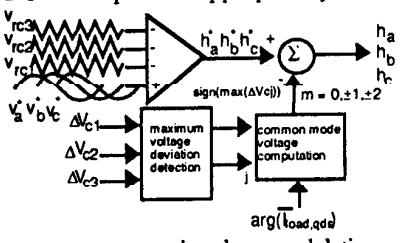

Fig. 7 Inverter common mode voltage modulation scheme

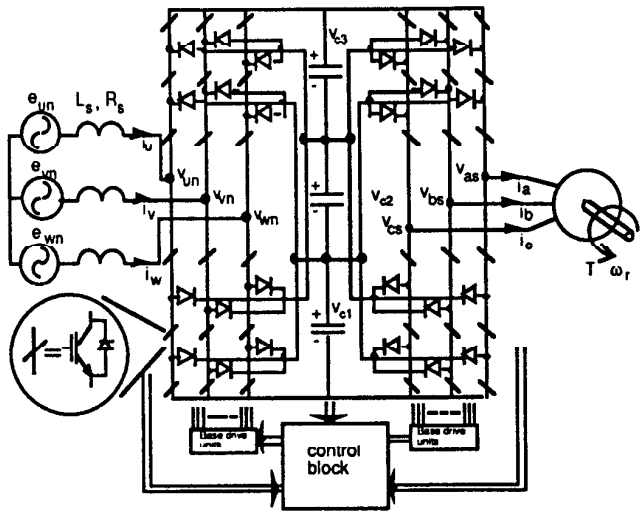

Fig. 8 Simulated four level rectifier inverter drive system

III. SIMULATION RESULTS

A typical induction motor drive was configured as shown in Fig. 8. The rectifier and inverter are fully controllable 4 level converters (shown using IGBTs). The load is a 3 phase, wye connected 100 HP induction motor with rated parameters given below :

$P = 100\ HP$ $\quad N_{pole} = 4$
$V = 460\ (line, rms)$ $\quad r_1 = .01\ pu$ $\quad x_1 = 0.1\ pu,$
$x_m = 3.0\ pu$ $\quad x_2 = 0.1\ pu$ $\quad r_2 = .015pu$
Utility : *460 V* (line, rms) , *120 kVA, 6 % impedance*
Series inductance : *1.5 mH/phase*
Inverter carrier frequency $f_c = 1620\ Hz$

In the first case, the DC bus was regulated at 1200 V and the inverter modulation index, $m_a = 0.6$. This corresponds approximately to the rated conditions on the induction motor. The motor provides the rated torque to a fan load. Fig. 9 shows the motor phase voltage and current under these conditions. The phase voltage THD was found to be 19.7%

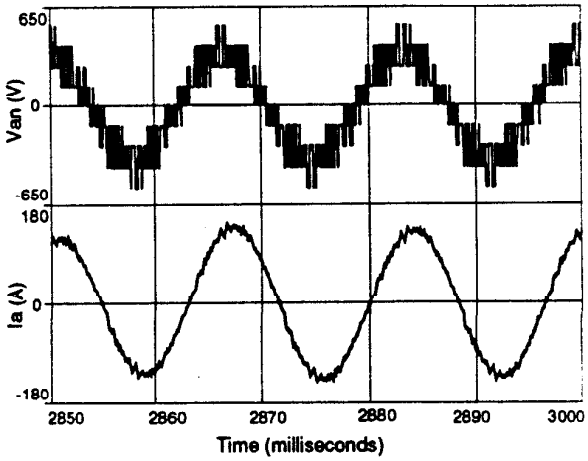

Fig. 9 Motor phase voltage and current (unsat. inverter)

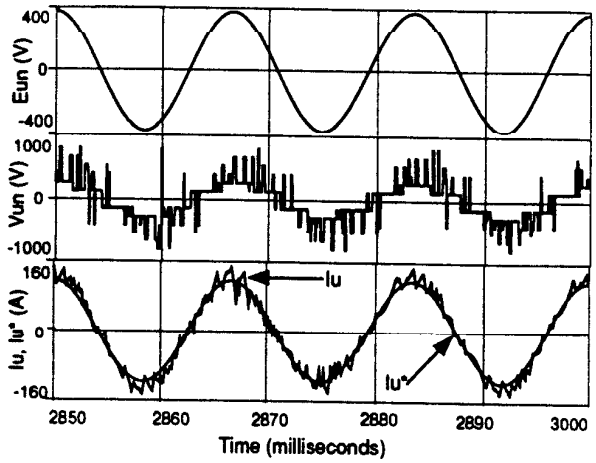

Fig. 10 Rectifier unity power factor operation (unsat. inverter)

but the phase current THD was only about 8%. Fig. 10 shows the rectifier unity power factor operation. The phase current THD was calculated as 9.3%. The mean rectifier switching frequency was approximately 1.4 kHz for a hysteresis band of 10 A.

Fig. 11 shows the DC bus voltages obtained for this operating condition (bus capacitance C_{dc} = 9 mF). The DC voltages are regulated efficiently around their nominal values. The corresponding capacitor currents and voltages are shown Fig. 12 and 13 respectively. In the steady state, $V_{c2,avg} < V_{c1,avg}, V_{c3,avg}$. Balancing is generally achieved by regulating $i_{c2,rms}$ to be less than $i_{c1,rms}$ and $i_{c3,rms}$. The common mode voltage modulation for reducing $i_{c2,rms}$ can be seen in Fig. 14. When ΔV_{c1} became > δ, the inverter selects a redundant state to minimize the deviation in ΔV_{c1}. This is reflected by the fact that stays bounded below about 405 V. Due to the the voltage drift, selection of a redundant state also results in a change in the applied motor phase voltage, leading to a change in phase current. A change in the value of $i_{c2,rms}$ is seen in Fig. 12 when common mode modulation occurs.

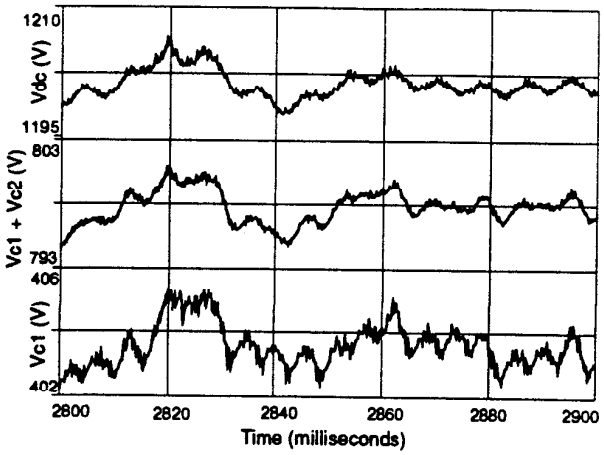

Fig. 11 DC bus voltages (unsaturated inverter)

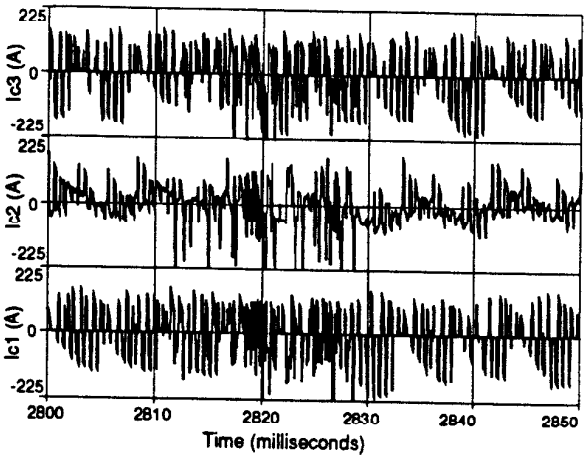

Fig. 12 Capacitor currents for unsaturated inverter operation

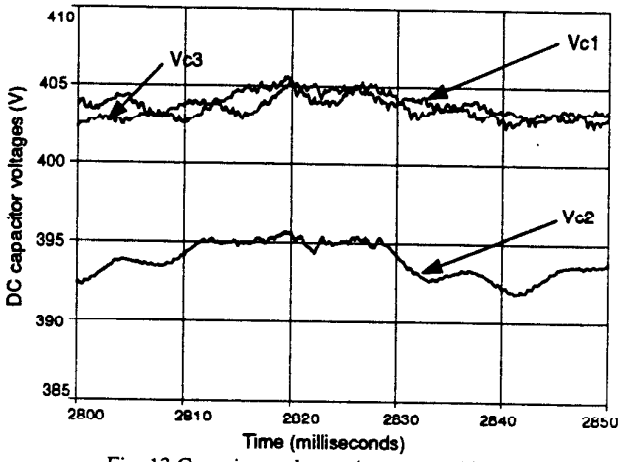

Fig. 13 Capacitor voltages (unsaturated inverter)

The next set of simulations are for the saturated inverter (m_a = 4.0) with the DC bus voltage regulated at 900 V so as to still produce rated torque. The motor phase voltage and current (THD = 37%) are shown in Fig. 15. Unity power

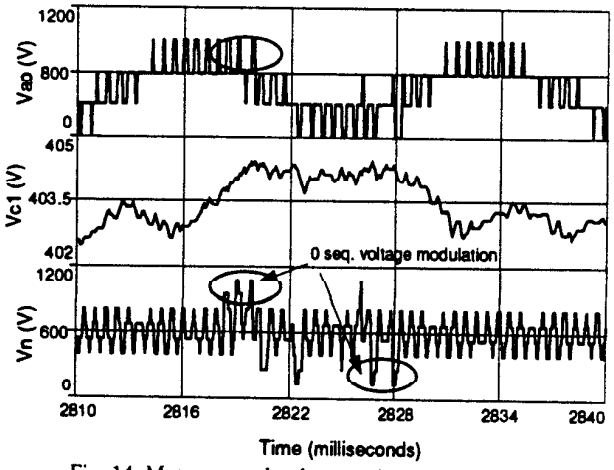

Fig. 14 Motor neutral voltage and phase A pole voltage

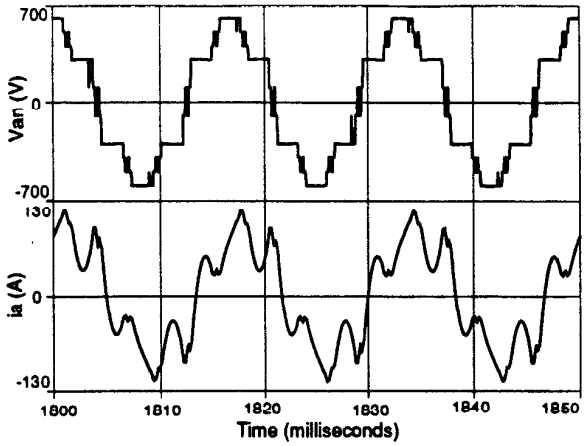

Fig. 15 Motor phase voltage and current (saturated inverter)

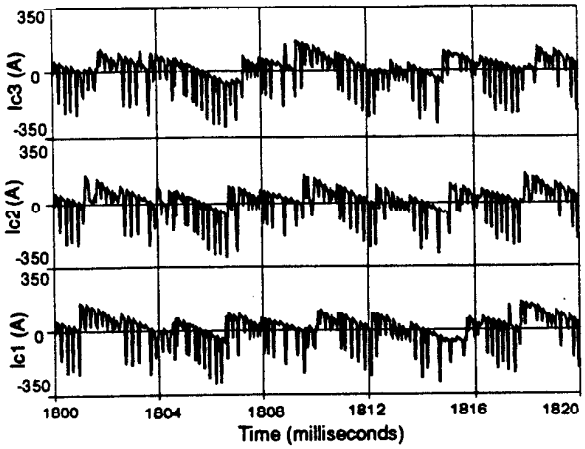

Fig. 18 Capacitor currents (saturated inverter)

factor operation of the rectifier is still maintained as shown in Fig. 16. The input current THD was about 7%. However, the rectifier average switching frequency was higher (2.5 kHz) than the unsaturated inverter case because the rectifier has to balance the DC voltages alone - so the double band hysteresis switching scheme results in more switching events. Fig. 17 shows the DC bus voltages in this case to be effectively regulated by the rectifier alone. For higher modulation indices, the capacitor currents (produced by the inverter) are symmetrical and so the capacitor voltage deviations are of similar polarity and magnitude. This considerably simplifies the voltage balancing scheme.

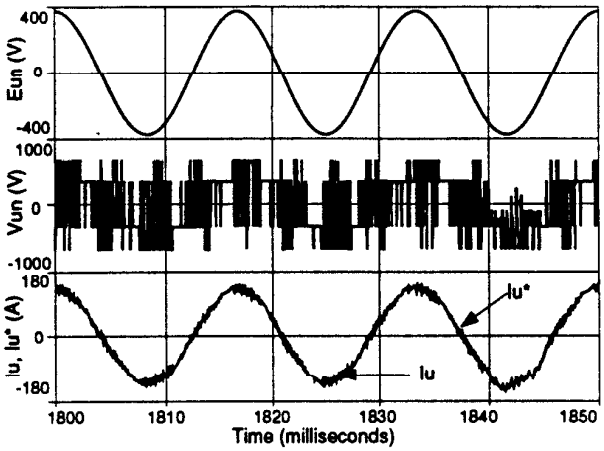

Fig. 16 Rectifier unity power factor operation (saturated inverter)

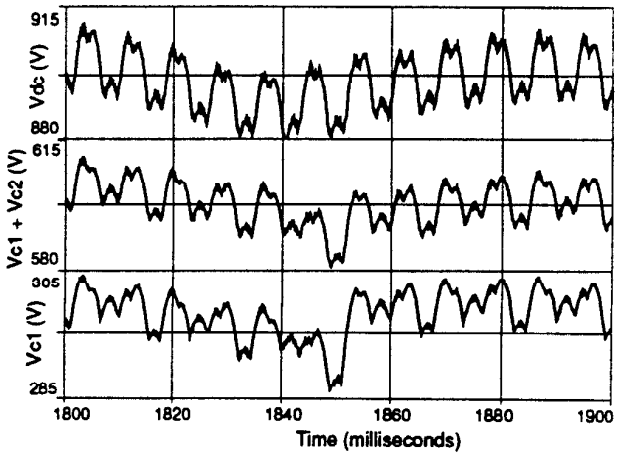

Fig. 17 DC bus voltages (saturated inverter)

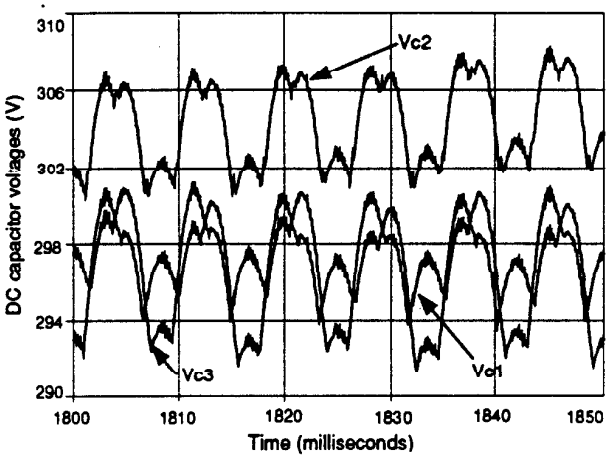

Fig. 19 Capacitor voltages (saturated inverter)

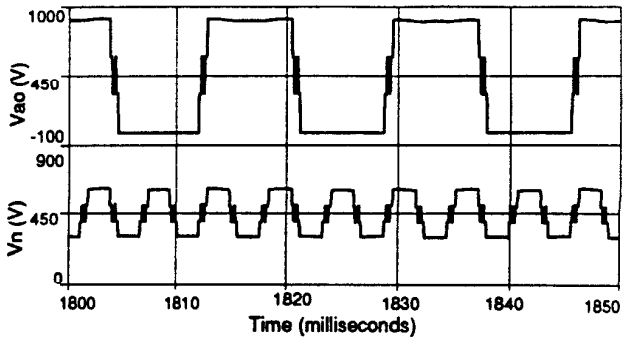

Fig. 20 Motor neutral voltage and phase A pole voltage

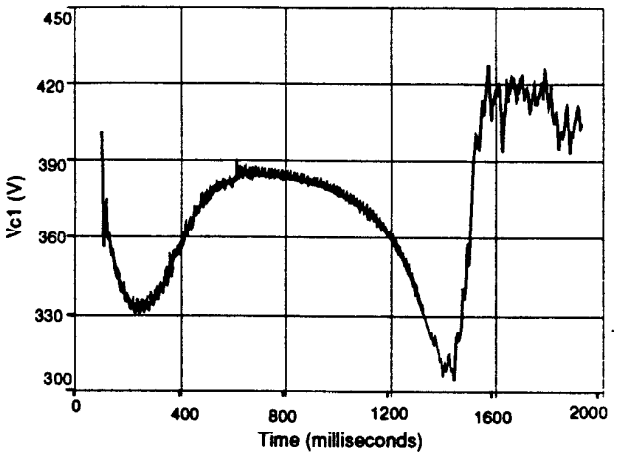

Fig. 21 Capacitor voltage V_{c1} during motor startup

Capacitor currents and voltages for this case can be seen in Fig. 18 and 19 respectively. As in the unsaturated case, $V_{c2,avg} < V_{c1,avg}, V_{c3,avg}$. The capacitor currents have the same shape and approximate rms values, leading to better voltage balancing. In contrast to the unsaturated inverter case, the motor neutral voltage does not display any common mode voltage regulation as seen in Fig. 20. In this case, only 0 redundancy vectors are chosen and so voltage balancing from the inverter cannot be effected. It is pertinent to point out that the control method described is robust enough to handle very large voltage deviations as seen in Fig. 21 where capacitor voltage V_{c1} is traced for a motor startup condition. Real power flows from the inverter to the DC link capacitors as the motor reaches its equilibrium speed, so increasing the DC capacitor voltages. The rectifier based voltage balancing scheme is able to transfer this real power to the utility from the DC bus thereby regulating the DC capacitor voltages.

IV. CONCLUSIONS

From the preceding analysis and simulation results, it can be concluded that a four level rectifier-inverter drive system can be satisfactorily controlled. It has been shown that the control algorithm is capable of simultaneously balancing the capacitor voltages and generating unity power factor currents at the input independently of the inverter operation. Since the inverter may be required only to switch between redundant states of a vector, its operation is unconstrained. The control method can be modified to optimize either the rectifier or inverter switching frequency or the DC capacitance. There is no direct coupling between the inverter and the rectifier voltage balancing algorithms. The voltage balancing works for bi-directional real power flow.

The DC capacitors used can be made even smaller with the availability of faster IGBTs which permit higher switching frequencies. The viability of a 4 level drive will depend on the tradeoffs between the cost and the performance which in turn depends on the application. For large motor loads, the multilevel voltage waveforms are an undeniable advantage. The unity power factor operation of the rectifier substantially mitigates the harmonic injection problem. Further, using devices of lower ratings, a 4 level inverter can satisfactorily drive loads requiring higher voltages. The strategy outlined adequately addresses the DC voltage balancing problem and serves to make the control of a four level drive more tractable, thus improving its viability.

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