A Four-Level Rectifier-Inverter System for Drive Applications

Gautam Sinha and Thomas A. Lipo

Multilevel converters are based on the neutral point clamped inverter topology proposed by Nabae et al. [1]. Subsequently, Bhagwat and Stefanovic [2] demonstrated the possible advantages of a multilevel converter topology. However, by using dc power supplies (i.e., batteries), voltage balancing of the dc link capacitors was not demonstrated for possible drive applications. Three distinct topologies have been proposed so far to realize the multilevel inverter (MLI) [3, 4], viz., the diode clamped MLI, the "flying capacitor" MLI, and MLIs with separate dc sources. So far, attention has been largely restricted to high-power, high-voltage applications such as static var compensation [5] in which the voltage balancing of the dc capacitors is less difficult.

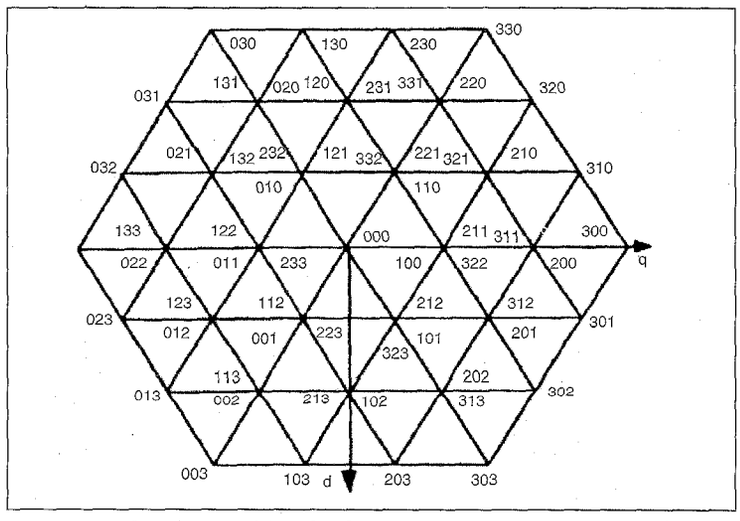

Fig. 1. Switching states of four-level converter.

This article appeared in its original form in the proceedings of the 1996 IAS Annual Meeting in San Diego. *Sinha, an IEEE Student Member, and Lipo, an IEEE Fellow, are with the University of Wisconsin in Madison. Both are IAS Members.*

However, recently a three-level rectifier-inverter drive system was investigated in [6, 7, 8], and a partially active three-level rectifier topology was proposed in [9].

Based on overall kVA ratings, the device count and ratings of the three topologies, the diode clamped topology is most suitable for drive applications and is the only topology discussed further. An n level diode clamped inverter is characterized by n distinct pole voltage levels and $2n$-2 switches per phase. Also, the n level inverter has $1 + 3n(n-1)$ nominally distinct voltage vectors. The large number of voltage vectors is a significant advantage in regulation and control schemes.

MLIs have a significant distinguishing feature—most voltage vectors in an n level inverter have one or more constitutive switching states for a total of n^3 states for a three-phase inverter. Therefore, an n level inverter has one vector of $(n-1)$ redundancy, six vectors of $(n-1)$ redundancy, 12 vectors of $(n-2)$ redundant states, etc. The large number of switching states offers a potential means for balancing the dc capacitor voltages and minimizing switching frequency.

Multilevel converters offer several advantages over the conventional two-level converters: (i) An increased number of voltage levels leads to better voltage waveforms and reduced voltage total harmonic distortion (THD). (ii) Switching dv/dt stresses are reduced. This is advantageous for reducing some of the electromagnetic interference (EMI) problems. (iii) Higher voltage levels can be attained by using devices of lower ratings. The diode circuits in this case clamp the voltages across each switch.

The primary disadvantage of an MLI is the increased overall kVA rating due to large device count. However, for a given rated utility and load voltages, the kVA rating of the MLI is much less than the kVA rating of the inverter obtained by scaling a two-level inverter to the corresponding number of levels. Devices of lower current ratings can be used in each phase at the pole extremities.

1077-2618/98/$10.00©1998 IEEE

For large drives, the higher voltages translate to a reduction in current ratings, which is highly desirable since it leads directly to cost savings.

MLIs have an additional problem with voltage balancing of the dc bus capacitors. In the absence of an explicit control strategy, the capacitor voltages in an MLI topology tend to deviate from their nominal rated values. Typically, the dc capacitor voltages can be balanced by using the redundant states. This approach has so far been incorporated in a three-level drive control largely by the use of lookup tables. As compared to a two level inverter, the MLI control is more complex. Reducing the control complexity would clearly serve to make the MLI-based drive more feasible.

A drive environment is substantially different from a static var compensation application of an MLI. Whereas in static var compensation, only reactive power flows between the converter and the system, in a motor drive, the converters must be able to handle bidirectional real power flow. So far, dc voltage balancing has not been satisfactorily discussed for the case when real power is drawn from the inverter. This article addresses the control issues involved in a drive application. The dc capacitor voltages are balanced for both motoring and regenerating modes of the inverter-motor system. In addition, dc voltages can be balanced even during motor startup with the associated large overcurrents.

A Four-Level Inverter-Based Motor Drive

The Four-Level Inverter

As stated earlier, the n level inverter is characterized by a large number of voltage vectors and switching states. In particular, a four-level inverter has 37 nominally distinct voltage vectors and 64 switching states. These vectors and switching states are represented in the dq plane as shown in Fig. 1. The relative locations of the voltage vectors and the switching states play a significant role in the control scheme employed. Fig. 2 illustrates the rectifier, inverter pole voltage, dc capacitor voltage, and current nomenclature. The inverter switching state shown is (h_a = 3, h_b = 2, h_c = 0), which results in pole voltages given as $V_{ao} = V_{C1} + V_{C2} + V_{C3}$; $V_{bo} = V_{C1} + V_{C2}$; $V_{co} = 0$. More compactly, the inverter pole voltages can be written in terms of switching functions as:

$$V_{abco} = H_{abc} V_C \; ; \; V_C = \begin{bmatrix} V_{c1} & V_{c2} & V_{c3} \end{bmatrix}^T \qquad (1)$$

$$H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} \\ h_{b1} & h_{b2} & h_{b3} \\ h_{c1} & h_{c2} & h_{c3} \end{bmatrix}; \quad V_{abco} = \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix};$$

$$h_{a1} = \delta(h_a - 1) + \delta(h_a - 2) + \delta(h_a - 3)$$

$$h_{a2} = \delta(h_a - 2) + \delta(h_a - 3); \; h_{a3} = \delta(h_a - 3); \; h_a = 0,1,2,3$$

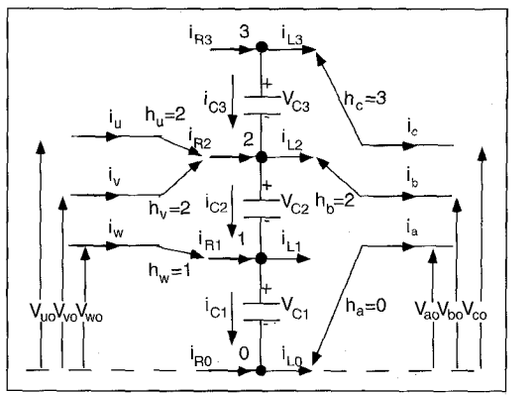

Fig. 2. Pole voltage and dc capacitor voltage.

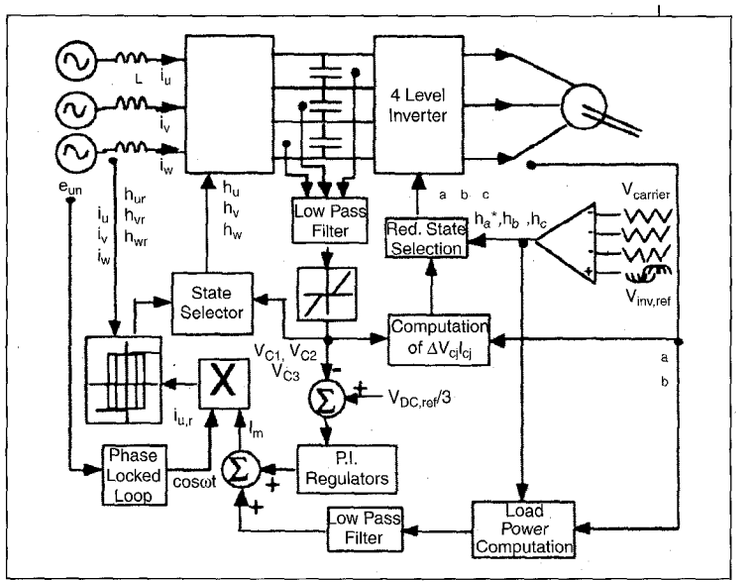

Fig. 3 Control scheme of four-level drive system.

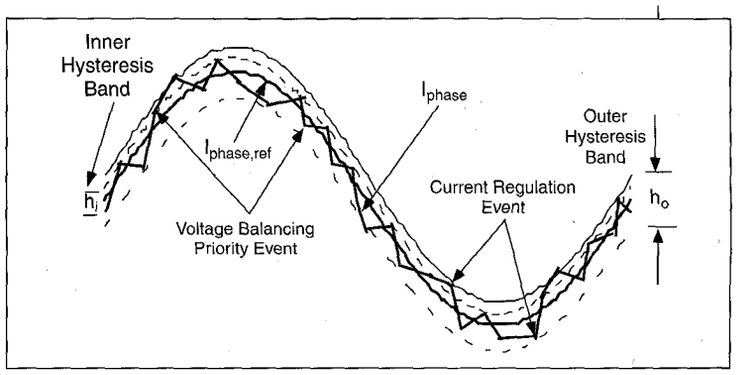

Fig. 4. Double hysteresis band regulation.

Here, h_a is the inverter phase A switching function and $\delta(x)$ is the delta function defined as:

$$\delta(x) = 1 \text{ if } x = 0; \; \delta(x) = 0 \text{ if } x \neq 0$$

Thus, if phase A is connected to the top of the dc bus, h_a = 3; if connected to node 1 (Fig. 2) h_a = 2,

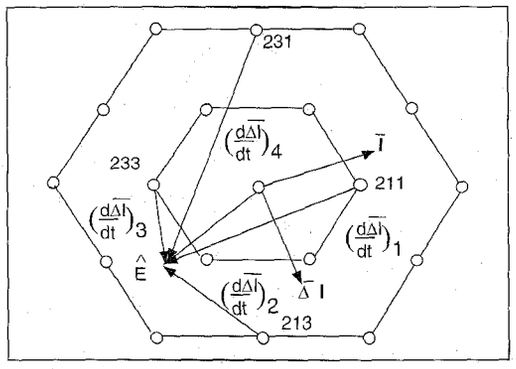

Fig. 5. Selection of rectifier switching states.

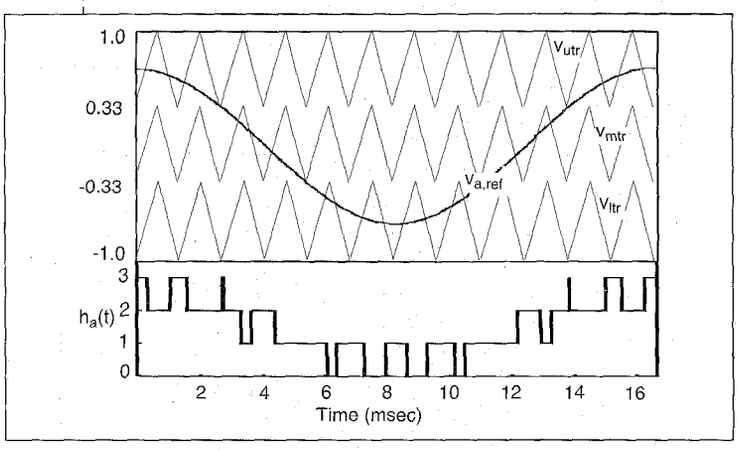

Fig. 6. Four level sine triangle PWM.

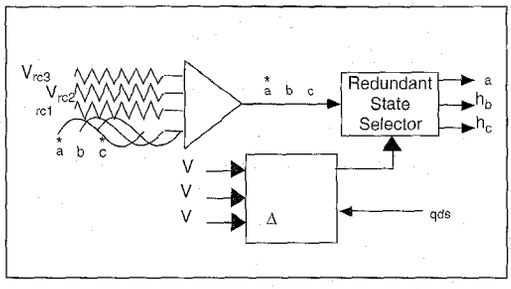

Fig. 7. Inverter common mode voltage modulation scheme.

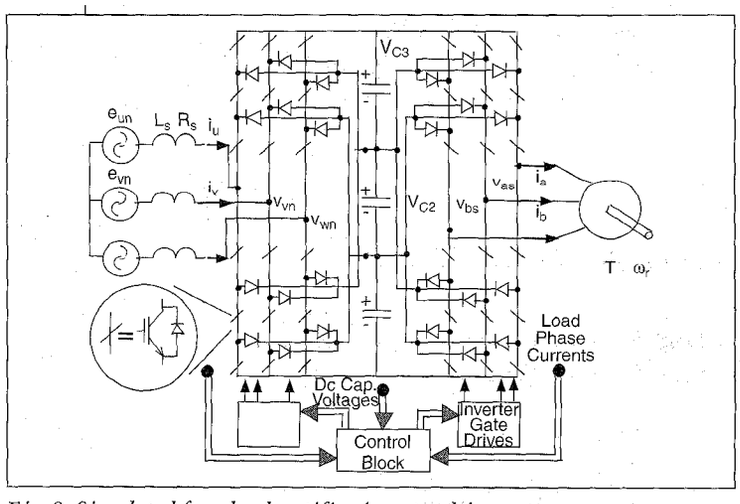

Fig. 8. Simulated four-level rectifier-inverter drive system.

etc. Similarly, the rectifier pole voltages can be written as:

$$V_{uvwo} = H_{uvw} VC \tag{2}$$

where $H_{uvw} = \begin{bmatrix} h_{u1} & h_{u2} & h_{u3} \\ h_{v1} & h_{v2} & h_{v3} \\ h_{w1} & h_{w2} & h_{w3} \end{bmatrix}$ and $V_{uvo} = \begin{bmatrix} v_{uo} \\ v_{vo} \\ v_{wo} \end{bmatrix}$

The rectifier switching functions are defined analogously to the inverter switching functions. Equations (1), (2) are written in terms of the capacitor voltages to bring out the explicit dependence of individual capacitor voltages on the switching functions chosen. The dc currents can then be expressed as:

$$I_L = H_{abc}^T I_{abc} \tag{3}$$

where

$$I_{abc} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T ; I_L = \begin{bmatrix} i_{l1} & i_{l2} & i_{l3} \end{bmatrix}^T$$

$$I_R = H_{uvw}^T I_{uvw} \tag{4}$$

where

$$I_{uvw} = \begin{bmatrix} i_u & i_v & i_w \end{bmatrix}^T ; I_R = \begin{bmatrix} i_{r1} & i_{r2} & i_{r3} \end{bmatrix}^T$$

The capacitor currents are then given by

$$ic3 = ir3 - il3 \tag{5.a}$$

$$ic2 = ir2 - il2 + ic1 = ir2 + ir3 - (il2 + il3) \tag{5.b}$$

$$ic1 = ir1 - il1 + ic2 = ir1 + ir2 + ir3 - (il1 + il2 + il3) \tag{5.c}$$

Referring to Fig. 1, it can be observed that six vectors can be realized using three switching states each (2 redundancy), 12 vectors can be realized using two switching states each (1 redundancy) and 18 vectors can be realized by a unique switching state (0 redundancy). However, each switching state produces a unique set of capacitor charging currents. For example, inverter states (210) and (321) produce the same voltage vector (under balanced conditions) but while state (210) leads to $i_{C1} = i_c$, $i_{C2} = -i_a$, $i_{C3} = 0$, state (321) leads to $i_{C1} = 0$, $i_{C2} = -i_c$ and $i_{C3} = i_a$ (neglecting rectifier currents). Thus, the capacitor voltages are affected differently depending on the switching state chosen. It should also be noted that the two switching states (210) and (321) also produce different zero sequence voltages.

Control Objective of Proposed Drive

As stated earlier, the control of the integrated system is the most critical part of the drive. There are three primary objectives of the control strategy:

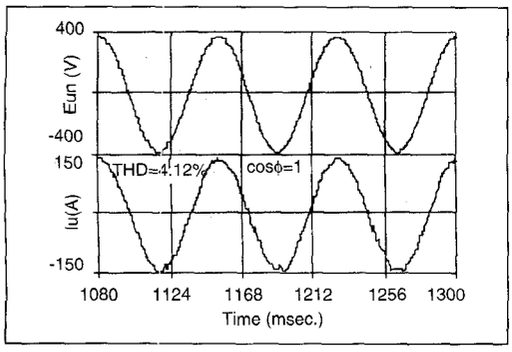

Fig. 9. Motor phase voltage and current (unsaturated inverter).

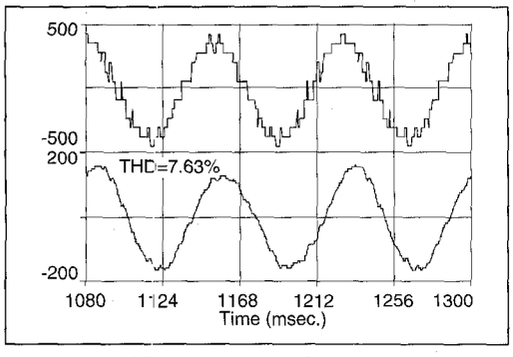

Fig. 10. Rectifier unity power factor operation (unsaturated inverter).

(i) The function of the inverter is primarily to supply the load with the required excitation so that the motor operation is optimized. This defines a modulation scheme on the inverter consistent with the load performance, viz., constant V/f operation, current regulated PWM, etc. The MLI has to be capable of any or all of these standard modulation schemes. In case of a three-level inverter, field-oriented control and sine triangle PWM have been successfully implemented [6, 7, 8].

(ii) The rectifier serves primarily to maintain the required dc voltage for stable inverter operation. By using force-commutated devices, the rectifier can be made to regulate the dc bus voltage and also generate unity power factor currents at the utility interface. In addition, the active rectifier also permits bidirectional real power flow, which allows a four-quadrant operation of the drive. For this reason, a four-level inverter is used in the rectifying mode. Hysteresis current control has been demonstrated for a partially active three-level rectifier in [6, 9].

(iii) The four-level system has to be able to balance the dc capacitor voltages. In an MLI, the capacitor voltages tend to drift in the absence of explicit control, which then degrades the rectifier, inverter, and consequently the motor performance, finally leading to a device failure or motor burnout. This is an additional constraint which was incorporated in the overall control strategy. Again, in case of three-level drives, the dc voltage balancing has

The control of the integrated system is the most critical part of the drive.

been adequately achieved from the inverter using lookup tables. Reference [10] used a combination of common mode voltage modification of sine triangle PWM and lookup tables. A five-level inverter using separate dc sources with an induction motor load has been demonstrated [12]. Sine triangle PWM of a four-level inverter, but with a dc voltage source across the dc bus, has been demonstrated for limited modulation depths [14].

Based on the control specification described above, a suitable control strategy has been devised which achieves the desired objectives. It is shown that dc voltage balancing can be achieved from the inverter or the rectifier or both depending on the load and bus conditions. The control strategy is completely dynamic, utilizes no lookup tables, and is capable of handling bidirectional real power flow.

Control of the Four-Level Drive

Rectifier-based voltage balancing. Fig. 3 shows the overall schematic of the control scheme used. The rectifier is the means for effecting primary control of the dc bus voltage balancing and regulation. In addition, the rectifier is used to draw unity power factor currents from the utility. Of all the schemes available for realizing this end, a modified version of the hysteresis current control was devised. The rectifier currents are given by

$$L_s \frac{d\bar{I}_{qds}}{dt} + R_s \bar{I}_{qds} = \bar{E}_{qds} - \bar{V}_{qds}(k) \qquad (6)$$

where L_S, R_S are system line inductance and resistance, respectively, and $\bar{I}_{qds} = I_{qs} - jI_{ds}$ is the line current vector in the stationary dq frame. Similarly, $\bar{E}_{qds} = E_{qs} - jE_{ds}$ is the utility phase voltage vector in the stationary reference frame and

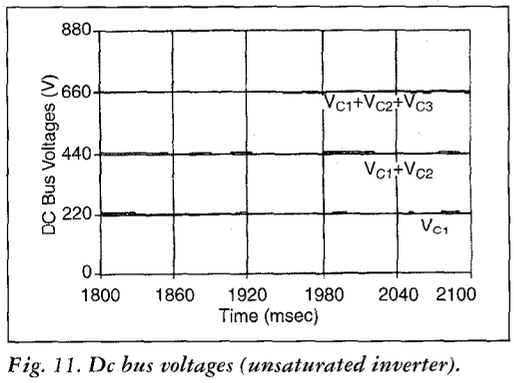

Fig. 11. Dc bus voltages (unsaturated inverter).

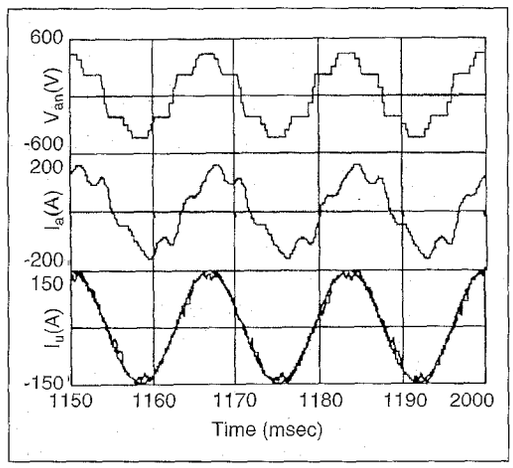

Fig. 12. Motor phase voltage and current and input rectifier phase current at saturated inverter operation at 60 Hz.

$\bar{V}_{qds}(k) = V_{qs}(k) - jV_{ds}(k)$ is the rectifier phase voltage with respect to the utility neutral. k is the index of the voltage vector that the rectifier can produce and corresponds to each node in the hexagon of Fig. 1 ($1 \le k \le 37$). The utility phase voltages are assumed to form a balanced set and are given as:

$$E_{un} = E_m \cos(\omega t) \tag{7.a}$$

$$E_{vn} = E_m \cos(\omega t - 2\pi/3) \tag{7.b}$$

$$E_{wn} = E_m \cos(\omega t + 2\pi/3) \tag{7.c}$$

Thus, $E_{qs} = E_m \cos(\omega t)$ and $E_{ds} = -E_m \sin(\omega t)$. Note that since the currents are always continuous, the rectifier phase voltages with respect to the utility neutral are related to the rectifier pole voltages as:

$$V_{uvwn} = TV_{uvo} \tag{8}$$

where

$$T = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix};$$

$$V_{uvwn} = \begin{bmatrix} V_{un} & V_{vn} & V_{wn} \end{bmatrix}^T$$

and the pole voltages are given by (2). Further, it can be observed that corresponding to each vector index k, there may be more than one constitutive switching states. The current error vector is governed by:

$$L_s \frac{d\Delta\bar{I}_{qds}}{dt} + R_s \Delta\bar{I}_{qds} = \bar{V}(k) - \bar{E}^*_{qds} \tag{9}$$

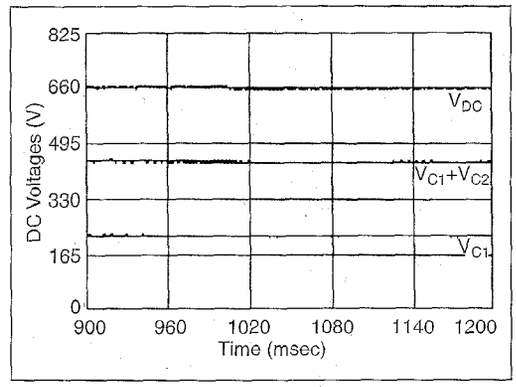

Fig. 13. dc bus voltages for saturated inverter operation.

where $\bar{E}^*_{qds} = \bar{E}_{qds} - R_s \bar{I}^*_{qds} - L_s \frac{d\bar{I}^*_{qds}}{dt}$; and $\Delta\bar{I}_{qds} = \bar{I}^*_{qds} - \bar{I}_{qds}$

The reference current is given by

$$\bar{I}^*_{qds} = I^*_m \cos(\omega t) + jI^*_m \sin(\omega t) \tag{10}$$

where a reference magnitude I_m^* is multiplied by a sinusoidal template co-phasal with the utility phase voltages for unity power factor phase current references. The reference current magnitude I_m^* is derived from two sources:

(i) Each capacitor voltage is regulated by a PI loop. The output of all PI loops forms one part of the reference.

(ii) An inverter output power feedforward term provides the other part of the reference current. Therefore:

$$I^*_{m_1}(t) = \sum_{j=1}^{3} \alpha_j \left(\begin{array}{l} k_p \left(V^*_{dc}/3 - V_{c_j} \right) \\ + k_i \int_0^t \left(V^*_{dc}/3 - V_{c_j} \right) d\tau \end{array} \right) \tag{11}$$

$$I^*_m(t) = I^*_{m_1}(t) + k_{ff} P_{out}(t) \tag{12}$$

Unequal values of the constants α_j in Equation 11 serves to bias the reference in the direction of a particular capacitor voltage deviation. A value of $\alpha_j = 1$ was found to be satisfactory. An important consequence of combining the regulated outputs of the capacitor voltages in this manner is that the rectifier response to voltage deviations becomes more sluggish since the effect of a positive capacitor voltage deviation in Equation 11 is canceled by a negative deviation of some other capacitor voltage. However, transient response is improved by the addition of the load feedforward term in the reference. In the steady state, the capacitor voltages are regulated to their nominal values. Thus, the phase current references are $i^*_u = I^*_m \cos(\omega t)$,

Most state selections occur in the innermost hexagon because it guarantees that at least one capacitor voltage deviation is minimized.

$i_v^* I_m^* \cos(\omega t - 2\pi/3)$, and
$i_w^* = I_m^* \cos(\omega t + 2\pi/3)$.

In order to concurrently balance the dc link capacitor voltages and regulate utility phase currents, a modified hysteresis control method was devised to schedule the rectifier switching events shown schematically in Fig. 4. Two tolerance bands are defined around the phase current reference. The inner band schedules a switching event of the rectifier when the rectifier control has to select a vector, $V(k)$, such that the resulting capacitor currents drive the voltage deviations to zero. If the same switching state can also drive the input current toward the reference, current regulation is also achieved. This scheme is implemented by first evaluating the resulting capacitor currents from Equations 3, 4, 5. A dead band of magnitude 2δ is introduced around the nominal capacitor voltages, disabling the voltage balancing if all deviations are within tolerances. Thus,

$$\Delta V_{c_j} = V_{c_j} - V_{dc}^*/3 \qquad (13)$$
$$j = 1,2,3 \;\&\; if \left| V_{c_j} - V_{dc}^*/3 \right| > \delta$$

The desirability of choosing a state k is determined by evaluating the incremental real power that would flow through each capacitor p_{cj} for state k.

$$p_{c_j}(k) - i_{c_j}(k) \times \Delta V_{c_j};\; j = 1,2,3 \qquad (14)$$

A state (h_a, h_b, h_c) with index k is ideal for balancing the voltages if it results in negative values of $p_{c1}(k)$, $p_{c2}(k)$, and $p_{c3}(k)$. For example, referring to Fig. 5, if $\Delta V_{C2} < -\delta$ and $\Delta V_{C3} > \delta$, $|\Delta V_{C1}| < \delta$, then voltages can be balanced if we could find a state such that it produces a current $i_{C3} < 0$ and $i_{C2} > 0$. If $i_u > 0, i_v < 0, i_w < 0$, the switching state (213) and (231) will produce desirable capacitor currents. Also, state (211) and (233) will drive ΔV_{C2} and ΔV_{C3} respectively toward 0. Whether these states also regulate the input current can be determined by evaluating the dot product $\mathrm{Re}\left\{\left(\Delta \bar{I}_{qds}\right)^* \left(\bar{V}(k) - \bar{E}_{qds}^*\right)\right\}$. A negative dot product results in the selection of a state that not only regulates input currents but also drives the capacitor voltages toward their nominal values. If no such state is found, that state is chosen that minimizes the maximum capacitor voltage deviation. In this case, states (213) or (233) can be chosen.

It was found that most state selections occur in the innermost hexagon because it guarantees that at least one capacitor voltage deviation is minimized. If the dc bus voltage is relatively low, none of the vectors in the innermost hexagons may reduce the current error. To achieve current regulation, an outer hysteresis band regulation scheme is imposed. This band is wider than the inner band, and rectifier switching is initiated when an intersection of a phase current with the outer band occurs. In this case, driving the current error vector to the origin is the priority. Of the states so identified by this requirement (again found by evaluating the dot product), those states are chosen which minimize the deviations. It was observed that the most optimum regulation occurred when the outermost six states (300), (330), (030), (033), (003), or (303) were chosen, since each of these states have the following two properties:

(i) Resulting capacitor charging currents and consequent capacitor voltage deviations produced by the rectifier are the same for each capacitor.

(ii) The magnitude of the voltage developed by the rectifier is the maximum, so these have the

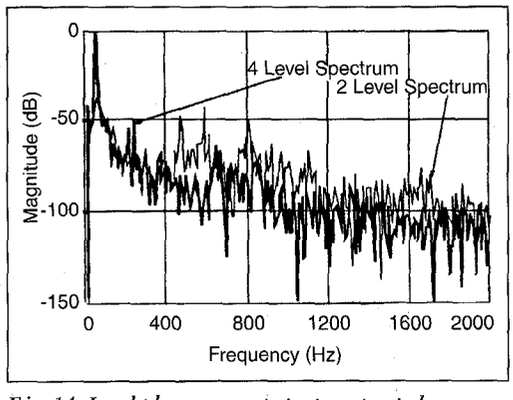

Fig. 14. Load phase current spectra at rated operating point by two- and four-level inverters.

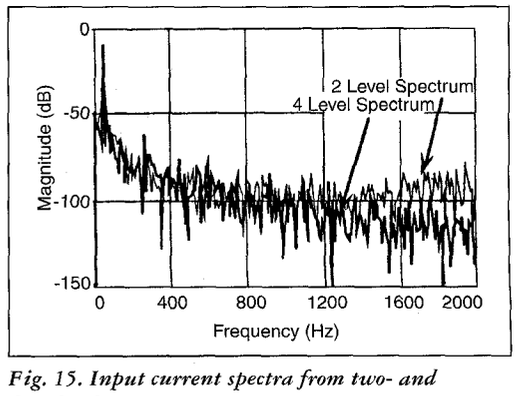

Fig. 15. Input current spectra from two- and four-level converters.

The intersection of the reference with each triangle carrier wave corresponds to modulation across the corresponding capacitor.

maximum effect on driving the current error vector to the origin.

Inverter modulation. Open-loop synchronous sine triangle PWM based on [13], was used on the inverter to drive the induction motor. Fig. 6 shows the carrier waves and the phase voltage reference. All the carrier waves are in phase with each other and phase A reference voltage. The switching functions are determined by the comparators which compare the phase reference with the carrier waves. For example, inverter phase A switching function is determined according to:

$$\begin{aligned} b_a &= 0 \quad if\ v_a^* < v_{rc1} \\ &= 1 \quad if\ v_{rc1} \le v_a^* < v_{rc1} \\ &= 2 \quad if\ v_{rc2} \le v_a^* < v_{rc3} \\ &= 3 \quad otherwise \end{aligned} \tag{15}$$

From Fig. 6, it is evident that the intersection of the reference with each triangle carrier wave corresponds to modulation across the corresponding capacitor. Note that pulse dropping occurs for $m_a > 1.0$. The modulation depth has a significant impact on the dc voltage balancing strategy. For $m_a < 1.0$, the innermost capacitor C_2 tends to discharge rapidly whereas the outer capacitors C_1 and C_3 uniformly charge up when the rectifier is used to regulate the dc bus voltage since $\Delta V_{C1} + \Delta V_{C2} + \Delta V_{C3} \approx 0$. So, $i_{c2,avg} \approx -\left(i_{c1avg} + i_{c3avg}\right)$. By symmetry, the outer capacitors have the same polarity of charging currents and the inner capacitor current has the opposite polarity.

In sine triangle PWM, if the phase reference voltages are shifted relative to the carrier waves by the subtraction or addition of a common mode voltage, the relative polarity of the capacitor currents can be changed since the switching functions are modified (Equation (15)). This is illustrated by the control block shown in Fig. 7. Suppose the load current vector is such that $i_a > 0$, $i_b < 0$, $i_c > 0$; the capacitor voltage deviations are $\Delta V_{C1} > \delta$, $\Delta V_{C2} < \delta$, and $\Delta V_{C3} > \delta$, and the sine triangle comparator yields (211). Then, the output of the common mode voltage modulation block is (100) if $\Delta V_{C1} > \Delta V_{C3}$ and (322) otherwise. This modulation offers a consistent way of selecting the right redundant states which charge the dc link capacitors appropriately.

Simulation Results

A typical induction motor drive was configured as shown in Fig. 8. The rectifier and inverter are fully controllable four-level converters (shown using IGBTs). The load is a three-phase, wye connected 100 hp induction motor with rated parameters given below:

P = 100 hp
N_{pole} = 4
V = 460V (line, rms)
r_1 = 0.01 pu
x_1 = 0.1 pu
x_m = 3.0 pu
x_2 = 0.1 pu
r_2 = 0.015 pu

Utility: 460 V (line, rms), 120 kVA, 6% impedance

Series inductance: 1.5 mH/phase

Inverter carrier frequency f_c = 1620 Hz

At the rated operating point (60Hz, T_{rated}) of the motor, the inverter was operated in its linear PWM region (m_a = 1.24) to produce the rated terminal voltage. For all motoring cases, the dc bus

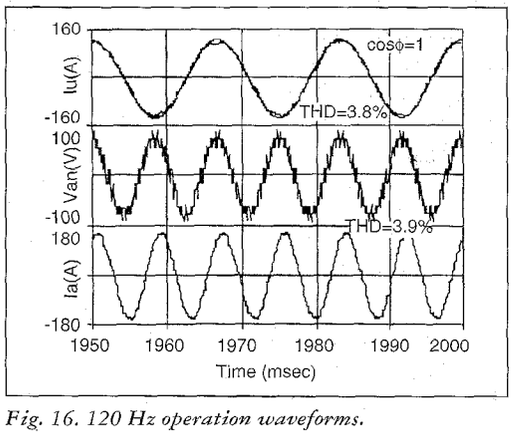

Fig. 16. 120 Hz operation waveforms.

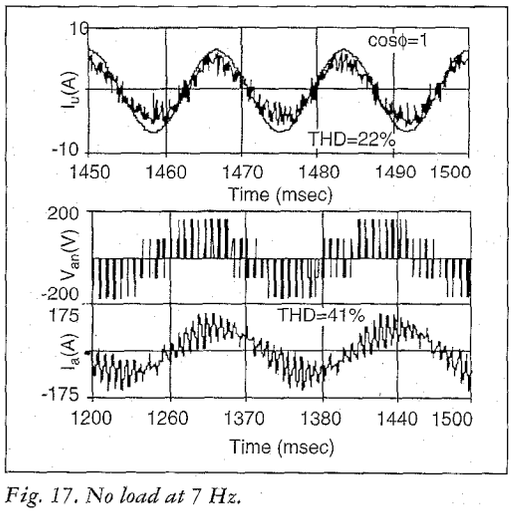

Fig. 17. No load at 7 Hz.

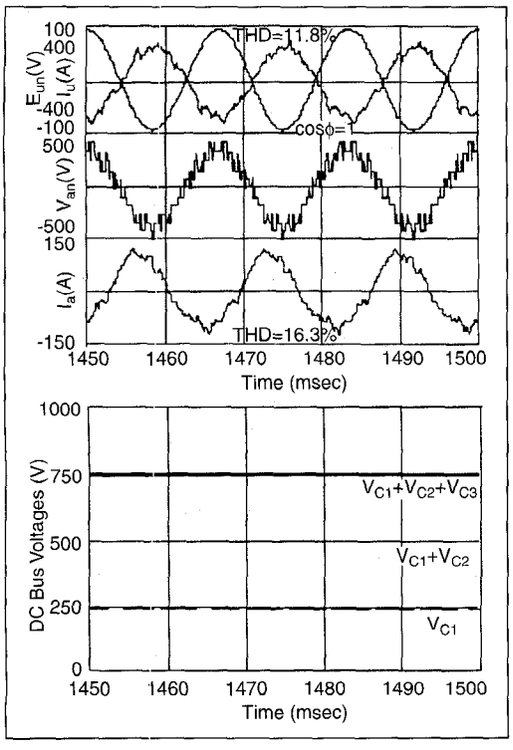

Fig. 18. Generating mode of induction motor. (a) Input and output phase voltage and current. (b) dc bus voltages.

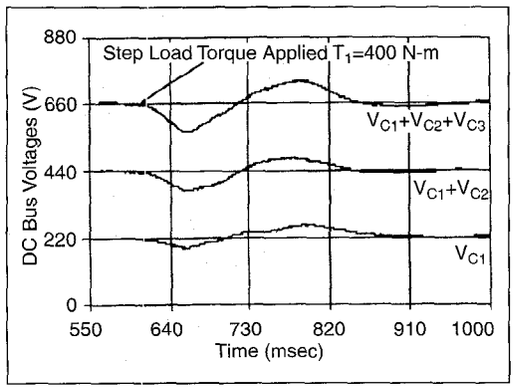

Fig. 19. Transient response of dc bus voltage.

was regulated at 660 V. Fig. 9 shows the motor phase voltage and current under these conditions. The phase voltage THD was found to be 20%, but the phase current THD was only about 8%. Fig. 10 shows the rectifier unity power factor operation (THD = 4%). If filters are used, the voltage THD can be reduced even further—hence, the filter requirements are naturally minimized as a consequence of multilevel PWM.

Fig. 11 shows the dc bus voltages obtained for this operating condition (bus capacitance C_{dc} = 9 *mF*). The dc voltages are regulated efficiently around their nominal values. In the steady state, $V_{c2,avg} < V_{c1,avg}, V_{c3,avg}$. Balancing is generally achieved by regulating $i_{c2,rms}$ to be less than $i_{c1,rms}$ and $i_{c3,rms}$.

The next set of simulation results (Fig. 12) show the motor phase voltage and current as well as the unity power factor input regulated currents when the inverter is saturated at 60 Hz. The input current THD was about 7%. However, the rectifier average switching frequency was higher (2.5 kHz) than the unsaturated inverter case because the rectifier has to balance the dc voltages alone—so the double band hysteresis switching scheme results in more switching events. The motor voltage is about 495V (line,rms) which is close to the limiting value of 515V. Though the current THD is increased to about 19%, the input current are still regulated and the dc voltages stay balanced as shown in Fig. 13.

Fig. 14 shows the spectra of the load phase current when the load is fed by a two-level inverter and by a four-level inverter at its rated point ($V_{ph,rms}$ = 265 V). The two level carrier frequency is 1620Hz whereas the four level carrier frequency is 750 Hz. Clearly, the four-level inverter produces lower distortion especially at lower frequencies. This also brings out a vital feature of multilevel PWM schemes that the switching frequency can be approximately traded off with the number of levels to yield the same distortion.

In Fig. 15, the spectrum of the utility phase current regulated by a four-level rectifier using double hysteresis switching scheme is compared with the current spectrum from an active two level rectifier employing the hysteresis current control scheme. In the former case, the average effective switching frequency (number of pole voltage transitions per second/2) is slightly greater at 1700 Hz as compared to the two-level case, where the rectifier switching frequency was about 1300 Hz. It must be pointed out that the average device switching frequency in the four-level case is less than the average switching frequency—hence the switching losses are not as great as would be expected by the switching frequency number. Also, the four-level rectifier is seen to produce slightly higher harmonics at lower frequency, though at frequencies greater than the average switching frequency the performance of the four-level hysteresis control is clearly demonstrated.

Fig. 16 shows the input and output current waveforms for operation of the motor at 120 Hz, i.e., in the field weakening region of the induction motor. Due to the high operating frequency, the leakage inductance of the motor has a greater effect in filtering the load currents, which explains the low load current THDs. In this case, the carrier frequency was maintained at about 1800 Hz.

Fig. 17 shows the input utility current regulated when the motor runs no load at a low speed (7 Hz). In this case, the rectifier draws only currents to sustain the losses in the system—hence the current references are small in magnitude and the hysteresis switching scheme produces higher

harmonics at the same switching frequencies in the conventional case. Also, the four-level PWM degenerates to two-level PWM due to the low modulation depth. The load phase current THD is high due to the low carrier frequency.

The proposed drive configuration is capable of bidirectional power flow and therefore is fully regenerative. This is a very significant feature of the proposed balancing scheme. Fig. 18(a)-(b) show the regulated input phase current as well as the motor phase voltage and current when the motor is regenerating. The dc bus voltages are still balanced but regulated at a higher voltage. The distortion levels are slightly higher in this operating mode.

The transient response of the rectifier control scheme is best exemplified by Fig. 19, which shows the dc bus voltages following the application of rated load torque on the motor. The total dc bus voltage sags by as much as 15%, though the individual capacitor voltages stay within 5% of their nominal values. The slow response time can be attributed to the strict unity power factor regulation requirement forced upon the rectifier (i.e., $I_{de}^* = 0$ during the transient)—if this condition is relaxed, the transient response is improved significantly.

From the preceding analysis and simulation results, it can be concluded that a four-level rectifier-inverter drive system can be satisfactorily controlled. It has been shown that the control algorithm is capable of simultaneously balancing the capacitor voltages and generating unity power factor currents at the input independently of the inverter operation. Since the inverter may be required only to switch between redundant states of a vector, its operation is unconstrained. The control method can be modified to optimize either the rectifier or inverter switching frequency or the dc capacitance. Though there is no direct coupling between the inverter and the rectifier voltage balancing algorithms, the rectifier control can benefits substantially by introduction of the load feedforward. The voltage balancing strategy works for bidirectional real power flow. There remain several avenues for further optimization of the system.

The dc capacitors used can be made even smaller with the availability of faster IGBTs, which permit higher switching frequencies. The viability of a four-level drive will depend on the tradeoffs between the cost and the performance, which in turn depends on the application. For large motor loads, the multilevel voltage waveforms are an undeniable advantage. The unity power factor operation of the rectifier substantially mitigates the harmonic injection problem. Further, using devices of lower ratings, a four-level inverter can satisfactorily drive loads requiring higher voltages. The strategy outlined adequately addresses the dc voltage balancing problem and serves to make the control of a four-level drive more tractable, thus improving its viability.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral Point Clamped PWM Inverter," *IEEE Trans. Industry Applications,* vol. IA-17, no. 5, September/October 1981, pp. 518-523.

[2] P.M. Bhagwat and V.R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Trans. on Industry Applications,* vol. IA-19, no. 6, November/December 1983, pp. 1057-1069.

[3] C. Hochgraf, R.H. Lasseter, D.M. Divan, and T.A. Lipo, "Comparison of Multilevel Inverters for Static Var Compensation," *Proc. IEEE-IAS '94 Conf.*, pp. 921-928.

[4] F.Z. Peng and J.S. Lai, "A Multilevel Voltage-Source Inverter With Separate dc Sources," *Proc. IEEE-IAS '95 Conf.* pp. 2541-2548.

[5] J.S. Lai and F.Z. Peng, "Multilevel Converters—A New Breed Of Power Converters," *Proc. IEEE-IAS '95 Conf.*, pp. 2348-2356.

[6] M. Klabunde, Y. Zhao, and T.A. Lipo, " Current Control of a 3 Level Rectifier/Inverter Drive System," *Proc. IEEE-IAS '94 Conf.*, pp. 859-865.

[7] J.K. Steinke, "Control Strategy for a Three Phase AC Traction Drive with Three Level GTO PWM Inverter," *Proc. IEEE-PESC '88 Conf.*, pp. 431-438.

[8] J. Zhang, "High Performance Control of a Three Level IGBT Inverter Fed AC Drive," *Proc. IEEE-IAS '95 Conf.,* pp. 22-28.

[9] Y. Zhao, Y. Li, and T. A. Lipo, "Force Commutated Three Level Boost Type Rectifier," *IEEE Trans. on Industry Applications,* vol. 31, no. 1, January/February 1995, pp. 155-161.

[10] J.K. Steinke, "Switching Frequency Optimal PWM Control of a Three Level Inverter," *IEEE Trans. on Power Electronics,* vol. 7, no. 3, July 1992, pp. 487-496.

[11] S. Ogasawara and H. Akagi, "A Vector Control System Using a Neutral-Point-Clamped Voltage Source PWM Inverter," *Proc. IEEE-IAS '91 Conf.*, vol. 1, pp. 422-427.

[12] R.W. Menzies, P. Steimer, and J.K. Steinke, "Five-Level GTO Inverters for Large Induction Motor Drives," *IEEE Trans. Industry Applications,* vol. 30, no. 4, pp. 938-944, July/August 1994.

[13] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis," *Proc. IEEE-PESC '90 Conf.*, pp. 363-371.

[14] M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized Modulation Techniques for the Generalized N-Level Converter," *Proc. IEEE-PESC '90 Conf.*, pp. 1205-1213.