Space-Vector Analysis and Modulation Issues of Passively Clamped Quasi-Resonant Inverters

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***Abstract*— The passively clamped quasi-resonant dc-link (PCQRL) inverter basic topology and other quasi-resonant inverters have been shown to be only partially compatible with pulsewidth modulation (PWM), due to a minimum dwell time created by the clamping mode in the inverter operation. This paper addresses this kind of modulation nonlinearity, employing the space-vector approach as a modeling tool. Closed-form expressions are obtained, defining the inverter linear modulation range in terms of the dwell time and other inverter and load parameters and characteristics. An alternative implementation of the resonant snubber that eliminates the low-order harmonics in the output voltages is presented. Experimental and simulation results are presented to support the theoretical analysis.**

***Index Terms*— Quasi-resonant inverters, soft-switching inverters, space-vector pulsewidth modulation.**

I. Introduction

PULSEWIDTH modulation (PWM) has been widely used in the synthesis of the output voltage of three-phase inverters in ac drive systems, along with many other applications in power electronics. The basic reason is that the PWM techniques lead to negligible energy at frequencies substantially below the inverter switching frequency. However, nonlinearities due to practical constraints on the inverter operation can lead to significant volts-second errors and low-order harmonics in the output voltage [1]–[3].

In recent years, quasi-resonant dc-link inverter topologies have been presented as an alternative to hard-switching inverters. However, these topologies are not fully capable of true PWM operation, due to the existence of a minimum dwell time intrinsic in the operation of the quasi-resonant dc-link circuit [4]–[7]. For instance, if a series inductance is employed to decouple the resonant capacitor from the main dc supply, there will always be a clamping mode to balance the series inductance volts-second with the bus voltage notch interval. During this clamping mode, additional voltage notches cannot be introduced. As a consequence, the inverter switching state cannot be changed (under zero-voltage conditions) during this interval and volts-second errors are introduced in the inverter output voltage with respect to the reference voltage.

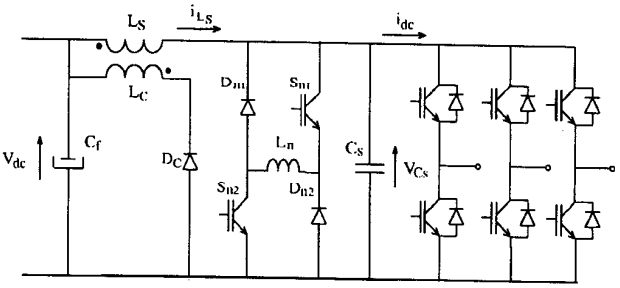

Fig. 1. PCQRL inverter basic topology.

Constant dwell time is obtained if the inverter input dc current is constant. However, the inverter input current changes, due to the modulation of the output voltage. As a consequence, significant changes in the dwell time take place, increasing its detrimental effects on the linearity of the inverter command voltage/output voltage transfer function.

In this paper, the modulation nonlinearity introduced by the minimum dwell time, as described above, is investigated in the passively clamped quasi-resonant dc-link (PCQRL) inverter [8], [9], employing the space-vector approach [10] as a modeling tool. Closed-form expressions are obtained, and the inverter nonlinear modulation range is defined in terms of the dwell time and other inverter parameters. This analysis introduces valuable information on converter design and modulation in applications where PWM compatibility is an issue. Further aspects regarding the compatibility of the basic PCQRL topology with PWM are also pointed out.

A new realization of the PCQRL inverter with distributed snubber capacitor is presented. This realization, along with a proper modulation strategy, is shown to lead to significant improvement in the linearity of the inverter command to output transfer function. Experimental and simulation results are presented to support the analysis presented in this paper.

II. The PCQRL Inverter Topology

A quick review of the PCQRL topology and operating modes is presented in this section. A detailed description, as well as practical design issues, are given in [8] and [9].

The PCQRL inverter topology considered is shown in Fig. 1. This topology is derived from the passively clamped resonant dc-link (PC-RDCL) inverter [11]. Introduction of the

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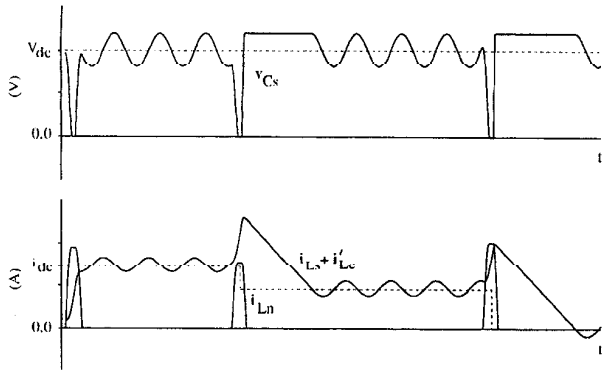


Fig. 2. PCQRL inverter waveforms.

TABLE I
PCQRL INVERTER PARAMETERS

Transformer:	
turns ratio (N1:N2)	1:5
primary inductance L_S	30μH
Notching circuit inductance L_n	14μH
DC Bus snubber capacitor C_S	60nF
Main DC supply	400V
Switching frequency f_S	10kHz

notching circuit (S_{n12}, D_{n12}, L_n) allows operation with dc-bus voltage clamping levels in the range from 1.1 to 1.3 V_{dc}.

In the PCQRL inverter, the function of the dc-link inductance L_S is to decouple the main dc supply from the bus capacitor C_S. The inductance L_C (tightly coupled to L_S) and the diode D_C form the clamping circuit. The extra energy trapped in L_S is pumped through this circuit back to the main dc supply, thus providing a reset mechanism to the quasi-resonant dc-link circuit.

The relevant inverter waveforms are shown in Fig. 2. It is seen that, in this topology, a clamping mode takes place after the dc-bus voltage notch. During this interval, it is not possible to obtain soft-switching conditions for the main inverter. An attempt to activate the notching circuit would lead to abnormally high currents through this circuit.

The PCQRL parameters used in the simulations presented in this paper are listed in Table I. The notching circuit switches are driven by a fixed command pulse (2-μs width). The minimum width of this pulse is given by the dc-bus voltage fall time plus the switching times of the main inverter switches.

The operation of the PCQRL inverter requires only the measurement of the dc-bus voltage amplitude. A bus voltage notch is introduced whenever a mismatch between the modulator output and the present state of the main inverter switches is detected. Further commands to the notching circuit are disabled at this point. When the bus voltage ramps down to zero, the main inverter switches are commanded according to the modulator output. The notching circuit operation is enabled again when the dc-bus voltage crosses the main dc voltage level with a negative derivative. This condition is used to define the point where the clamping mode finishes. This

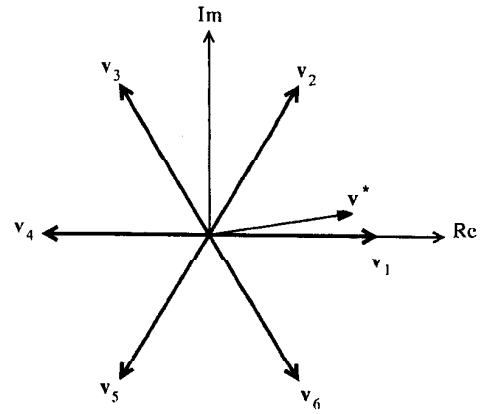


Fig. 3. Space-vector diagram.

operation scheme implies a dwell time given essentially by the bus clamping mode interval. There is also a delay in the switching corresponding to the dc-bus voltage fall time plus the main inverter devices switching time. The dwell time is much larger than the switching delay, and its effects on the inverter operation are significantly more important.

III. QUASI-RESONANT INVERTER MODULATION NONLINEARITIES

A. Characterization of the Minimum Dwell-Time Effects

In order to characterize the PWM capabilities of the inverter, subject to a minimum dwell time, consider the basic situation presented in Fig. 3, where $\mathbf{v}^*$ is the target output voltage vector (reference) assumed located in the sector between vectors $\mathbf{v}_1$ and $\mathbf{v}_2$.

From Fig. 3, the reference vector $\mathbf{v}^*$ can be expressed, in average terms, as

$$\mathbf{v}^* = \frac{t_1^m}{T_S}\mathbf{v}_1 + \frac{t_2^m}{T_S}\mathbf{v}_2 \tag{1}$$

where t_1^m and t_2^m are the calculated intervals for application of the voltage vectors $\mathbf{v}_1$ and $\mathbf{v}_2$ obtained from the space-vector modulation method.

Without loss of generality, assume that the modulator output is such that $0 \leq t_2^m \leq \Delta t_d$, and the inverter operates in the nonlinear modulation range. This situation is depicted in the switching diagram shown in Fig. 4, where Δt_d is the dwell time. The switching commanded at the end of the interval t_2^m only takes place after the dwell time. Hence, the inverter output voltage vector is given by (2):

$$\mathbf{v}_{out} = \frac{t_1}{T_S}\mathbf{v}_1 + \frac{t_2}{T_S}\mathbf{v}_2 \tag{2}$$

where $t_1 = t_1^m$ and $t_2 = \Delta t_d$ are the actual intervals corresponding to the application of voltage vectors $\mathbf{v}_1$ and $\mathbf{v}_2$, respectively. A condition implicit in this switching diagram is that the interval t_0 of application of the null vector is larger than $2\Delta t_d$. Further discussion on this latter condition is presented later in this paper.

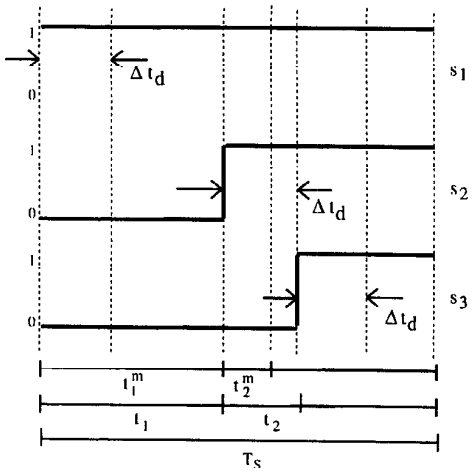


Fig. 4. Basic three-phase switching pattern.

Equation (2) can be rewritten in the form

$$\mathbf{v}_{\text{out}} = \frac{t_1^m}{T_S}\mathbf{v}_1 + \frac{t_2^m}{T_S}\mathbf{v}_2 + \frac{\Delta t_d - t_2^m}{T_S}\mathbf{v}_2. \tag{3}$$

Equation (3) shows the existence of an error voltage vector that models the nonlinear operation of the inverter under the conditions in Fig. 4

$$\mathbf{v}_{\text{error}} = \frac{\Delta t_d - t_2^m}{T_S}\mathbf{v}_2 \quad 0 \le t_2^m \le \Delta t_d. \tag{4}$$

Equations (3) and (4) can be generalized for an arbitrary reference voltage vector $\mathbf{v}^*$. From (4), it is seen that the error voltage vector has variable amplitude and is always aligned with one of the inverter active vectors. The vector $\mathbf{v}_{\text{error}}$ has nonzero amplitude only when the reference voltage vector is close to any of the six active voltage vectors of the three-phase inverter.

Comparing (1) and (3), it is seen that the boundary between the linear and nonlinear modulation regions is reached when $t_2^m = \Delta t_d$, where it can be assumed that $\mathbf{v}_{\text{out}} = \mathbf{v}^*$.

Applying (1) at the boundary between linear and nonlinear modulation leads to

$$T_S|\mathbf{v}^*|\begin{bmatrix}\cos\alpha\\ \sin\alpha\end{bmatrix} = t_1^m\left(\frac{2}{3}\right)V_{\text{dc}}\begin{bmatrix}1\\0\end{bmatrix} + \Delta t_d\left(\frac{2}{3}\right)V_{\text{dc}}\begin{bmatrix}1/2\\ \sqrt{3}/2\end{bmatrix} \tag{5}$$

where vectors $\mathbf{v}^*$, $\mathbf{v}_1$, and $\mathbf{v}_2$ are represented in terms of their components in the complex plane.

Solving (5) for the position of the reference voltage vector corresponding to the boundary between linear and nonlinear modulation ranges

$$\alpha = \sin^{-1}\left(\frac{1}{\sqrt{3}}\frac{V_{\text{dc}}}{|\mathbf{v}^*|}\frac{\Delta t_d}{T_S}\right). \tag{6}$$

A geometrical interpretation of the above results is shown in Fig. 5. It is seen that the angle α in (6) defines a region around the inverter active voltage vectors in the complex plane where a nonlinear relationship between the reference voltage vector and the inverter output voltage vector take place. In other words, the angle α defines the nonlinear modulation range.

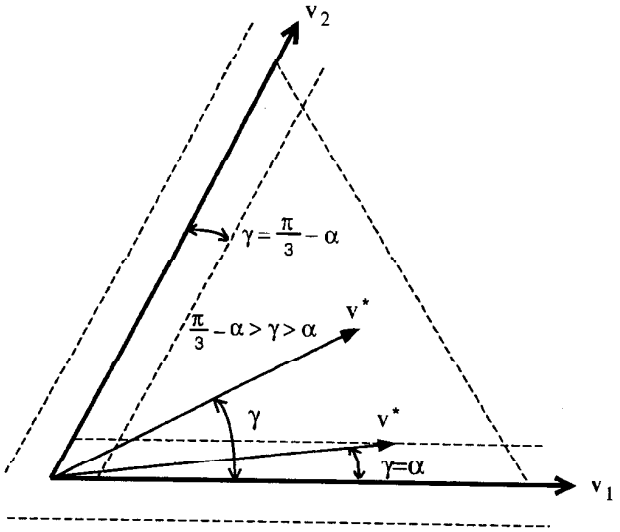


Fig. 5. Vector representation of the linear/nonlinear modulation regions due to the dwell time.

In Fig. 5, it is pointed out that the nonlinear range about the vector $\mathbf{v}_2$ is also given in terms of the angle α defined in (6). In fact, following the procedure described above for all the other active voltage vectors of the inverter, it is seen that the nonlinear modulation range can be described in terms of the angle γ of the reference voltage vector with respect to the real axis as

$$(n-1)\frac{\pi}{3} - \alpha < \gamma < (n-1)\frac{\pi}{3} + \alpha, \qquad n = 1, 2, \cdots, 6. \tag{7}$$

As already pointed out, the nonlinear modulation range leads to volts-second errors in the output voltage with respect to the reference. These errors are modeled in the form of the error voltage vector in (4). Equation (6) shows the effect of relevant parameters of the inverter on the size of the nonlinear modulation range.

The dwell time also affects the dc-bus voltage utilization, limiting the maximum amplitude of the output voltage that can be synthesized. For constant switching frequency operation in the inverter linear modulation range, it is required that $t_0 \ge \Delta t_d$, as the dwell time also imposes a minimum interval for the null vector. In the nonlinear modulation range, a sufficient condition to keep constant switching frequency is $t_0 \ge 2\Delta t_d$. This condition arises from the limit case where the dwell time exceeds the interval of application of one of the active voltage vectors involved in the modulation process by Δt_d. If this "extra" time is taken from the zero-voltage vector interval, volts-second errors are introduced, but the switching frequency remains constant.

The dc-bus voltage utilization of the PCQRL inverter is lower than that observed for a hard-switching inverter with space-vector modulation. However, it can be shown that the dc-bus utilization of a hard-switching inverter with sine-triangle PWM ($m \le 1.0$) is matched under the condition

$$\Delta t_d < 0.13 T_S. \tag{8}$$

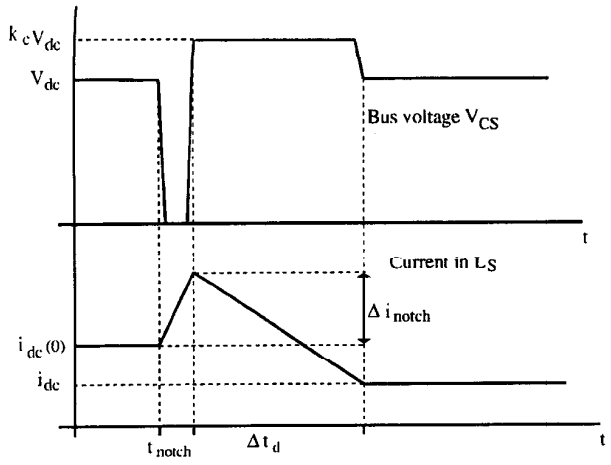


Fig. 6. Simplified PCQRL waveforms.

A last point that can be observed from Fig. 5 is that the output voltage vector amplitude cannot be continuously reduced down to zero. The minimum nonzero output voltage corresponds to the condition where $t_1^m = t_2^m = \Delta t_d$, for the situation in Fig. 3.

B. Load Current Effects on the Dwell Time

In the analysis above, the dwell time was included as an independent parameter. In this section, its dependency on the inverter operating conditions is discussed.

As mentioned earlier in this paper, the dwell time is essentially due to the intervals where the dc-bus voltage is clamped and soft-switching conditions for the main inverter cannot be introduced. This is true for the PCQRL topology and similar ones that employ a series inductor in the dc link. Other quasi-resonant link inverter topologies have similar dwell-time problems due to the time required to build up the necessary energy levels to complete the notching cycle and, also, the relaxation time of the notching circuit [6], [7].

The PCQRL, as well as other quasi-resonant inverter topologies, exhibit a "standard" dwell time under no-load conditions. In this case, the dwell time is constant and it is basically due to the volts-second balance on L_S (notch and clamping intervals) and can be calculated from the inverter parameters. A similar situation is observed if the peak load current is significantly lower than the peak resonant current through L_S, since small changes in the volts-second on L_S are required for i_{Ls} to track i_{dc}. On the other hand, significant changes on the duration of the dwell time will take place as a result of the modulation process if the peak load current is comparable to the peak resonant current through L_S.

Fig. 6 shows simplified waveforms for the dc-link bus voltage v_{Cs} and the current through L_S. From Fig. 6, the dwell time can be calculated in a first-order approximation as (9)

$$\Delta t_d = \frac{L_S}{(k_C - 1)V_{\rm dc}}[i_{\rm dc}(0) - i_{\rm dc}] + \frac{L_S}{(k_C - 1)V_{\rm dc}}\Delta i_{\rm notch} \quad (9)$$

where $\Delta i_{\rm notch}$ (the current increase in L_S during the notch interval) is approximately constant, k_C is the clamping factor, $i_{\rm dc}$ is the inverter dc input current after the switching, and $i_{\rm dc}(0)$ is the previous inverter input current. In (9), $\Delta t_d \geq 0$. The inverter input current $i_{\rm dc}$ can be obtained at any instant from the scalar product

$$i_{\rm dc} = \mathbf{i}_{\rm load} \cdot \frac{\mathbf{v}_n}{|\mathbf{v}_n|} \quad (10)$$

where $\mathbf{i}_{\rm load}$ is the load current space vector and $\mathbf{v}_n$ is the present output voltage vector, with $n = 0, 1, 2, \cdots, 7$. From the assumption that the load current amplitude is constant during any switching interval and from (10), it is seen that the load power factor plays an important role on determining the inverter dwell time. It is also clear that the current $i_{\rm dc}$ changes discontinuously as a result of the output voltage modulation. Notice also that, if $i_{\rm dc}(0) - i_{\rm dc} \ll \Delta i_{\rm notch}$, the dwell time is approximately constant.

From (9), it is seen that maximum dwell time is obtained when $i_{\rm dc}(0) - i_{\rm dc} = i_{\rm load,peak}$, for a certain load. It can be shown that this worst case scenario happens when the position of the load current vector with respect to the real axis in the complex plane is an integer multiple of $\pi/3$ ($\mathbf{i}_{\rm load}$ is aligned with one of the inverter voltage vectors $\mathbf{v}_1, \mathbf{v}_2, \cdots, \mathbf{v}_6$). Its occurrence depends on the load power factor and on the switching pattern adopted in the modulation process. An important observation is that the dwell time increases when the instantaneous power transferred to the load decreases ($i_{\rm dc}(0) - i_{\rm dc} > 0$) as result of the commanded switching pattern. Under this condition, the excess energy trapped in the dc-link transformer is transferred back to the main dc supply and a longer clamping mode takes place.

A reduction in the dwell time (compared to the one associated with the no-load case where $i_{\rm dc}(0) - i_{\rm dc} \ll \Delta i_{\rm notch}$) is observed if the main inverter switching leads to an increase of the instantaneous power transferred to the load. In this case, the energy trapped in the dc-link transformer is transferred to the load, and the duration of the clamping mode (or reset mode) is minimized.

IV. Simulation Results

The analysis developed in the previous section has important implications on both design and control of the PCQRL and other quasi-resonant inverter topologies if compatibility with PWM is an issue. In this section, some of the aspects previously discussed are demonstrated by means of simulation results.

Fig. 7 illustrates the condition where the inverter supplies a load with lagging displacement power factor (DPF). This situation is considered here as the PCQRL topology is most likely to be used in ac drive systems.

For the condition illustrated in Fig. 7, two possible switching patterns are considered here to obtain $\mathbf{v}^*$ in the first sextant.

Sequence 1: $\mathbf{v}_1 \rightarrow \mathbf{v}_2 \rightarrow \mathbf{v}_7$.

Sequence 2: $\mathbf{v}_2 \rightarrow \mathbf{v}_1 \rightarrow \mathbf{v}_0$.

Although these two patterns are the inverse of each other, they essentially differ in the placement of the null vector in the switching sequence.

Consider operation with a high load power factor, such that $\cos\phi > 0.87$. A careful analysis of the switching sequences 1

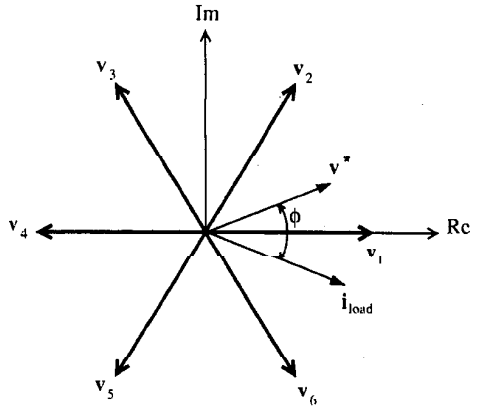


Fig. 7. Space-vector diagram with lagging power factor load.

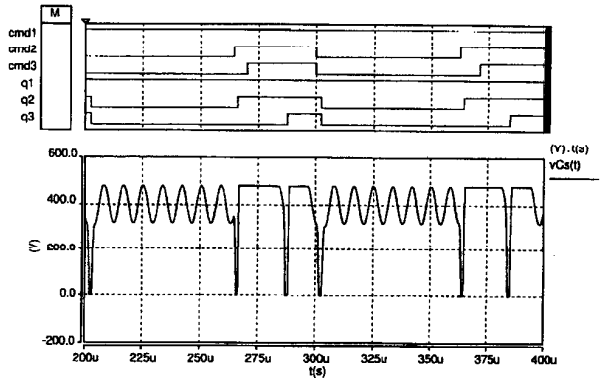


Fig. 8. Switching states and dc-bus voltage for switching sequence 1.

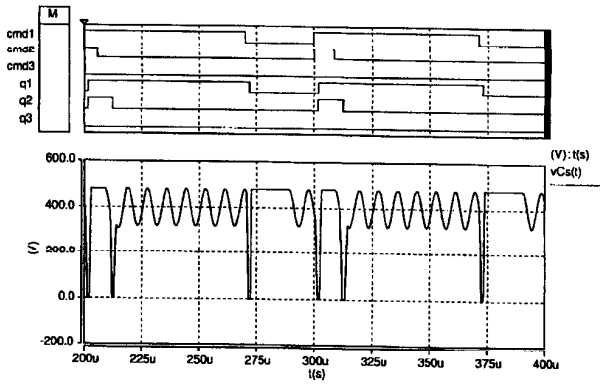
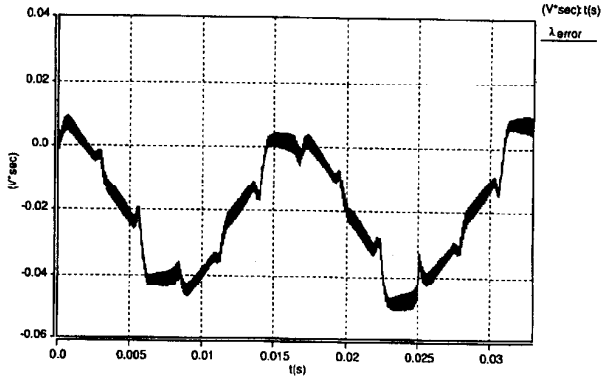
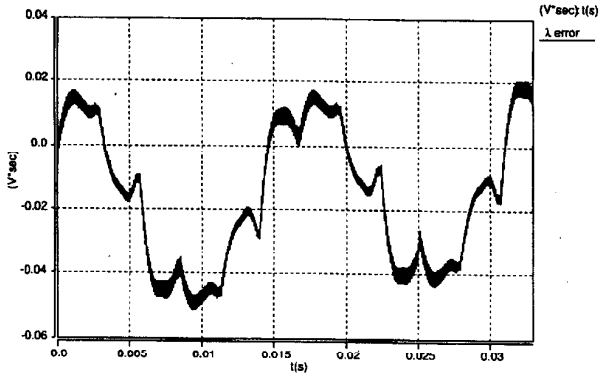


Fig. 9. Switching states and dc-bus voltage for switching sequence 2.



(a)



(b)

Fig. 10. Volts-second error plots with switching pattern 1. (a) Modulation index = 0.90. (b) Modulation index = 0.45.

and 2 under this condition shows that the inverter input current i_{dc}decreases from one inverter state to the next with switching sequence 1. The opposite behavior is obtained with switching sequence 2, where i_{dc} increases from one state to the other within one switching period.

Figs. 8–11 illustrate the issues pointed out in the analysis developed in this paper. The results were obtained for a load current $I_{LOAD} = 30$ A (peak), $\cos\phi = 0.87$, and $f = 60$ Hz.

Figs. 8 and 9 show switching states and dc-bus voltage (v_{Cs}) waveforms for the vector sequences 1 and 2, respectively. In these figures, cmd_{123} are the space vector modulator output and q_{123} are the actual states of the main inverter switches. These plots correspond to $\gamma \approx 0$ and the reference voltage vector $\mathbf{v}^*$ is as indicated in Fig. 7, but very close to $\mathbf{v}_1$. Notice that, with switching pattern 1, the dwell-time effects are much more pronounced than with switching sequence 2, as expected. The significant reduction of the dwell time observed on switching pattern 2 indicates a corresponding reduction of the size of the nonlinear modulation range.

The effect of the modulation index on the volts-second error between the PCQRL inverter output voltage and reference is illustrated by means of Figs. 10 and 11 for switching patterns 1 and 2, respectively. These plots correspond to the phase-a component of the volts-second error vector λ_{error}, defined as

$$\lambda_{error} = \int (\mathbf{v}_{out} - \mathbf{v}^*)\, dt. \tag{11}$$

It can be observed that the vector λ_{error} differs from the ripple current vector introduced in [11] by a constant factor that models the inverse of the load inductance.

The volts-second error plots in Figs. 10 and 11 show spikes at regular intervals of $\pi/3$ rad, corresponding to the nonlinear modulation regions around the voltage vectors $\mathbf{v}_1, \mathbf{v}_2, \cdots, \mathbf{v}_6$,

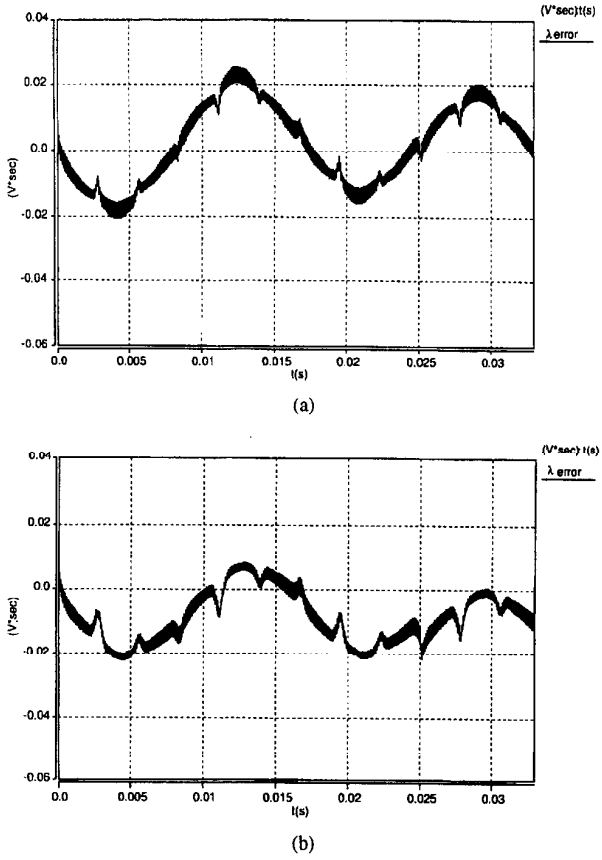


Fig. 11. Volts-second error plots with switching pattern 2. (a) Modulation index = 0.90. (b) Modulation index = 0.45.

as discussed in the analysis of the effects of dwell time. These plots also illustrate the fact that a reduction in m leads to a reduction of the linear modulation region, as shown by (6). A comparison between Figs. 9 and 10 shows that the detrimental effects of the dwell time are significantly reduced with switching pattern 2. It is important to mention the similarity between the results in Figs. 9 and 10 and the current spikes present in the results shown in [4], for a classical space-vector modulator.

The volts-second error plots in Figs. 10 and 11 reveal other important facts about the PCQRL modulation characteristics, besides the influence of the dwell time. Shown, for instance, is the presence of a fundamental frequency component on the volts-second error, indicating the existence of a nonzero error between the reference voltage and the fundamental component of the output voltage. One source of error is the oscillatory characteristic of the dc-bus voltage, due to the resonance between L_S and C_S. Since these oscillations and the main inverter switching commands are not synchronized, volts-second errors might take place during the interval of application of any active voltage vector $\mathbf{v}_n$ $(n = 1, 2, \ldots, 6)$. Another source of error is the mismatch between the volts-second accumulated during the dc-bus voltage notch and during the clamping interval. This mismatch happens because the current i_{dc} is not constant, but changes according to the switching pattern of the inverter. These errors are difficult to anticipate and compensate for in a feedforward manner. This characteristic suggests that superior performance is obtained in applications involving closed-loop operation.

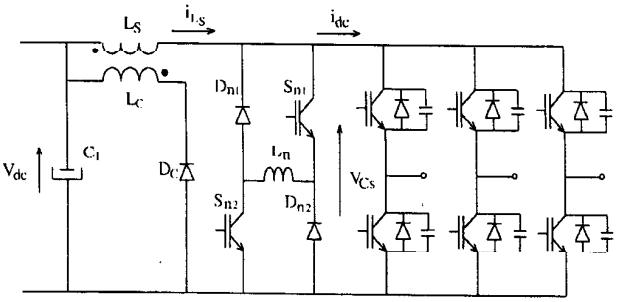


Fig. 12. PCQRL topology with distributed snubber capacitor.

V. The Distributed Snubber Capacitor Topology

Fig. 12 shows a variation of the PCQRL topology, where the resonant capacitor is distributed across the main inverter switches. This arrangement allows zero-voltage turnoff of the inverter switches, without the introduction of a dc-bus voltage notch. This topology features improvement in the PWM linearity and reduction of the notching circuit switching frequency (f_S in contrast with $3f_S$ or higher in the basic PCQRL topology). The distributed snubber capacitor structure has been proposed for resonant and quasi-resonant dc-link inverter topologies in previous papers [12], [13].

The control of the distributed snubber topology implies a switching pattern that is uniquely defined by the reference voltage vector and load current vector. In order to take maximum advantage of the zero-voltage turnoff without dc-bus voltage notching, three of the inverter switches are always conducting at the beginning of the switching interval. The desired switching pattern is obtained by turning off these switches under zero-voltage conditions, without notching the dc-bus voltage. For the situation illustrated in Fig. 7, a suitable switching pattern for the distributed snubber capacitor topology is given by the vector sequence (switching pattern 1) $\mathbf{v}_1 \rightarrow \mathbf{v}_2 \rightarrow \mathbf{v}_7$. A dc-bus voltage notch is introduced to reach the required inverter state at the beginning of each switching period.

Proper operation of the PCQRL topology with distributed snubber capacitor leads to a minimization of the effects of the clamping mode on the commanded switching pattern when compared to the basic topology. The distributed snubber capacitor guarantees ZVS conditions for switch $\rightarrow$ diode commutations, without the need to introduce a dc-bus voltage notch. Introduction of a bus voltage notch is required only to perform the transition from $\mathbf{v}_7 \rightarrow \mathbf{v}_1$, where all the diode $\rightarrow$ switch commutations take place. As a result, the switching commands are not blocked during the clamping interval, since the output voltage vector can be switched, even during a dc-bus clamping interval. Another consequence of this switching strategy is the reduction of the notching circuit switching frequency to that of the main inverter (one dc-bus notch per switching period).

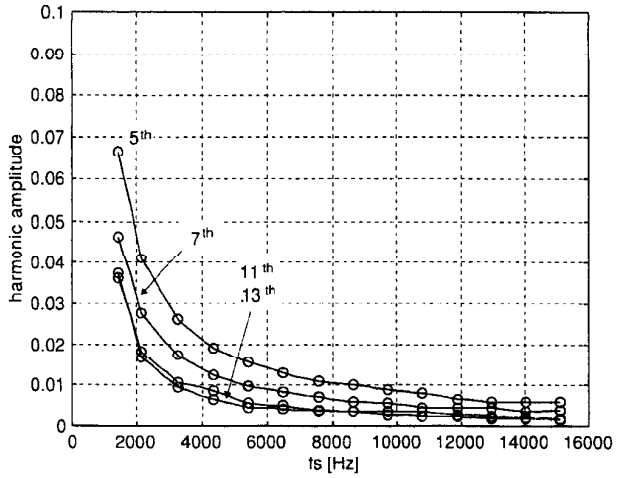


Fig. 13. Low-frequency harmonics amplitudes associated with the proposed switching pattern (DPF = 0.9 lagging).

TABLE II
PCQRL INVERTER PARAMETERS.

Transformer:	
turns ratio (N1:N2)	1:5
primary inductance L_s	30μH
Notching circuit inductance L_n	14μH
DC Bus snubber capacitor C_S	22nF (x6)
Switching frequency f_S	10kHz

Although the volts-second errors due to the dc-bus voltage clamping are minimized in this case, the introduction of low-frequency distortion associated with the switching function described above still has to be investigated. Notice that the proposed switching pattern implies single-edge PWM, as well as changes in pulse position within the switching period at $\pi/3$ intervals, potentially originating low-frequency harmonic distortion of the output voltages.

Fig. 13 shows the variation in the amplitude of characteristic low-frequency harmonics present in the inverter switching function as a function of the inverter switching frequency. These plots were obtained from numerical simulation results for a 60-Hz command voltage and DPF equal to 0.9 lagging. Notice the fast decay of the harmonics amplitudes as the switching frequency increases. Negligible harmonics amplitudes are anticipated for switching frequencies above 10 kHz. This high switching frequency requirement does not constitutes a limitation, considering that quasi-resonant dc-link inverters are intended for operation at high switching frequencies (reduced switching losses from ZVS operation).

A prototype of the PCQRL inverter with distributed snubber capacitor was implemented for the experimental evaluation of the performance of this new PCQRL topology and proposed switching strategy from the perspective of modulation linearity. The inverter parameters are given in Table II. Modulation and control functions were implemented on a Motorola 56 000 fixed-point digital signal processor (DSP) system.

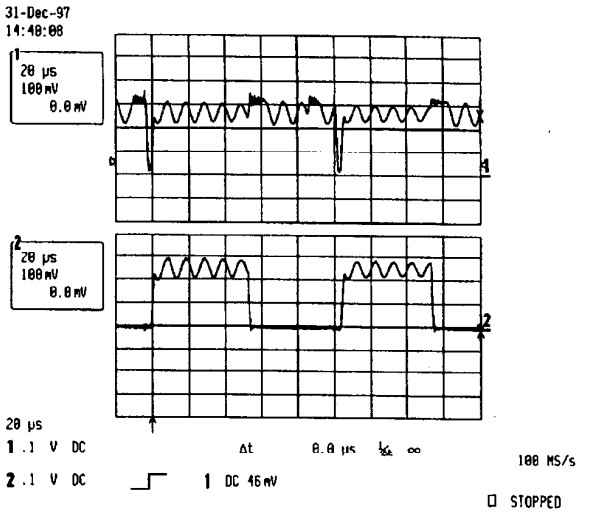


Fig. 14. PCQRL with distributed snubber capacitor. Upper trace: inverter input voltage (50 V/div). Lower trace: output line voltage (50 V/div).

Figs. 14–16 show plots of the relevant variables associated with the inverter operation. These plots were obtained for open-loop operation with a passive load set at approximately 10 A_{rms} with a displacement power factor equal to 0.88 lagging ($r = 3.9\ \Omega$, $L = 5.6$ mH). The inverter was operated at reduced dc bus voltage (130 V). The modulation index was set at 0.9. The fundamental output voltage frequency was fixed at 60 Hz.

Fig. 14 shows the inverter input voltage v_{Cs} and the inverter output line voltage v_{ab}. Notice the absence of a clamping interval following the dc-bus voltage notch, since the dc-link current is stepped up at this point. The following switching events cause the dc-link current to reduce and clamping modes result, so that i_{Ls} tracks i_{dc}, as explained in the previous sections.

Fig. 15 shows a detail of the voltages across the switches in the inverter leg associated with phase a. The two commutation conditions present in this topology are shown in this figure. The commutation from the upper switch to the lower one is performed during a dc-bus notch (notice the delay between the voltage waveforms). The second commutation is performed using only the snubber capacitors.

Fig. 16 shows plots of the output current on phase a and line voltage v_{ab} for operation under the conditions specified above. Results from the spectral analysis of the output line voltage are summarized in Table III, measured using an HP3561A spectrum analyzer. The total harmonic distortion (THD) of the output line voltage shown in this figure is THD= 1.19% (measurements include up to the 20th harmonic of the fundamental).

The line voltage harmonic components are the same seen on the line current [10], but with amplitudes scaled down by the filtering effect of the inductive load. The measurements in Table III confirm the expectations in terms of a significant reduction of the effects of the clamping mode on the linearity of the inverter transfer function. Hence, volts-second errors on the output voltages and the associated low-frequency harmonics are minimized.

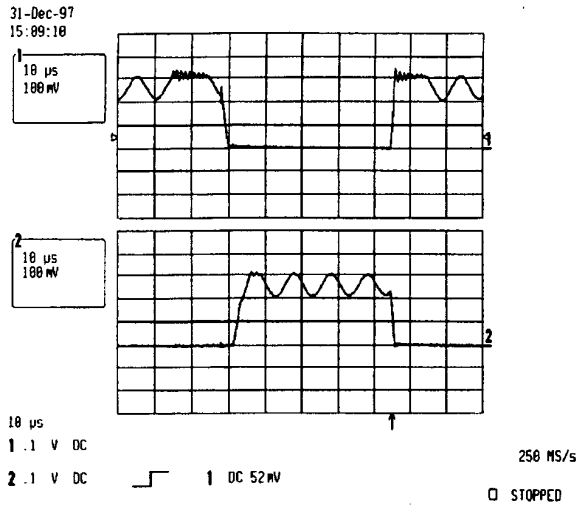


Fig. 15. PCQRL with distributed snubber capacitor. Upper trace: voltage across S_{a+} (50 V/div). Lower trace: voltage across S_{a-} (50 V/div).

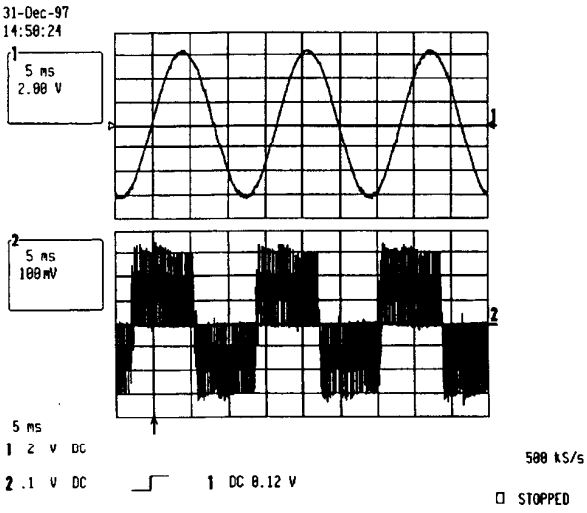


Fig. 16. PCQRL with distributed snubber capacitor. Upper trace: inverter line current (5 A/div). Lower trace: output line voltage (50 V/div).

TABLE III
OUTPUT LINE VOLTAGE HARMONICS

Order	fund	5th	7th	11th	13th
Amplitude [V]	78.4	0.38	0.32	0.26	0.05
Amplitude [%]	100	0.48	0.40	0.33	0.06

THD = 1.19% (including up to 20th harmonic).

VI. CONCLUSION

In this paper, a detailed analysis of the modulation nonlinearity introduced by the dwell time in the PCQRL inverter topology was presented. A relationship between inverter parameters and the size of the nonlinear modulation range of the inverter voltage space vectors was derived. Although the modeling in this paper was developed for the PCQRL topology, the methodology employed is general and can be applied to other quasi-resonant inverter topologies.

The equations defining the nonlinear modulation range can be used in the characterization and comparison of quasi-resonant converter topologies. Alternatively, they can be used along with circuit dynamics and losses considerations in the design of quasi-resonant inverters in applications where PWM compatibility is an issue.

The analysis presented on the basic PCQRL inverter topology indicates a decrease in performance as the switching frequency is increased. The distortions in the inverter switching function as a result of the dc-bus voltage clamping mode were shown to be reduced by proper switching schemes leading to the reduction of the total clamping time within a switching period. This latter statement also implies that the clamping mode effects are naturally minimized if the switching frequency is made sufficiently low ($T_S \gg \Delta t_d$).

A variation of the PCQRL inverter with distributed snubber capacitor was introduced in this paper, along with suitable modulation and control techniques. This new realization of the PCQRL inverter is aimed at applications involving high switching frequency operation. Simulation and experimental results presented in the paper have shown that modulation linearity problems are essentially eliminated in this case, provided that sufficiently high switching frequencies are employed (10 kHz and higher). Another advantage over the basic PCQRL inverter topology is the operation of the notching circuit at the main inverter switching frequency.

REFERENCES

[1] P. D. Evans and P. R. Close, "Harmonic distortion in pwm inverter output waveforms," *Proc. Inst. Elect. Eng.*, vol. 134, pt. B, no. 4, pp. 224–232. July 1987.
[2] R. B. Sepe and J. H. Lang, "Inverter nonlinearities and discrete time vector current control," *IEEE Trans. Ind. Applicat.*, vol. 30, pp. 62–70, Jan./Feb. 1994.
[3] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for pwm inverters with switching lag-times," *IEEE Trans. Ind. Applicat.*, vol. 23, pp. 881–886, Sept./Oct. 1987.
[4] S. Salama and Y. Tadros, "Quasi resonant 3-phase IGBT inverter," in *Conf. Rec. IEEE PESC'95*, 1995, pp. 28–33.
[5] D. M. Divan, L. Malesani, P. Tenti, and V. Toigo, "A synchronized resonant dc link converter for soft-switched PWM," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 940–947, Sept./Oct. 1993.
[6] J. G. Cho, H. S. Kim, and G. H. Cho, "Novel soft switching converter using a new parallel resonant dc link," in *Conf. Rec. IEEE PESC'91*, 1991, pp. 241–247.
[7] L. Malesani, P. Tenti, P. Tamasin, and V. Toigo, "High efficiency quasi resonant dc link converter for full-range PWM," in *Conf. Rec. IEEE APEC'92*, 1992, pp. 472–478.
[8] S. Chen and T. A. Lipo, "A passively clamped quasiresonant dc link inverter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1994, pp. 841 848.
[9] S. Chen, B. J. C. Filho, and T. A. Lipo, "Design and implementation of a passively clamped quasi resonant dc link inverter," in *Conf, Rec. IEEE-IAS Annu. Meeting*, 1995, pp. 2387–2392.
[10] H. W. Van der Broeck, H. C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," *IEEE Trans. Ind. Applicat.*, vol. 24, pp. 142–150, Jan./Feb. 1988.
[11] D. M. Divan and G. Skibinski, "Zero switching loss inverters for high power applications," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1987, pp. 627–634.
[12] L. Malesani, P. Tomasin, and V. Toigo, "Space vector control and current harmonics in quasi-resonant soft-switching pwm conversion," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 269–277, Mar./Apr. 1996.
[13] G. Venkataramanan and D. M. Divan, "Control of pulse width modulated resonant dc link inverter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1992, pp. 737–743.

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