CURRENT PEAK LIMITING FOR A SERIES RESONANT DC LINK POWER CONVERTER USING A SATURABLE CORE

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ABSTRACT **High frequency resonant dc link power conversion circuits often experience irregular high peak current pulses during three phase operation and the pulses rise to over twice the regular pulse amplitude giving rise to current or voltage fluctuations at the output side. This high peak current/voltage problem appears to be common to both series/parallel resonant types respectively because of duality of the systems. In this paper current peak limiting has been performed by means of a saturable core inserted in the DC link as the resonant inductance. A simplified circuit limiting peak current is proposed and the resulting performance of the system is investigated by means of digital simulation.**

1. INTRODUCTION

Interest in power conversion schemes with an ac or dc resonant link, featuring zero voltage or zero current switching has expanded enormously recently. This method of power conversion concerns the possibility of having not only very low switching losses but also a higher power density converter arrangement. The method of pulse modulation using a DC-AC series resonant converter was originally introduced by [1], which confers almost all the inherent features of the high frequency link that is being described in this paper. Unfortunately, the major draw back of this system was that it required bi-directional current carrying switches, giving rise to a high device cost. Moreover, the current peaks of the resonant link could not be controlled, which consequently further increased the device cost. The series resonant DC link type AC to AC power conversion scheme was proposed later [2]. This converter is the dual of the parallel resonant DC link type and the switching occurs at zero current instants [3]. In addition, the system utilizes only twelve thyristors for full double bridges at the input and at the output. Thus, this configuration features a minimum number of devices as well as high current and high voltage withstand margins because of the use of thyristors. However, this system experiences high peak currents depending upon the voltage difference impressed on the link when the conducting switches change. This current pulse amplitude occasionally becomes two or three times larger than that of the normal pulse height and disturbs the output current as well as the voltage regulation. In the case of the parallel resonant dc link converter, the problem encountered is not the occurrence of high current peaks but high voltage peaks that arise when the switching of conducting transistors occurs between phases. This situation is expected since the two schemes are duals of each other. A method of voltage clipping for the parallel resonant system was presented by utilizing an extra transistor, diode and a capacitor [3]. It is shown in this paper, that to realize current clipping, a simple saturable ferrite core can be employed in place of the resonant inductance. The principles of the pulse limiting and the simplification of the circuit are explained in detail and the control strategies adopted are discussed. A new method for establishing the switching function and a feedback method for selecting the optimum biasing current, are also presented. Since the trimming or circulating current mode is not used, this

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system allows a simple control method for operation while still maintaining stability accompanied by good motor torque characteristics.

2. PRINCIPLE OF OPERATION

2.1 Prototype System

Figure 1 shows a prototype of the series resonant dc link converter. The inductance L_0 and the capacitance C_0 form a high frequency series resonant circuit and the capacitor banks at the output and input are simple low-pass filters needed to maintain the resonant frequency and to obtain better output and input current waveforms. The resonating current i_s is shown in the Fig. 1. The dc current I_d is superimposed on the resonant current by the inductance L_d which is very large and is considered as a constant current source.

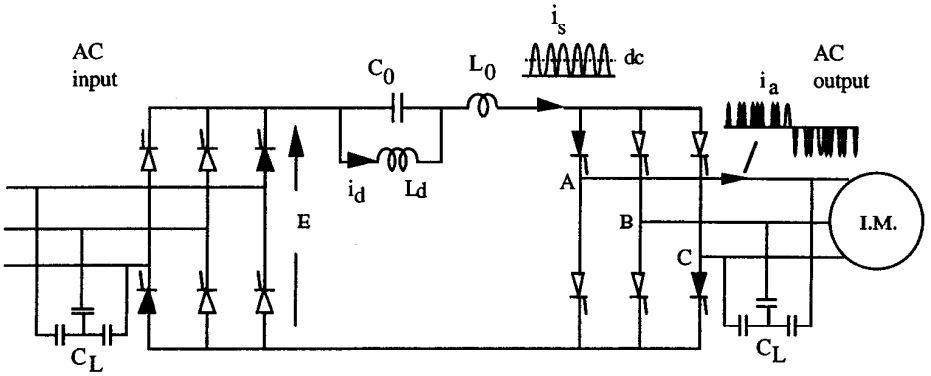


Fig.1 Conventional High Frequency Series Resonant DC Link AC/AC Converter

The resonant current i_s begins by triggering the four thyristors shown in black. After the occurrence of each current pulse, all the thyristors are subsequently extinguished and the bias current I_d begins charging the resonant capacitor C_0 linearly so that a forward bias is reached for the next pair of thyristors to be triggered. When the forward bias has reached a specified threshold voltage, the next set of four thyristors are triggered to obtain a new current pulse. The switching of main thyristors is done only at zero current instants of i_s resulting in very low switching losses. The current pulses are distributed to each phase by the method of Pulse Density Modulation (PDM) [2].

2.2 Resonant Pulses

A mono-phase equivalent circuit of the three phase converter topology is shown in Fig. 2 (a). The voltage E is the output voltage of the input converter and V_{CL} is the line-line voltage of the output capacitor bank. The capacitor C_L represents the effective lumped capacitance of the filter capacitors at the input and output bridges. Thyristor T_h represents the effect of the conducting four thyristors in series and the selector switch shows the possibility of selecting different output phases. Due to the fact that the inductance L_d is sufficiently large, the DC off-set given by the current I_d is almost constant. Since the output frequency is low compared with the resonant frequency and the capacitor C_L is also relatively large, the voltage V_{CL} across the capacitor C_L can be assumed as constant over the period of each current pulse. Under these assumptions, the circuit equation is simplified as,

$$E - v_{CL} = L_0 \frac{di_s}{dt} + \frac{1}{C_0}\int (i_s - I_d)\, dt \qquad (1)$$

and the resulting current i_s becomes

$$i_s = I_d (1 - \cos \omega_0 t) + \sqrt{\frac{C_0}{L_0}} V_{th} \sin \omega_0 t \qquad (2)$$

where,

$$\omega_0 = \sqrt{\frac{1}{L_0 C_0}}$$

$$V_{th} = E - V_0 - V_{CL} \; ; \; V_0 : \text{initial voltage across } C_0 \qquad (2')$$

Therefore, the peak value of i_s is dominated by the DC off set I_d and the threshold voltage V_{th}. From equation (2), the maximum current I_{smax} can be expressed as

$$I_{smax} = I_d + \sqrt{I_d^2 + \frac{C_0}{L_0} V_{th}^2} \qquad (3)$$

Therefore I_{smax} becomes constant provided that V_{th} and I_d are kept constant as shown in Fig. 2 (b).

2.3 Irregular Current Peaks

When the output thyristors are switched between different output phases, triggering at V_{th} is not always available. As a result, irregular current peaks appear as shown in Fig. 2 (c). In Fig. 2 (a), if the thyristor T_h stops conducting at time t_1, the following equations are possible with reference to the circuit in Fig. 2 (a).

$$E - \left(V_{C0} + L_0 \frac{d\{i_s(t)\}}{dt} \right)_{t = t_1^-} - V_{01} = 0 \qquad (4)$$

where the phase selected has an output voltage of V_{01}. As the capacitor voltage V_{C0} does not change instantaneously, the voltage of inductance L_0 just before t_1 moves to the voltage V_{swt} across thyristor T_h at the moment just after t_1; that is,

$$(V_{swt})_{t = t_1^+} = \left(L_0 \frac{d[i_s(t)]}{dt} \right)_{t = t_1^-}$$

$$= E - (V_{C0})_{t = t_1^-} - V_{01}. \qquad (5)$$

When thyristors stop conducting at time t_1, the calculation for selecting the next mode is accomplished during the interval given by δt and the capacitor charges linearly by the constant biasing current I_d. The voltage V_{swt} increases to V_{th} at which point the next triggering is scheduled as shown in Fig. 2 (d).

$$(V_{swt})_{t = t_1 + \delta t} = V_{th}$$

$$(V_{swt})_{t = t_1 + \delta t} = V_{th}$$

$$= (V_{swt})_{t = t_1^+} + I_d \frac{\delta t}{C_0}$$

$$= E - (V_{C0})_{t = t_1} - V_{01} \; . \qquad (6)$$

However, when V_{02} is selected for the next current pulse, V_{swt} changes to

$$(V_{swt})_{t = t + \delta t} = E - (V_{C0})_{t = t_1^-} - V_{02} \qquad (7)$$

This case is equivalent to the case where the selector switches move from V_{01} to V_{02} in Fig. 2 (a) during the period $t_1 < t < t_1 + \delta t$.

If the voltage V_{02} is much larger than V_{01}, V_{swt} at $t = t + \delta t$ rises far beyond V_{th} and a high peak current pulse possibly occurs as shown in dotted line in Fig. 2 (d). As a result the system becomes disturbed. Since the biasing current I_d varies because of finite inductance L_d, I_d control, carried out by switching the input thyristors to other input phase voltages

according to the error in I_d (= I_{dref} - I_d), is difficult. Since the voltage E also changes, this also exaggerates the above phenomena.

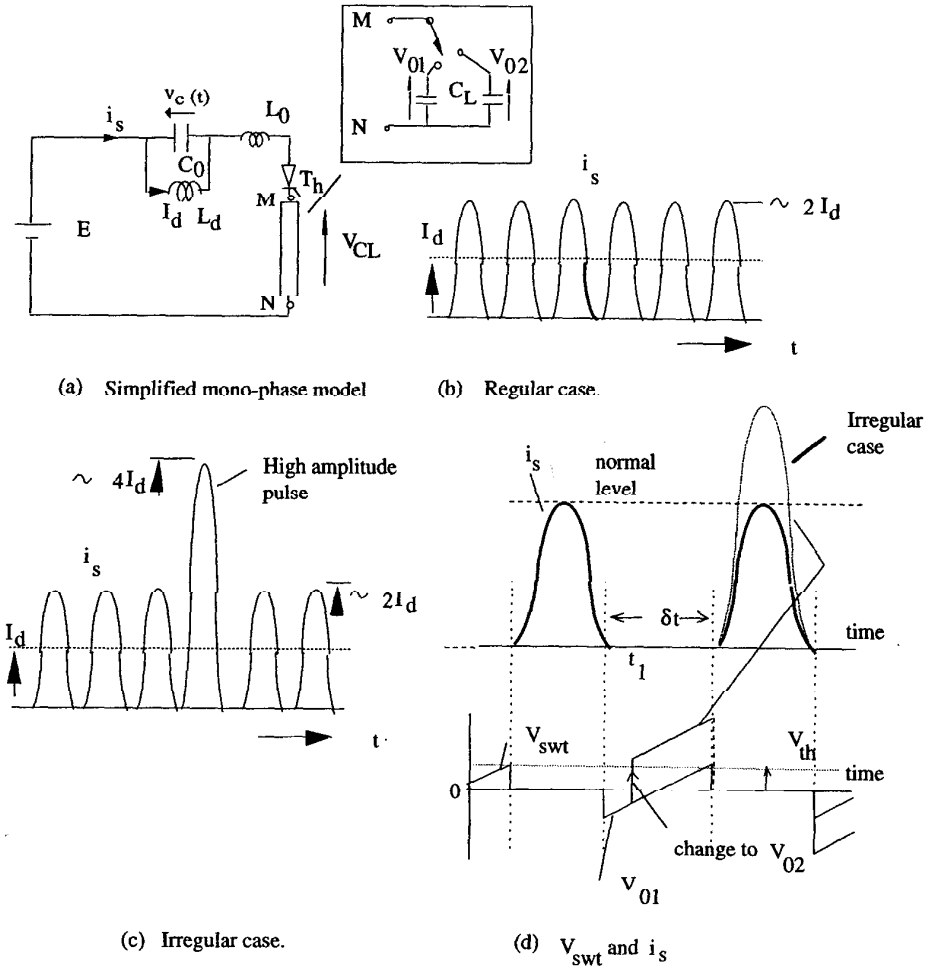


Fig. 2. Current pulse peak for conventional system.

3. CURRENT PEAK LIMITING

A current peak limiting strategy is proposed in this paper to eliminate undesirable high pulses from occurring and to assure uniform pulse height. Figure 3 illustrates the basic idea of current peak limiting. The system, shown in Fig. 3(a), illustrates a simplified mono-phase equivalent circuit for current peak limiting. In this circuit, the resonant inductance L_0 is replaced by a saturable inductance with a bias current I_m and the dc inductance L_d is expressed by a constant current source I_d. The principle of the current pulse limiting is illustrated in Fig. 3(b). In the characteristic of the saturable reactor, i.e., exciting current i_s+i_m vs. magnetic flux linkage λ, the current i_m biases the core in the negative direction. The gradient of the slope of the saturated region is equal to the resonant inductance L_0 and the non-saturated region offers a very high inductance. In the circuit in Figure 3(a), when

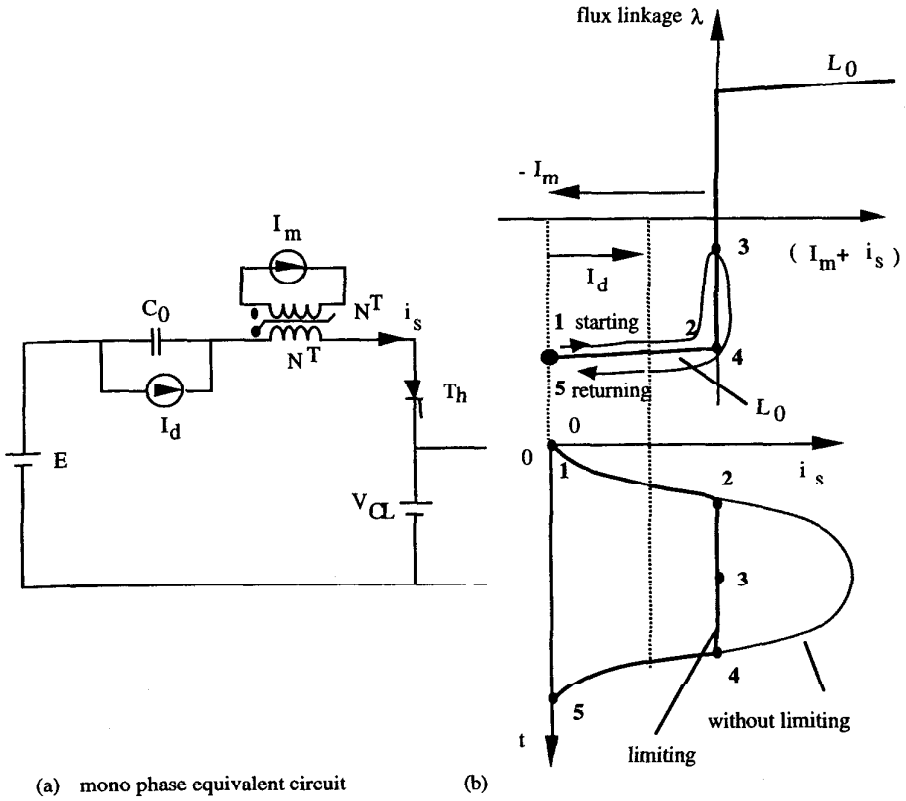


Fig. 3. Illustration for the principle of current pulse limiting.

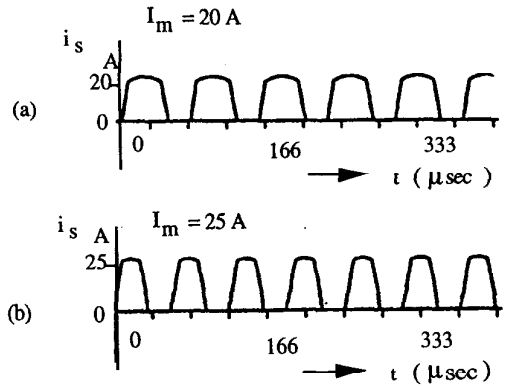


Fig. 4. Examples of current pulses
for the circuit with saturable core.

the thyristor Th is triggered the current pulse starts flowing and the flux λ begins to increase toward point 2 and then to 3 so that the current nearly reaches a plateau, suppressed by the high inductance and returns to zero passing through points 3, 4 and 5 in that order. The corresponding current wave becomes as shown in Figs. 4(a) and (b). Figure 5 shows the actual three phase configuration with current peak limiting. In this system the bias current is

simply fed from the inductor L_d and the biasing current automatically changes according to the load current.

4. CONTROL SCHEME

4.1 Output Converter Control

The control method adopted for the output converter control compares the output voltage of the converter has been defined and the actual output voltage is compared with the reference voltage to generate a switching function. In the implementation of the scheme, the output reference voltages are modified from pulse to pulse by which means the voltage feedback is indirectly achieved. The output voltage feedback criterion is illustrated in Fig. 6. For example, let v_{ab}^* and v_{ab}^{**} represent the defined reference and the modified reference, respectively. When the deviation $e_0 = v_{ab}^* - v_{ab}$ exists at $t = t_0^-$, the modified reference during $t_0 < t < t_1$ is set as $v_{ab}^{**} = v_{ab}^* + e_0$, The required charge to boost the average of the next voltage pulse voltage v_{ab} to the reference v_{ab}^{**} is performed. After this procedure if the deviation $e_1 = v_{ab}^{**} - v_{ab}$ results at $t = t_1^-$ the deviation e_1 will be used for the next modified reference as $v_{ab}^{**} = v_{ab}^* + e_1$ as illustrated in the figure. This method is also particularly effective in reducing the torque ripple which occurs in converter fed induction motor drives.

The overall system diagram is given in Fig. 7. Thyristor selection for triggering is performed based on the sign of the charge demand by each phase and the estimation of charges required is done in such a manner that the errors sustained in the output three phases

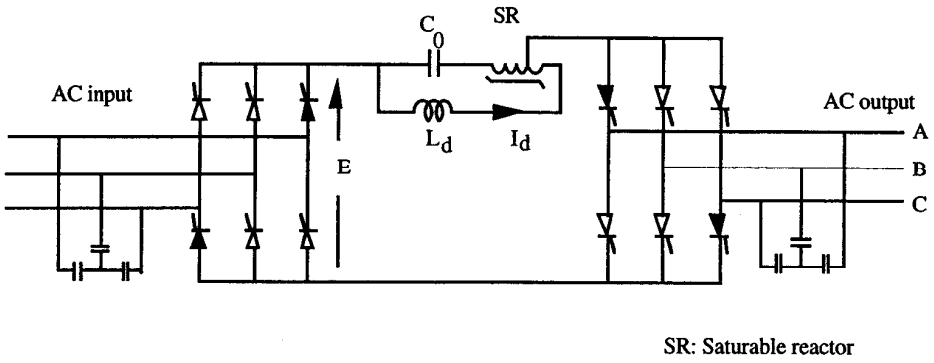
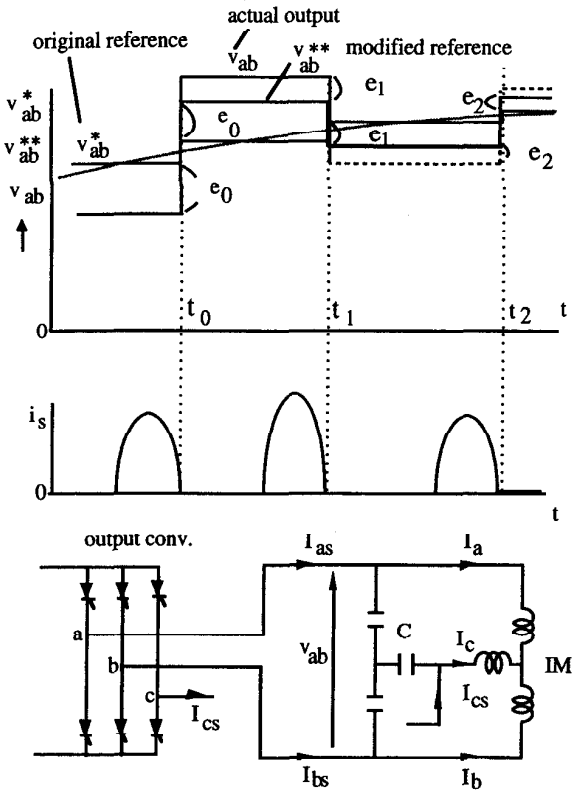


Fig. 5. Actual circuit configuration with current peak limiting.

are canceled out with the estimated charges. A detailed derivation of charges required to correct voltage errors at the output is given in the Appendix. Since the required charges ΔQ_{as}, ΔQ_{bs}, and ΔQ_{cs} follow the relation $\Delta Q_{as}+\Delta Q_{bs}+\Delta Q_{cs}= 0$ in eq. (11), three thyristors can be uniquely defined as shown in Table 1. For a particular "MODE" in Table 1, there appear two charge quantities with the same sign as shown in Table 2. Two thyristors in the output bridge are selected for firing at a time. Therefore, having decided the mode, the two thyristors to be fired next, are selected. For this purpose, the comparison between the magnitude of required charges is done. The phase thyristors with positive maximum and negative maximum required charges are selected. The relevant columns in Table 1 to which the selected charge belongs gives the two lines to be selected. Positive signs in Table 1 indicate the thyristors with a positive sign (top three thyristors) and the negative signs indicate the thyristors with the negative sign. Accordingly, the thyristors shown in black in Fig. 1 and Fig. 5 represent Mode 1 and it follows from Table 2 that at this instant ΔQ_{as} is larger than ΔQ_{bs}.



(definition of voltages and currents)

Fig. 6. Output voltage control.

MODE	ΔQ_{as}	ΔQ_{bs}	ΔQ_{cs}
1	+	+	−
2	+	−	+
3	−	+	+
4	−	−	+
5	−	+	−
6	+	−	−

Table 1. Polarity combinations of required charges.

+ Positive Charge
− Negative Charge

MODE	ΔQ_{as}	ΔQ_{bs}	ΔQ_{cs}
1	+		−
		+	−
2	+	−	
		−	+
3	−		+
	−	+	
4	−		+
		−	+
5	−	+	
		+	−
6	+	−	
	+		−

Table 2 Combinations of triggering thyristors for the modes of Table 1.

4.2 Input Converter Control

The input converter involves I_d control with reference I_{dref} which is determined by the required charges. Hence, this system uses a current feedback loop from the output to the As the load increases, system needs a larger I_d for the energy balance. In the implementation of the system, adjustment of I_d can be achieved by a simple feedback criterion that uses comparison of charges. It should be noted that if the thyristor threshold voltage V_{th} is

defined in which case the charge Q afforded by a single current pulse is roughly calculated by the bias current I_d. Therefore, to maintain an energy balance between input and output, an adequate I_d should be selected to balance the required charge Q_{req}. for the converter in addition to the voltage feedback used in the control of output converter. Fig. 8 shows the tendencies of Q and Q_{req} according to biasing current I_d which is normalized by the amplitude I_0 of output motor current. To the left of the balancing point P in Fig. 8, the possible charge Q is less than the required value Q_{req}, in which case Q is not sufficient to correct the errors and the motor currents are not smooth. When I_d is increased beyond the balance point, the system has a higher capability of correcting errors but the ripple in the output voltage increases. Hence, I_d control should be implemented so as to balance Q with Q_{req}, i.e., $I_d / I_0 \cong 2$. Therefore, the thyristors in the input converter should be switched to have the polarity of the output voltage E as,

(i) If $Q < Q_{req}$, input DC voltage is switched to + E; to increase I_{dref}

(ii) If $Q > Q_{req}$, input DC voltage is switched to - E, to decrease I_{dref}

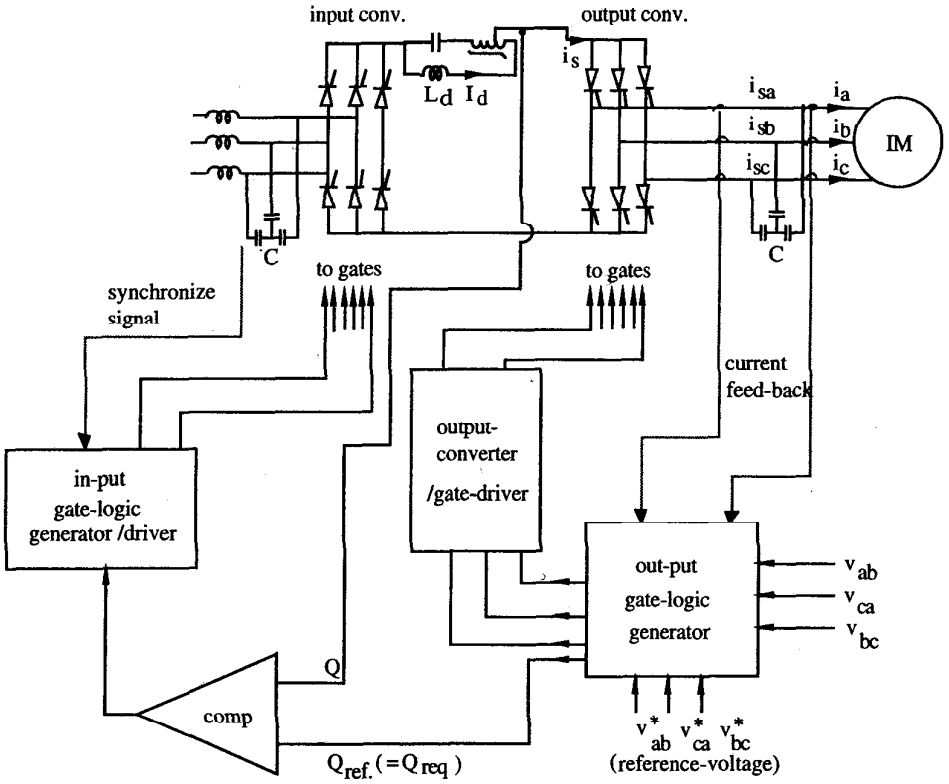


Fig.7. Control diagram of overall system

The voltage E depends on the input three phase voltages and the selection of triggering phases is performed as the same manner as in [4] to have simultaneous unity power factor and sinusoidal input current.

4.3 Other Calculated Results

Figure 9 shows the tendency of the pulse frequency and the ripple voltage in the output. In this figure, when I_d increases, the pulse frequency increases because of less dt [the interval between pulses in Fig. 2 (d)] and the output ripple voltage V_{ripple} increases because of the increased supply of charge. It also shows that the larger filter capacitor C_f causes smaller

voltage ripple in the output. In Fig. 8, it is demonstrated that as dt decreases according to the increase of I_d, the required per-pulse-charge Q_{req} with constant output current I_0 also decreases before the balancing point P, whereas the charge Q_{req} again increases after P because of excessive regulation by an excessive supply of charge. Figure 10 shows the dependencies of the peak voltage stresses across the resonant capacitor and across the thyristors. The figure also shows that V_{ripple} depends on the increase of capacitor C_L. According to the increase of C_L, smoother motor current and less voltage stresses on resonant elements and switches clearly result. In Fig. 11, simulated waveforms are shown. In Fig. 11 (a) pulses are shown with very small amplitude fluctuation compared with that of the previous prototype system [2]. Figure 11 (c) and (d) show the output voltage and current. Both are clearly well regulated and have sinusoidal waveform.

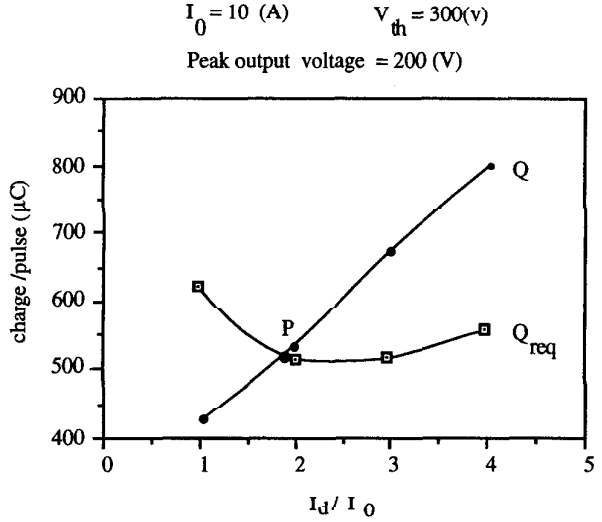


Fig. 8. Dependencies of Q_{cal} and Q upon I_d.

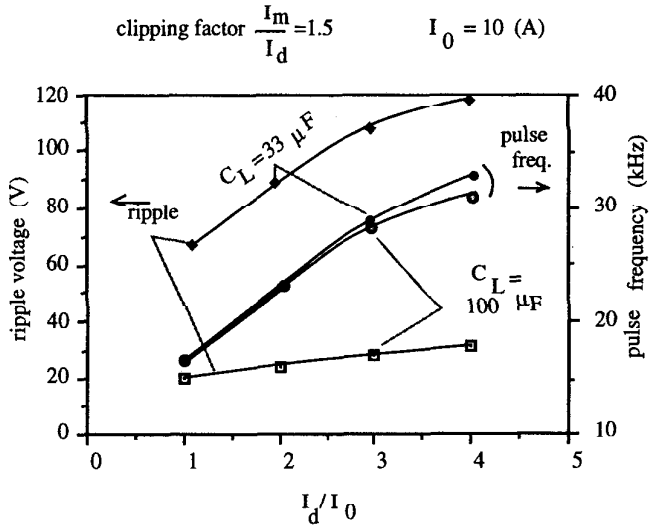


Fig. 9. Dependencies of ripple voltage and pulse frequency upon I_d.

5. CONCLUSION

In this paper, a new current-peak limiting scheme was proposed by utilizing a simple saturable ferrite core in place of the resonant inductance. The principles of the pulse limiting and the simplification of the circuit were performed and the control strategies adopted have been discussed. A new method for establishing the switching function and a feedback method for selecting optimum biasing current, have also been presented. Although a trimming procedure or circulating mode is not used, this system provides stable and good output current regulation in straightforward, simple manner.

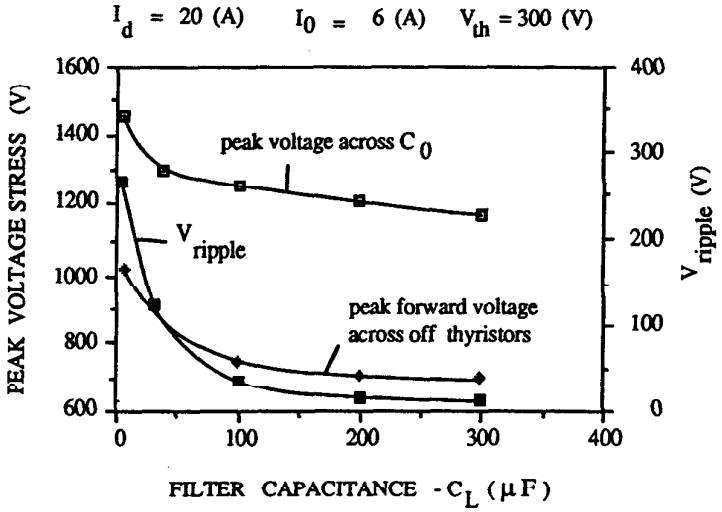


Fig. 10. Voltage stresses.

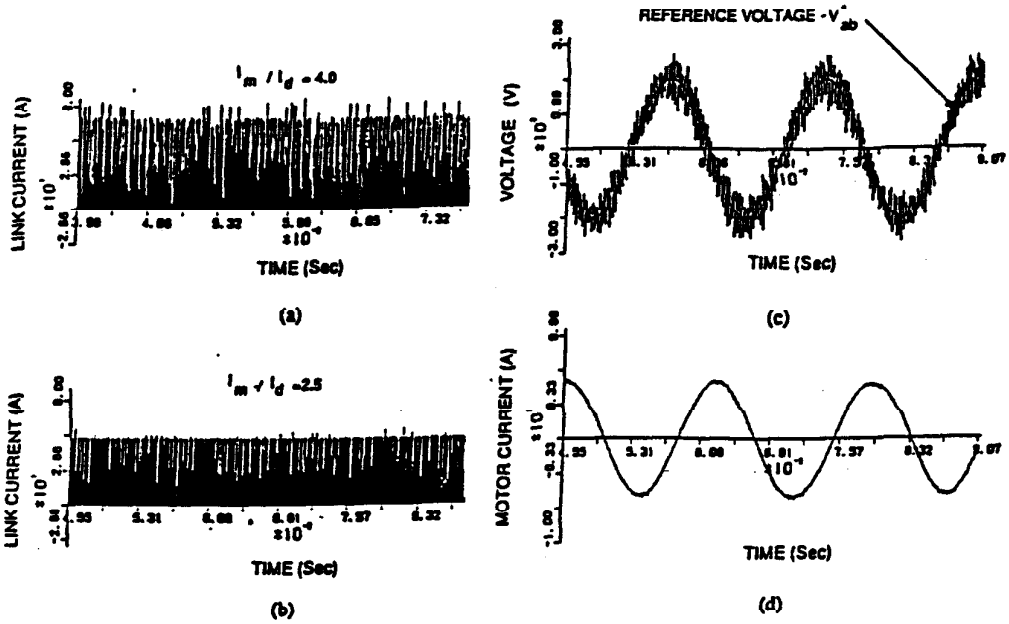


Fig. 11 Simulated Waveforms

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7. APPENDIX 1

Trade-off study of switching losses vs. core losses

The flux pulsation in the saturable core introduces an additional loss component to the system, and therefore, the core-loss should be maintained much lower than the switching loss eliminated by the soft switching, inorder to justify the low overall-loss. Low core-loss, high initial permeability, low saturation flux density materials, such as Supermalloy, Metglas Alloy 2714A, or 48 Alloy[5] would be an ideal selection for the above saturable core. The converter is expected to be operating at an average switching frequency of 25 kHz (thyristor limitation). Now let us consider the supermalloy toroidal core with the following data for our loss comparison.

1) Core type: Magnetics. 5_066 (toroidal, supermalloy) [5]

2) Value of the inductance, $L_0 = 5\ \mu H$

3) No. of cores in parallel = 2,

4) Saturation flux density of 0.7 tesla is assumed for supermalloy [6]

5) Wire size AWG 10 - Litz (worst case DC current of 40 A is assumed quite adequate for a threephase output of 500W, used in the comparison).

At 25 kHz, total core losses for 1/2 mil supermalloy, considering the fact that the B-H loop traverses nearly half of the complete loop as shown in Fig.3, is in the order of 60 (W). In order to compare the losses in the hard-switched version and the soft-switched counter part of the current source type, thyristor switches are replaced by GTO'S. In essence, the hard switch topology to compare would be the one described in the literature[7]. Our intention here is not to perform elaborate loss comparison scheme, but to have a rough estimation of probable losses, for justifying the low overall-loss of the soft-switched, current-sourced version described above. It is assumed here that the loss data of a GTO in

current-sourced version described above. It is assumed here that the loss data of a GTO in the zero voltage topology[8], can be closely adapted as representative loss data for the zero current-switched topology presented herein, for they are duels of each other (how closely follows the loss data adapted, is in reality have a bearing on the switching device type as well as the topology).

It has been demonstrated in the literature[8] that for the same power loss a frequency gain of 20:1 could be achieved by the soft-switched topology. It should be noted at this point that for those converters, which do not facilitate true PWM operation, an adequate pseudo-PWM scheme can be introduced over an effective period of three consecutive pulses. It can be seen from the above data that given the spectral requirement of the output waveformes, frequency gain of three can be easily adopted while operating way below the thermal limit of the switches. Therefore, soft switching scheme with GTO's (or thyristors) can handle more power than the hard switched counterpart, which reaches its thermal limit earlier.

7.1 Experimental data:

Soft switching

switching frequency	= 25 kHz
Total loss in two GTO's and Diodes	= 52.5 W
Output power of the test circuit	= 500 W

Hard switching

Switching frequency	= 1.1 kHz
Total losses in two GTO's	= 50.5 W
Output power of the test circuit	= 500 W

7.2 Loss comparison of hard switched converter and saturable core soft-switched converter

Considering the fact that the switching-loss is proportional to the switching-frequency and the soft switched converter needs roughly a switching frequency three times as high, for comparable output performances as its hard-switched converter, the switching loss of the soft-switched inveter side can be estimated as,

$$6 * \frac{52.5\ (W)}{25\ (kIIz)} * 3\ (kHz) = 37.8\ (W)$$

From the core loss data [5], at a switching frequency of 3kHz, the Core losses would become;

- Core losses introduced by the saturable core at 3 kHz = 16 (W)
- Total loses = 54 (W)
- Hard-switched counterpart at 1.1 kHz will generate a total loss of;

$$6 * 50.5\ (W) = 303\ (W)$$

Therefore, it could be seen that even with the introduction of the saturable core, losses can be kept lower than in the hard switched version. As the power level of the converter pushes further up, the soft-switched power converters would be favorable.

8. APPENDIX 2

8.1 Required Charge

As shown in Fig. 6, assuming average currents to flow in all phases simultaneously,

$I_{as} + I_{bs} + I_{cs} = 0$

$$\Delta V_{ab} = (I_{as} - I_a - I_{bs} + I_b) \Delta t / C_L$$

$$\Delta V_{cb} = (-I_{bs} + I_b + I_{cs} - I_c) \Delta t / C_L$$

$$\Delta V_{ac} = (- I_{cs} + I_c + I_{as} - I_a) \Delta t / C_L \qquad (8)$$

Defining,

$$I_a \Delta t = \Delta Q_a$$

$$I_{as} \Delta t = \Delta Q_{as}$$

$$\Delta V_{ab} C_L = \Delta Q_{ab} \qquad (9)$$

(similar notations were adopted for other phases)

Substituting (9) into (8) and solving for ΔQ_{as}, ΔQ_{bs}, ΔQ_{cs} the following equations are derived.

$$\Delta Q_{as} = (\Delta Q_{ab} + \Delta Q_{ac} - \Delta Q_b - \Delta Q_c + 2 \Delta Q_a) / 3$$

$$\Delta Q_{bs} = (- \Delta Q_{ab} - \Delta Q_{cb} - \Delta Q_a - \Delta Q_c + 2 \Delta Q_b) / 3$$

$$\Delta Q_{cs} = (\Delta Q_{cb} - \Delta Q_{ac} + 2 \Delta Q_c - \Delta Q_a - \Delta Q_b) / 3 \qquad (10)$$

Equation (10) indicates that

$$\Delta Q_{as} + \Delta Q_{bs} + \Delta Q_{cs} = 0 \qquad (11)$$

so that the triggering thyristors can be uniquely defined as shown in the Table 1.