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A High Performance Generalized Discontinuous PWM Algorithm

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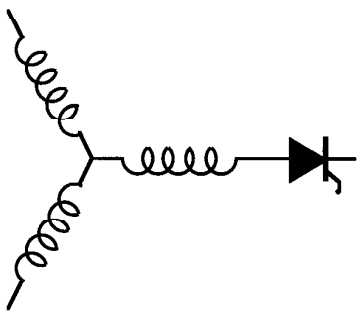

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Abstract— **In this paper a Generalized Discontinuous Pulse Width Modulation (GDPWM) method with superior high modulation operating range performance characteristics is developed. An algorithm which employs the conventional space vector PWM method in the low modulation range, and the GDPWM method in the high modulation range is established. As a result, the current waveform quality, switching losses, voltage linearity range and the overmodulation region voltage gain of a PWM-VSI drive are on-line optimized as opposed to conventional modulators with fixed characteristics. Due to its compactness, simplicity, and superior performance, the algorithm is suitable for most high performance PWM-VSI drive applications. The paper provides detailed performance analysis of the method and compares it to the other methods. The experimental results verify the superiority of this algorithm to the conventional PWM methods.**

I. Introduction

Voltage Source Inverters (VSIs) are widely utilized in AC motor drive, utility interface, and uninterrupted power supply applications as means for DC ⇔ AC electric energy conversion. Shown in Figure 1, the classical VSI has a relatively simple structure and generates a low frequency output voltage with controllable magnitude and frequency by programming high frequency voltage pulses. Carrier based PWM methods employ the "per carrier volt-second balance" principle to program a desirable inverter output voltage waveform. Two main implementation techniques exist. In the direct digital technique, the complex plane voltage vector concept is utilized to calculate the duty cycle of the inverter switching devices and digital counters utilize the duty cycle information to program the switch gate signals [1]. In the triangular intersection technique, the reference voltage (modulation) waveforms are compared with the triangular carrier wave and the intersections define the switching instants [2]. Although the early triangular intersection implementations employed analog circuits, low cost digital microelectronics have proven the viability of digital hardware/software implementation.

The absence of neutral wire in star connected loads provides a degree of freedom in determining the duty cycle of the inverter switches. In the direct digital implementation the degree of freedom appears as the partitioning of two zero states [3]. In a triangular intersection implementation, this degree of freedom appears in choosing the modulation wave because adding a signal (zero sequence signal) to the three phase reference signals does not change the inverter output line-to-line voltage per carrier cycle average value. The zero sequence signal injection technique block diagram is illustrated in Figure 2. In both direct digital and triangular intersection methods the voltage

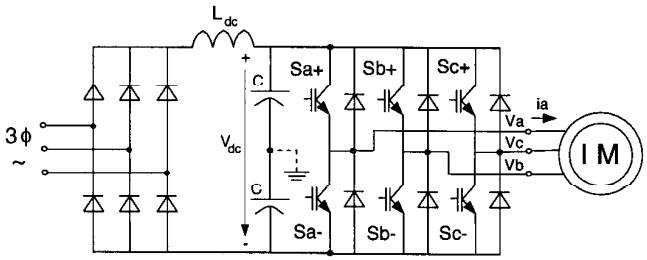

Fig. 1. Circuit diagram of a diode rectifier front end type PWM-VSI drive.

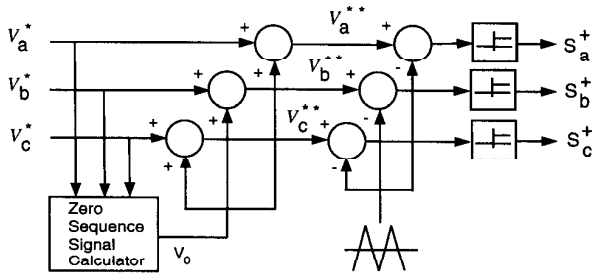

Fig. 2. Triangular intersection technique based PWM employing the zero sequence injection principle.

linearity, waveform quality (current ripple), and switching losses are all influenced by the choice of the zero sequence signal (zero state partitioning). Recognizing this property, many researchers have been investigating high performance PWM methods. With performance and implementation simplicity being the main criteria, only a few of the many developed PWM methods gained acceptance [4].

Due to its simplicity, the Sinusoidal PWM (SPWM) method has found a wide range of applications since the early development of PWM-VSI technology [2]. Employing the zero sequence signal injection technique, King developed the Third Harmonic Injection PWM (THIPWM) method [5] and illustrated the method is linear between 0% and 90.7% of six-step voltage value, and therefore, is superior to SPWM which is only linear between 0% and 78.5%. About two decades later, the method was investigated in more detail by Houldsworth and Grant [6]. Utilizing a discontinuous type of zero sequence signal, Schörner developed a modulation method with discontinuous modulation waves (later named as Discontinuous PWM (DPWM) method) which also provides a wider linearity range than

SPWM [7]. This modulation method was thoroughly investigated by Depenbrock and its superior voltage linearity range, reduced switching loss, and the superior high modulation range current waveform quality were illustrated [8]. However, the poor low modulation range performance (the narrow pulse width problems and poor current waveform quality) and implementation complexity has limited the application of this modulator. Employing the complex voltage vector for "per carrier volt-seconds control" Pfaff et al. established the Space Vector PWM (SVPWM) [9] method which has superior waveform characteristics to SPWM and THIPWM and suits the high performance vector control algorithms of PWM-VSI drives. Skudelny et al. later thoroughly investigated the SVPWM method and illustrated its superior performance characteristics [1]. Subsequently, Ogasawara et al. developed a modified SVPWM method with superior high modulation range waveform quality and reduced switching loss characteristics suitable for induction motor drives. The modulation waveforms of these modulators and several other popular PWM methods [10, 11] are shown in Figure 3 along with their zero sequence signals. In the figure, unity the triangular carrier wave gain is assumed and the signals are normalized to $\frac{V_{dc}}{2}$. Therefore, $\pm\frac{V_{dc}}{2}$ saturation limits correspond to ± 1. Since the performance of a modulator is voltage utilization (modulation index) dependent, at this stage a modulation index definition is required.

Modulation Index: for a given DC link voltage V_{dc}, the ratio of the fundamental component magnitude of the line to neutral inverter output voltage, V_{1m}, to the fundamental component magnitude of the six-step mode voltage, $\frac{2V_{dc}}{\pi}$, is termed the modulation index M_i [4]:

$$M_i = \frac{V_{1m}}{\frac{2}{\pi}V_{dc}} \tag{1}$$

As discussed in detail in references [4, 11], the performance of the popular PWM methods is modulation index dependent and no single modulator provides a satisfactory performance over a very wide modulation range. Therefore, a high performance drive with a wide operating range must combine at least two PWM methods and on-line select a proper modulator as a function of the modulation index. In the low modulation range the overall performance of SVPWM is superior to most other methods. The modulation waveform of SVPWM is easy to generate also [12]. Therefore, SVPWM is the natural choice for operating in the low modulation region. In the high modulation region DPWM methods are superior to SVPWM and the other PWM methods with continuous modulation waveforms which will all be grouped as Continuous PWM (CPWM) methods. However, the DPWM method of choice depends on the performance criteria and no modulator has an overall superior performance. The switching losses, waveform quality and voltage linearity are different in each DPWM method. Therefore, selecting only two PWM methods results in a less than optimal performance, while employing more than two PWM methods increases the algorithm complexity. Therefore, a DPWM method with controllable characteristics is a superior approach.

This paper develops a high performance Generalized DPWM (GDPWM) method and an algorithm combines GDPWM with SVPWM to maximize the drive performance in the whole modulation range. First the GDPWM method is described, then the modulator characteristics are studied and compared to the other popular methods to illustrate the performance superiority. Finally, laboratory test results are illustrated to verify the capabilities of the method. The paper will focus on the triangular intersection implementation (digital hardware/software based), however the algorithm can be employed in a direct digital implementation also.

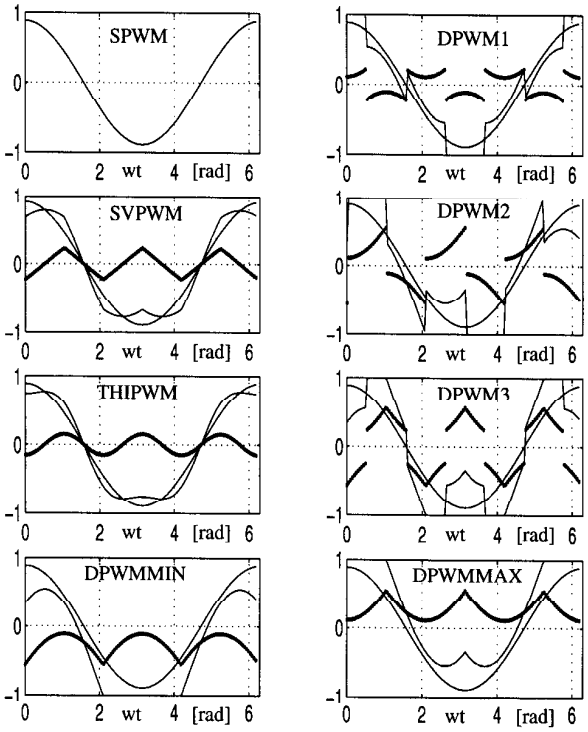

Fig. 3. Modulation waveforms of the popular PWM methods ($M_i = 0.7$).

II. The Generalized Discontinuous PWM Method

A careful examination of the DPWM1 and DPWM2 modulation waveforms of Figure 3 indicates the shape difference between these two modulation waveforms arises from the 30° phase difference between the two unmodulated 60° segments of DPWM1 and DPWM2. However, the 60° unmodulated segments can be located at any position provided that the modulator voltage linearity is not lost before the theoretical limit ($M_{imax} = \frac{\pi}{2\sqrt{3}}$) and DPWM1 and DPWM2 are special cases of a family of DPWM modulation waves which will be called the Generalized DPWM (GDPWM) method modulation waves.

The GDPWM method has two 60° unmodulated segments and its zero sequence signal generation method is illustrated in Figure 4. For illustration purposes, the triangle carrier wave peak to peak voltage is up-scaled to the VSI DC link voltage V_{dc}. Therefore, the modulator saturates at a signal value larger than $\pm\frac{V_{dc}}{2}$. It is useful to define the modulator phase angle ψ increasing from the intersection point of the two modulation waves at $w_e t = \frac{\pi}{6}$ as shown in Figure 4. From ψ to $\psi + \frac{\pi}{3}$, the zero sequence signal is the shaded signal which is equal to the difference between the saturation line ($\frac{V_{dc}}{2}$) and the reference modulation signal which passes the *maximum magnitude test*. In the *maximum magnitude test*, all three reference modulation signals are phase shifted (lagging) by $\psi - \frac{\pi}{6}$, and of the three new signals, the one with the maximum magnitude determines the zero sequence signal. The difference between the original reference that passes the largest magnitude test and the saturation line becomes the zero sequence signal. Adding this zero sequence signal to the three original modulation waves, the GDPWM waves are generated.

Figure 5 illustrates the modulation and zero sequence waveforms

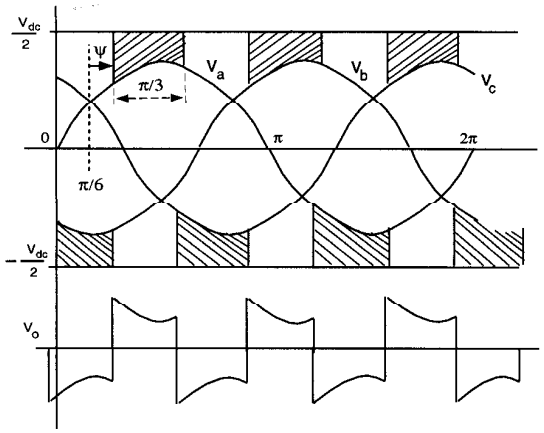

Fig. 4. Generalized DPWM zero sequence signal generation method: ψ is the only control parameter.

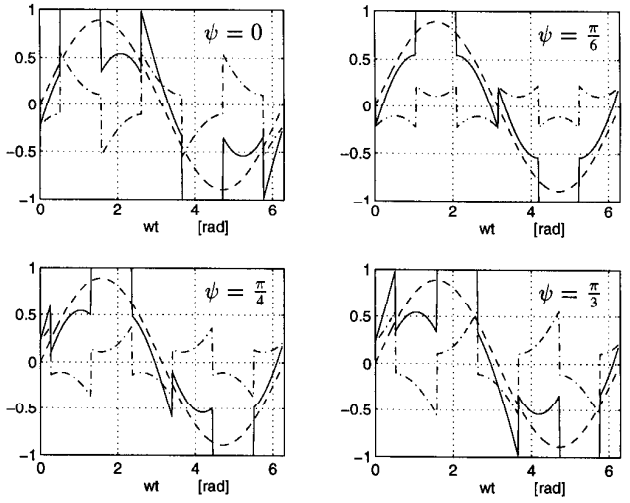

Fig. 5. GDPWM method modulation waves("–"), their zero sequence signal ("-.") and the fundamental component ("-") for $M_i = 0.7$ and four different modulator phase angle values.

for four different ψ values for $M_i = 0.7$. Notice that DPWM1 corresponds to $\psi = \frac{\pi}{6}$ and DPWM2 to $\psi = \frac{\pi}{3}$. In order to obtain the maximum possible voltage linearity range the control range of ψ is confined to the interval $[0, \frac{\pi}{3}]$. The DPWM1 region is quite attractive in PWM-VSC utility interface applications and AC Permanent Magnet (PM) motor applications where the load power factor is near unity, while the DPWM2 end provides attractive performance characteristics for lagging loads near 30° such as induction motor drives. The $\psi = 0$ region is suitable for operating an induction machine as a generator. In all these cases, the phase that conducts the largest current is not switched. Therefore, the inverter switching losses are significantly reduced. The GDPWM method requires only a small number of multiplications and comparisons to yield the proper zero sequence and modulation wave signals. The only control parameter of GDPWM, ψ, strongly affects the inverter switching losses, waveform quality, and overmodulation region fundamental component voltage gain. The following sections investigate these characteristics.

III. Waveform Quality

Linear modulation range inverter output current harmonics of the carrier based PWM methods are concentrated at the carrier frequency and its sidebands. The waveform quality of the inverter currents is determined by the RMS value (per fundamental cycle) of these harmonics. Since each zero sequence signal (zero state partitioning) and each modulation index value results in a unique inverter output voltage waveform, the harmonic current waveform and therefore its RMS value is unique for each modulator and modulation index value.

Since the discussed zero sequence injection PWM methods have periodic zero sequence signals, the switching signals and the harmonic currents are periodic also. With the assumption that the carrier frequency is larger than the fundamental frequency by at least an order of magnitude and the load high frequency model can be approximated with an inductance, the harmonic current RMS value of these periodic waveform modulators can be closed form calculated as a function of the modulation index [11]. To obtain a load inductance and carrier frequency independent formula, the RMS harmonic current can be normalized to the single phase inverter maximum uniform harmonic current RMS value and the resulting Harmonic Distortion Factor (HDF) function is a polynomial which only depends on the modulation index.

The HDF of SVPWM, DPWM1, and DPWM2 are as follows [13].

$$\mathrm{HDF_{SVPWM}} = \frac{3}{2}(\frac{\pi}{4}\mathrm{M_i})^2 - \frac{4\sqrt{3}}{\pi}(\frac{\pi}{4}\mathrm{M_i})^3 + (\frac{27}{16} - \frac{81\sqrt{3}}{64\pi})(\frac{\pi}{4}\mathrm{M_i})^4 \quad (2)$$

$$\mathrm{HDF_{DPWM1}} = 6(\frac{\pi}{4}\mathrm{M_i})^2 - (\frac{8\sqrt{3}+45}{2\pi})(\frac{\pi}{4}\mathrm{M_i})^3 + (\frac{27}{8} + \frac{27\sqrt{3}}{32\pi})(\frac{\pi}{4}\mathrm{M_i})^4 \quad (3)$$

$$\mathrm{HDF_{DPWM2}} = 6(\frac{\pi}{4}\mathrm{M_i})^2 - \frac{35\sqrt{3}}{2\pi}(\frac{\pi}{4}\mathrm{M_i})^3 + (\frac{27}{8} + \frac{81\sqrt{3}}{64\pi})(\frac{\pi}{4}\mathrm{M_i})^4 \quad (4)$$

The exact relation between the HDF function and the phase "a" harmonic current RMS value, $\mathrm{I_{ah}}$, is as follows.

$$\mathrm{I_{ah}^2} = (\frac{\mathrm{V_{dc}}}{24\mathrm{L}_\sigma \mathrm{f_c}})^2 \times \mathrm{HDF(M_i)} \quad (5)$$

The HDF function of GDPWM method for any ψ value can be accurately approximated by interpolating the HDF of DPWM1 ($HD1$) and DPWM2 ($HD2$) which are its two end points. Since it is symmetric about $\psi = \frac{\pi}{6}$, the HDF of GDPWM (HDF_{GD}) can be written in two pieces as follows.

$$\mathrm{HDF_{GD}}(\psi) = \begin{cases} (\frac{6\psi}{\pi})HD1 + (1 - \frac{6\psi}{\pi})HD2 & 0 \le \psi \le \frac{\pi}{6}, \\ (2 - \frac{6\psi}{\pi})HD1 + (\frac{6\psi}{\pi} - 1)HD2 & \frac{\pi}{6} \le \psi \le \frac{\pi}{3} \end{cases} \quad (6)$$

Figure 6 shows the HDF curves of all the discussed PWM methods under constant inverter average switching frequency (HDF of DPWM methods is multiplied by $(\frac{2}{3})^2$). Since the difference between the HDF of DPWM1 and DPWM2 is at most 10-15 %, the HDF of GDPWM is not a strong function of ψ and the difference is only noticeable at the high modulation index range. As the HDF curves indicate the CPWM methods have better waveform quality in the low modulation range while the DPWM methods are superior in the high modulation range. Therefore, in order to have small current ripple, high performance PWM-VSI drives should employ at least two modulators and select a different modulator in each region. Utilizing the HDF formula, the transition point can be calculated according to the design criteria.

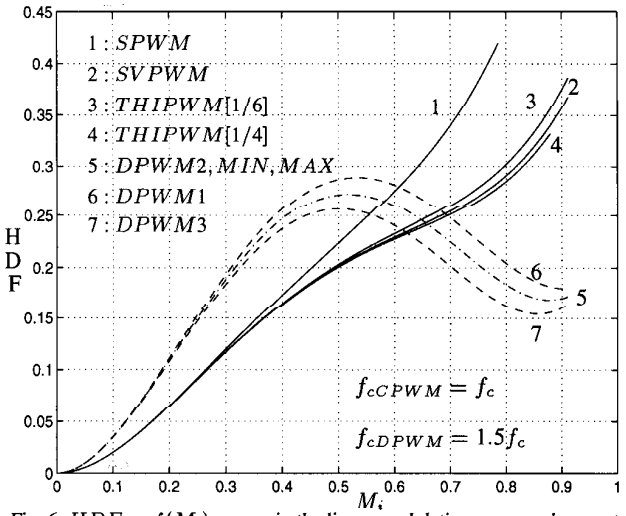

Fig. 6. $HDF = f(M_i)$ curves in the linear modulation range under constant inverter average switching frequency.

In the very low modulation index range all CPWM methods have practically equal HDF. However, as the modulation index increases the SPWM performance rapidly degrades while the remaining CPWM methods have practically equal HDF and maintain low HDF over a fairly wide range. Although the THIPWM method with minimum HDF ($v_{0opt} = \frac{V_{1m}}{4} \sin 3\theta$) [14] has theoretically smaller HDF than SVPWM and the conventional THIPWM ($v_0 = \frac{V_{1m}}{6} \sin 3\theta$), the difference is practically negligible, and the SVPWM modulation wave is easier to generate and has a slightly wider voltage linearity range [13]. Therefore, the SVPWM method is superior to all the discussed methods in the low modulation index range. In the high modulation index range as Figure 6 indicates the DPWM methods are superior to SVPWM and intersection point of the DPWM method of choice and the SVPWM HDF curves define the optimal transition point. Although in the high modulation range the DPWM3 method has less HDF than the other DPWM methods, the difference is not large and the DPWM method selection criteria can be based on the switching loss characteristics or voltage linearity characteristics which are stronger functions of the DPWM methods. Since it sweeps a wide range of modulation waveforms, the GDPWM method has the potential of optimizing these performance characteristics. Therefore, a clear understanding of the switching loss mechanism of DPWM methods and the voltage gain characteristics is required.

IV. Switching Losses

Inverter switching losses of the CPWM methods are not modulator type dependent, while the switching losses of DPWM methods are significantly influenced by the modulation method and load power factor. This is due to the fact that DPWM methods cease to switch each switch for a total of 120^0 per cycle and the location of the unmodulated segments with respect to the modulation wave fundamental component signal is modulator type dependent. Therefore, the load power factor and the modulation method together determine the time interval that the load current is not commutated. Since the switching losses are strongly dependent on and increase with the magnitude of the commutating phase current, selecting a suitable DPWM method can significantly contribute to the performance of the drive. Therefore, it is necessary to characterize and compare the switching losses of DPWM methods.

Assuming the inverter switching devices have linear current turn-on and turn-off characteristics with respect to time, the switching losses of a PWM-VSI drive can be calculated in a closed form formula [11, 15]. Although it is only a rough approximation, such a formula illustrates the device and load parameter dependency of the switching losses and assists developing the GDPWM switching loss reduction algorithm. With this assumption, the switching losses of an inverter switch can be calculated for a carrier cycle T_c and this function can be averaged over the fundamental cycle resulting in a power factor angle φ dependent formula. Defining P_o as the base power, P_{swave} as the per fundamental cycle average switching loss, and applying the principle to the GDPWM method, the following normalized Switching Loss Factor (SLF) function results.

$$P_o = \frac{V_{dc} I_{max}}{\pi T_c} \times (t_{on} + t_{off}) \tag{7}$$

$$SLF = \frac{P_{swave}}{P_o} \tag{8}$$

$$SLF_{GDPWM} = \begin{cases} 1 - \frac{1}{2}\sin(\frac{\pi}{3} + \psi - \varphi) & 0 \le \varphi \le \frac{\pi}{6} + \psi, \\ \frac{\sqrt{3}}{2}\cos(\frac{\pi}{3} + \psi - \varphi) & \frac{\pi}{6} + \psi \le \varphi \le \frac{\pi}{2} \end{cases} \tag{9}$$

In the P_o formula, t_{on} and t_{off} variables represent the turn-on and turn-off times of the switching devices, I_{max} represents the load current fundamental component maximum value, and ψ is the GDPWM phase angle. The SLF surface of GDPWM for $\varphi \ge 0$ is shown in Figure 7 and for $\varphi < 0$ the surface is symmetric with respect to φ. The three dimensional plot indicates that the switching losses of GDPWM can be minimized by controlling the modulator phase angle as a function of the load power factor angle. In the $-\frac{\pi}{6} \le \varphi \le \frac{\pi}{6}$ region, selecting $\psi = \varphi + \frac{\pi}{6}$ results in minimum switching loss value which is equal to 50 % of the CPWM methods. Outside this range, as the figure indicates, the minimum switching loss algorithm requires that the modulator phase angle be held at the boundary value of $\psi = \frac{\pi}{3}$ for positive φ (DPWM2) and at the value of $\psi = 0$ for negative φ.

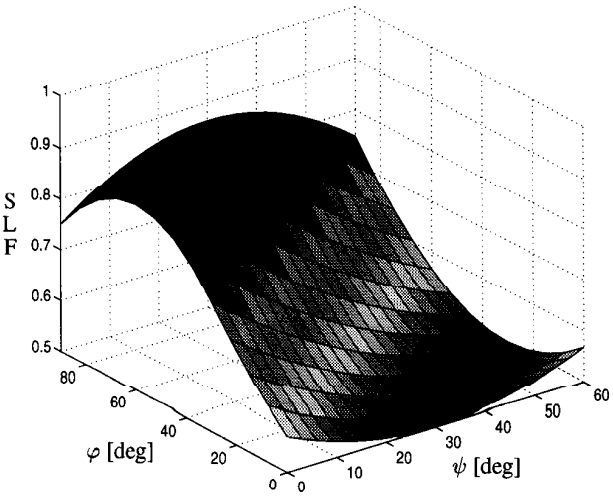

Fig. 7. $SLF = f(\psi, \varphi)$ function of the GDPWM method.

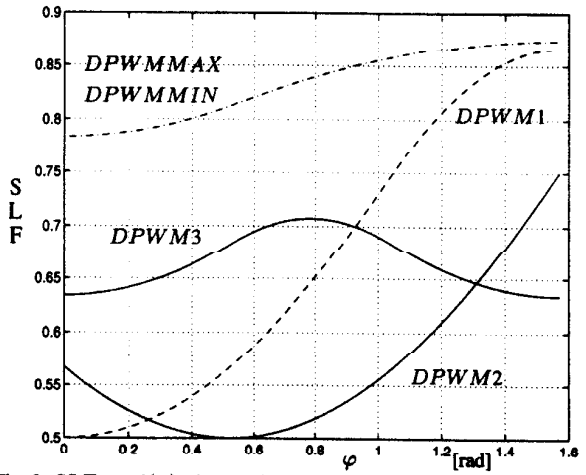

Fig. 8. $SLF = f(\varphi)$ characteristics of the popular DPWM methods under fixed carrier frequency constraint ($SLF_{CPWM} = 1$).

The switching loss performance superiority of the GDPWM method over the other DPWM methods can be observed in Figure 8. Comparing this SLF graph to the 3-D SLF graph of GDPWM, it becomes obvious that the optimum SLF of GDPWM is far superior to all the methods in a very wide range and only near 90° lagging/leading power factor conditions is the DPWM3 performance better than GDPWM. Typically PWM-VSI drives operate in the $-30° \leq \varphi \leq 30°$ range, therefore, the method has less switching losses than other methods for most practical applications.

When the performance criteria is only switching loss minimization, the GDPWM algorithm can utilize the load power factor information and select the ψ value which minimizes the SLF function and the zero sequence signal which unmodulates the inverter leg that conducts the largest current. However, as the linear modulation range expires, the nonlinear modulation range performance characteristics increasingly dominate drive performance and in addition to SLF and HDF, the inverter overmodulation voltage gain characteristics must be considered.

V. Overmodulation and Voltage Gain

As well known, when the modulation wave becomes larger than the triangular carrier wave, the inverter saturates and ceases to match the reference volt-seconds per carrier cycle, and a nonlinear reference-output voltage relation results. The region starting from the end of the linear region until the six-step operating point ($M_i = 1$) is called the overmodulation region. SPWM's linear modulation range ends at a modulation index of $\frac{\pi}{4} \approx 0.785$. With the exception of the THIPWM method with optimum HDF which looses linearity at $\frac{3\sqrt{3}}{7\sqrt{7}}\pi \approx 0.88$, the theoretical maximum linear modulation index for all of the discussed zero sequence injection PWM methods is $M_{Lmax} = \frac{\pi}{2\sqrt{3}} \approx 0.907$. For each modulator a unique nonlinear fundamental component voltage gain relation exists and this relation can be closed form calculated by means of Fourier analysis of the saturated modulation wave [13, 16]. For example, the gain function for DPWM1 is given as follows.

$$G_{DPWM1} = \frac{M_i}{M_i^*} = \frac{\sqrt{3}}{\pi} - \frac{1}{2} - \frac{1}{M_i^*} + \left(\frac{\pi}{4\sqrt{3}}\right)\frac{1}{M_i^{*2}} + \left(\frac{3}{\pi}\right)\arcsin\left(\frac{\pi}{2\sqrt{3}M_i^*}\right) + \left(\frac{\sqrt{3}}{2M_i^*}\right)\sqrt{1 - \left(\frac{\pi}{2\sqrt{3}M_i^*}\right)^2} \qquad (10)$$

Figure 9 shows the voltage gain characteristics of various PWM methods [13, 16]. The gain was intentionally drawn as a function of M_i (instead of the reference value M_i^*) so that the characteristics of all the modulators could be illustrated in detail in one graph. As the figure indicates, except DPWM1 all the modulators experience a substantial gain reduction in the overmodulation range. In order to operate in the overmodulation range, such modulators require a wide modulation signal range (increased word length in digital systems and a wide voltage range in analog systems), however, this either increases the processor cost or reduces modulation waveform resolution, which degrades performance. In current controlled drives, modulator gain reduction in addition results in reduced current loop gain and poor dynamic performance [13]. Therefore, the DPWM1 voltage gain characteristic is superior to all the other modulators [16].

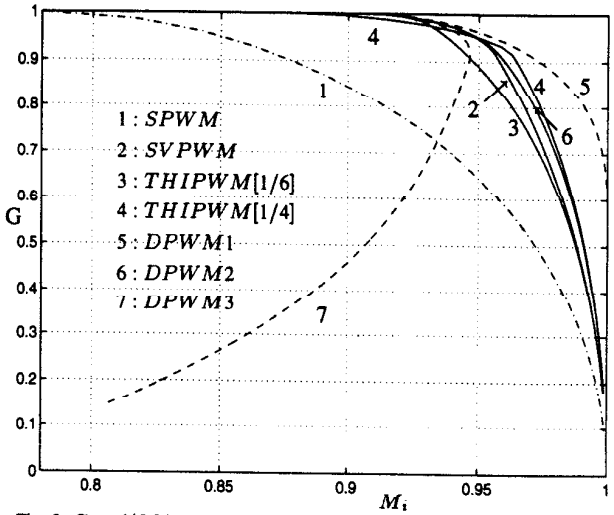

Fig. 9. $G = f(M_i)$ voltage gain characteristics of the popular modulators.

As DPWM1 and DPWM2 voltage gain characteristics indicate, the GDPWM method voltage gain is a function of ψ and $\psi = \frac{\pi}{6}$ provides maximum gain (DPWM1). In particular in the high end of the overmodulation range, a small deviation from $\psi = \frac{\pi}{6}$ value results in a large gain reduction. Therefore, the $\psi = \frac{\pi}{6}$ is the optimal gain point and should be selected to fully utilize the resolution range of the digital/analog PWM circuit. Closed form modeling of the ψ dependent GDPWM voltage gain is difficult and impractical, hence will be omitted.

In addition to the voltage gain characteristics, the overmodulation range waveform quality and switching loss characteristics of different modulators are also important and must be investigated. In the lower end of the overmodulation range ($M_i \leq 0.95$) the unmodulated signal segments slowly increase with the modulation index. In this region the superior HDF and SLF characteristics of the GDPWM method are partially retained. The volt-second errors generated in the unmodulated segments result in subcarrier frequency harmonic currents and the drive performance gradually degrades. As the modulation index increases and the six step mode is approached the performance is rapidly lost. With the exception of the voltage gain characteristics, the performance of all the modulators (DPWM and CPWM) equally degrade and the subcarrier frequency inverter harmonics dominate the

drive performance. Therefore, in the lower overmodulation region it is advantageous to select GDPWM and select ψ such that SLF and HDF are minimized, and in the higher overmodulation region transition to $\psi = \frac{\pi}{6}$ value is required. However, transition between $\psi = \frac{\pi}{6}$ and the SLF/HDF optimizing ψ value must be free of oscillation in order to avoid generating harmful low frequency voltage/current harmonics. If the drive is sensitive to low frequency harmonics, the transition to $\psi = \frac{\pi}{6}$ must occur at the end of the voltage linearity region.

In applications that require large inverter blanking time (high power drives) or minimum pulse width control (high switching frequency drives, high power drives) the voltage linearity is significantly influenced by the blanking time and minimum pulse width. The practical voltage linearity limit of a PWM-VSI drive with t_d blanking time and $f_c = \frac{1}{T_c}$ carrier frequency can be calculated as follows [13, 16].

$$M^t_{Lmax} = (\frac{\pi}{2\sqrt{3}}) \times (1 - K_m \frac{2t_d}{T_c}) \tag{11}$$

In the above formula K_m is the modulator coefficient and its value is 1 in DPWM methods and 2 in CPWM methods. When minimum pulse width control is employed and voltage pulses narrower than t_{min} are dropped the linearity limit can be found from the above formula by replacing $2t_d$ by t_{min}. Since the reduction in the voltage linearity range is proportional to $\frac{2t_d}{T_c}$ or $\frac{t_{min}}{T_c}$ in many practical applications gain reduction is experienced at a substantially low modulation index values. Although the blanking time only partially affects the gain, the minimum pulse width based gain reduction can be significant. Therefore, with 50 % less reduction in voltage linearity range than the CPWM methods, the DPWM methods have an additional advantageous characteristics and it becomes clear that the GDPWM method is the natural approach for operating in the overmodulation range.

VI. A HIGH PERFORMANCE PWM ALGORITHM

The performance analysis conducted thus far clearly shows selecting SVPWM in the lower end of the linear modulation range, and GDPWM in the remainder results in a superior overall performance when compared to the conventional PWM methods. To maximize the drive performance, the transition point from SVPWM to GDPWM and the ψ value of GDPWM must be properly selected. As the previous sections indicate, the transition point from SVPWM to GDPWM is determined by the waveform quality characteristics while the GDPWM modulator phase angle ψ is determined from the switching loss and voltage gain characteristics. Figure 10 shows the on-line modulator selector flow diagram of the novel algorithm. Simple in structure and computational procedure, the algorithm requires only two transition modulation indices and the load power factor angle information as optimization parameters.

The value M_{itr2} is determined by the modulator linearity limit which can be easily calculated from (11). However, the optimal value of M_{itr1} depends on the carrier frequency value as well as the SLF and HDF characteristics. Depending on the carrier frequency value, three practical cases can be distinguished.

1) $f_c = const.$: If the carrier frequency of the drive is fixed, then the HDF curves of SVPWM will be superior to GDPWM until M_{itr2}. As a result, transition from SVPWM to GDPWM at a point before M_{itr2} implies an increase in the waveform distortion. However, the switching losses can be reduced by as much as 50%. Depending on the application, as waveform quality requirements diminish the trade-off relations between the SLF and HDF characteristics along with (5) and (7) can be utilized to calculate the M_{itr1} value precisely.

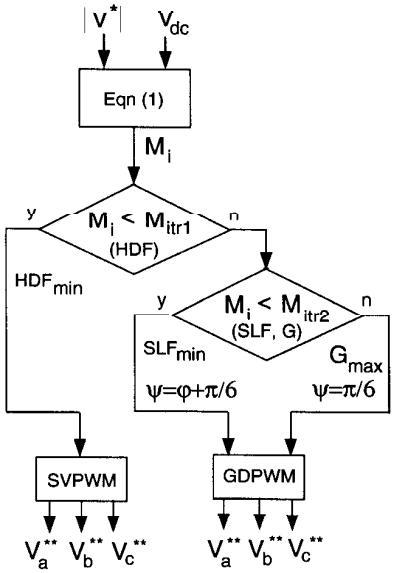

Fig. 10. The combined high performance PWM algorithm flow diagram.

2) $f_{swave} = const.$: In this case, the carrier frequency for SVPWM case is selected as f_c, and for GDPWM as $1.5f_c$, such that the inverter average switching frequency, f_{swave} remains constant. In this case, the HDF curves of Figure 6 indicate the intersection point of SVPWM and GDPWM (roughly average value of DPWM1 and DPWM2) is at $M_{itr1} \approx 0.65$. Therefore, this M_{itr1} value minimizes the HDF of the drive, and under this condition the switching losses in the GDPWM mode are reduced by at most 25% when compared to the SVPWM mode.

3) $P_{swave} = const.$: In this case, the carrier frequency for SVPWM case is selected as f_c, and for GDPWM as $2f_c$, such that the inverter switching losses P_{swave} remain constant. Scaling the HDF curves according to the increase in the carrier frequency, it can be found that the intersection point of the SVPWM and GDPWM method now occurs near a modulation index of 0.3. Therefore, $M_{itr1} \approx 0.3$ can be selected for transition. However, SVPWM is not fully utilized, and in applications with small current ripple requirements the switching loss function must yield to allow SVPWM to be active over a wider modulation range.

The full PWM algorithm can be easily and efficiently programmed in a microprocessor or a Digital Signal Processor (DSP) leading to a low cost high performance drive. The algorithm can also be employed in controlling both sides of back-to-back VSI-VSC drives to reduce the software complexity and optimize the drive performance over a very wide modulation range. Since the transition from SVPWM to GDPWM only involves a zero sequence signal, motion control and load currents are oscillation free, and only the harmonic content changes. The only costs in realizing the optimal modulator are increased DSP software code and small increments in computational requirements. Thus, the algorithm is suitable over a wide range of applications where low cost, high performance, and high energy efficiency are in demand. Employing one algorithm and providing user programmability, such a drive fits all the practical applications including induction machines, permanent magnet AC machines, and VSC utility interface and obtains superior performance.

VII. Experimental Results

The novel high performance PWM algorithm was tested in the laboratory on a constant volts per hetz controlled 5 HP induction motor drive. The VSI utilizes a diode rectifier front end with a DC bus voltage of 620 V. The PWM-VSI drive control board was fully digital and it employed a 40 MHz, 24-bit fixed point DSP. The PWM algorithm employed the triangular intersection technique and a simple software code generated the modulation signals. The carrier frequency was fixed at 5 kHz and modulation waves were fed to the digital PWM counters to generate the VSI gate switch signals. The drive had $4\mu s$ blanking time, and through symmetric blanking time compensation the voltage pulses were precisely generated. A minimum pulse width control algorithm was employed and through a Pulse Elimination Method (PEM), voltage pulses less than $12\mu s$ were eliminated.

The DSP computed the SVPWM zero sequence signal by comparing the three reference signals and multiplying the signal with the smallest magnitude by 0.5. Adding the zero sequence to the references, the SVPWM modulation wave was obtained. The GDPWM modulation waveforms were computed by the algorithm described. The GDPWM method employed minimum SLF control algorithm ($\psi = \varphi + \frac{\pi}{6} \leq \frac{\pi}{3}$ for motoring) until the end of the linear region. The phase difference between a modulation wave and the corresponding phase current was measured to estimate the power factor angle. In the overmodulation region an inverse gain compensation was employed. A DC bus voltage disturbance decoupling algorithm was also employed to reduce the sensitivity of the drive to DC bus voltage variations.

Since the carrier frequency was fixed at 5 kHz, the transition point from SVPWM to GDPWM was determined by the linearity limit of SVPWM (with $12\mu s$ PEM control) which was calculated from (11) as $M_{itr1} = 0.8$. However, the experimental observation suggested that the current waveform quality with SVPWM did not immediately degrade and was slightly better than with GDPWM until approximately 0.81. Therefore, the transition value was selected as $M_{itr1} = 0.81$. Figure 11, Figure 12, and Figure 13 illustrate the modulator and motor phase current waveforms immediately before, during, and after transition ($M_i = 0.79, 0.81, 0.82$) under 50% of the rated motor torque (T_{eR}). The current waveform quality of all three figures, in particular the peak current ripple, is practically the same. Since the speed reference signal of the drive is fed to the DSP through an A/D converter, at the transition modulation index operating point ($M_i = M_{itr1}$) a small reference signal noise results in an oscillation between SVPWM and GDPWM. However, this is a zero sequence signal oscillation and it only affects the carrier frequency harmonic content of the motor current and as Figure 12 shows, it does not disturb the motor current fundamental component and therefore, the motion quality. Since the carrier frequency is constant, changing from SVPWM to GDPWM results in significant reduction in switching losses. With the power factor angle at this operating point being larger than 30°, the SLF curve in Figure 7 indicates the losses are reduced by at least 40% when compared to SVPWM. Confirming this improvement, measurements showed several degrees decrease in the heat sink temperature.

The GDPWM linear modulation limit with $12\mu s$ PEM control is $M_{Lmax} = 0.85$ (calculated from (11)), thus the transition modulation index value becomes $M_{itr2} = 0.85$. However, experimental observation indicated transition at 0.86 modulation index value did not cause performance degradation. Therefore, $M_{itr2} = 0.86$ was selected. Within its voltage linearity range, the GDPWM method minimizes the SLF function and reduces the switching losses significantly.

As shown in Figure 14 at $M_i = 0.854$ and $100\%T_{eR}$, the algo-

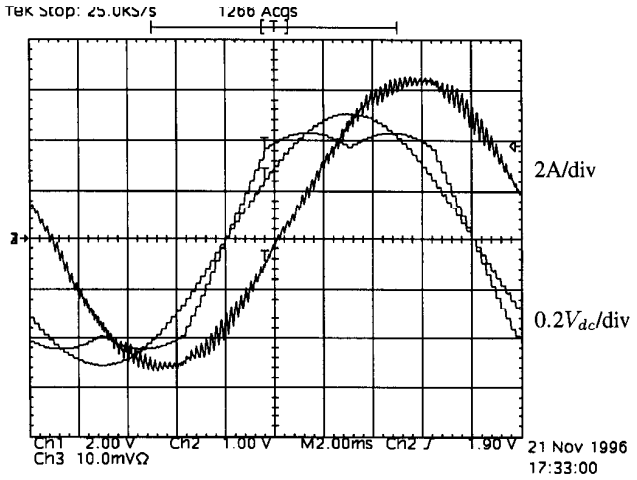

Fig. 11. Experimental SVPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.79$, 49 Hz, $50\%T_{eR}$).

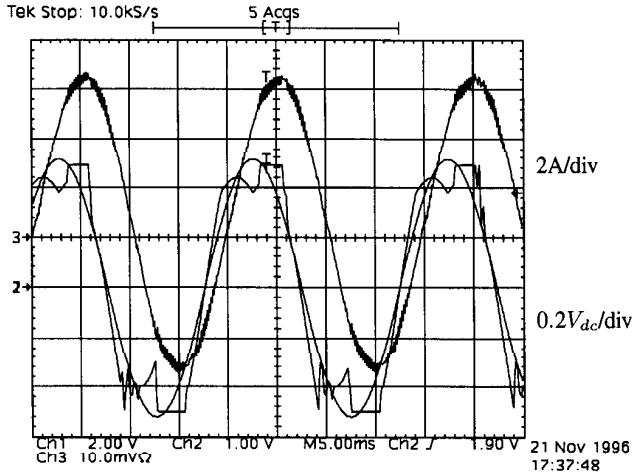

Fig. 12. Transition from SVPWM to GDPWM ($M_i = 0.81$, 50 Hz, $50\%T_{eR}$).

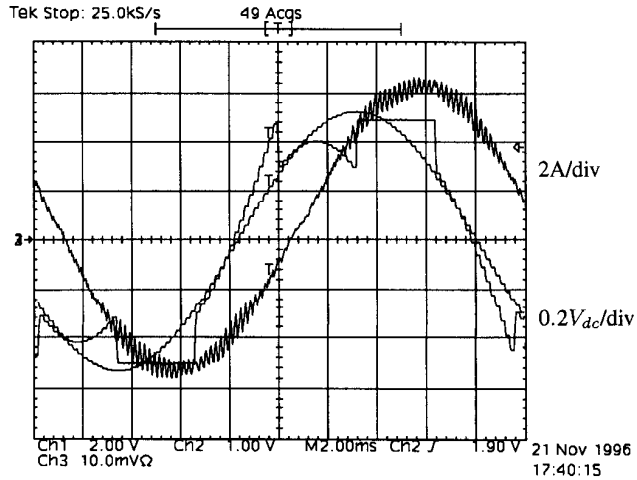

Fig. 13. Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.82$, 51 Hz, $50\%T_{eR}$).

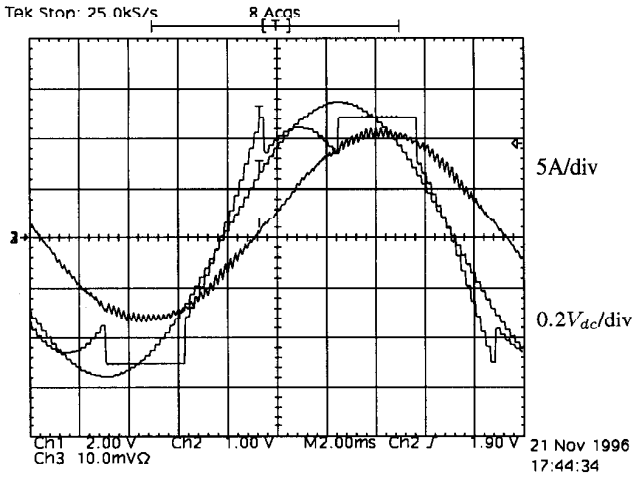

Fig. 14. Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.854$, 53 Hz, $100\%T_{eR}$).

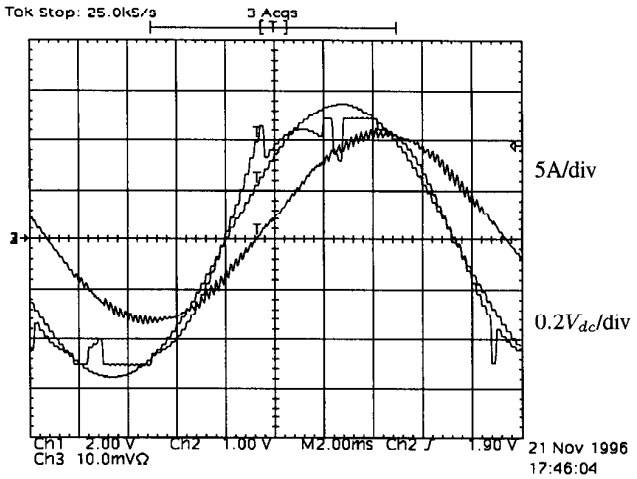

Fig. 15. Transition of GDPWM from $\psi = \varphi$ to $\psi = 0$ ($M_i = 0.86$, 54 Hz, $100\%T_{eR}$).

rithm on-line optimizes ψ to minimize the switching losses. Since the power factor angle for this operating condition is less than 30°, the transistor which conducts the largest current is held on and this reduces the switching losses by approximately 50% when compared to SVPWM. Above M_{itr2} the algorithm on-line selects $\psi = 0$ to maximize the gain, and the inverse gain compensated modulator operates in the overmodulation range. Figure 15 and Figure 16 show the modulator and motor phase current waveforms during and after transition ($M_i = 0.86, 0.903$). As the figures indicate the zero sequence signal oscillation (sudden variation of ψ) does not distort the current, and motion quality is not affected. As the HDF curves suggest, the phase current ripple decreases as the modulation index increases. In the overmodulation range the switching losses are reduced by approximately 30% when compared to SVPWM. As the modulation index is further increased large amount of non-triplen odd subcarrier frequency voltage/current harmonics are generated and the waveform quality degrades due to inverter saturation. However, as Figure 17, and Figure 18 indicate, the modulated segments of the waveform still retain the low distortion characteristic of GDPWM method.

Figure 19 and Figure 20 illustrate and compare the effect of PEM control algorithm on the SVPWM and GDPWM method performance. As the experimental waveforms indicate, eliminating voltage pulses narrower than 12 μs, the SVPWM method looses linearity at a lower modulation index than GDPWM method and the phase current waveform distorts significantly. As all the experimental waveforms indicate, the SVPWM method in the lower modulation index range combined with the GDPWM method in the remainder of the range creates a superior approach.

VIII. Conclusions

A generalized discontinuous PWM method with on-line performance optimization capability has been developed and its characteristics have been analytically and experimentally studied. An algorithm that combines the superior high modulation range performance characteristics of this modulator and the superior low modulation range performance characteristics of SVPWM method has been developed and implemented. The algorithm has a simple structure and it is suitable for DSP or microprocessor based digital implementation. The phase angle ψ of the modulator can be on-line controlled in order to optimize

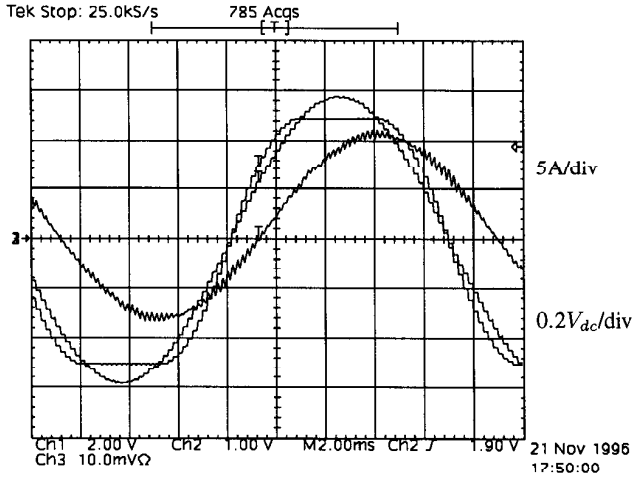

Fig. 16. Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms ($M_i = 0.903$, 56 Hz, $100\%T_{eR}$).

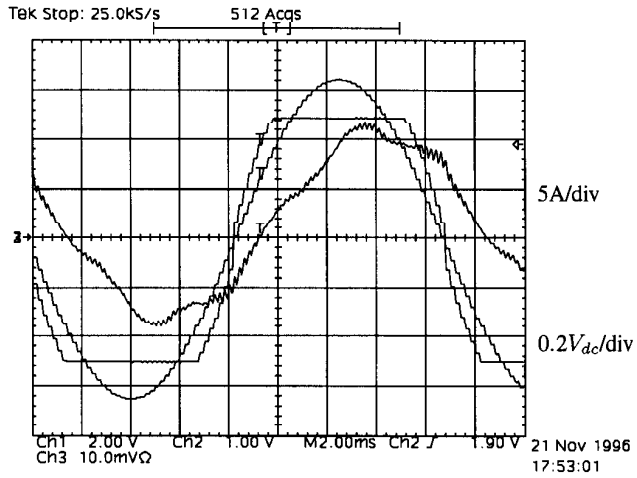

Fig. 17. Experimental GDPWM modulation wave, its fundamental component and the motor current waveforms in the overmodulation range ($M_i = 0.96$, 59 Hz, $100\%T_{eR}$).

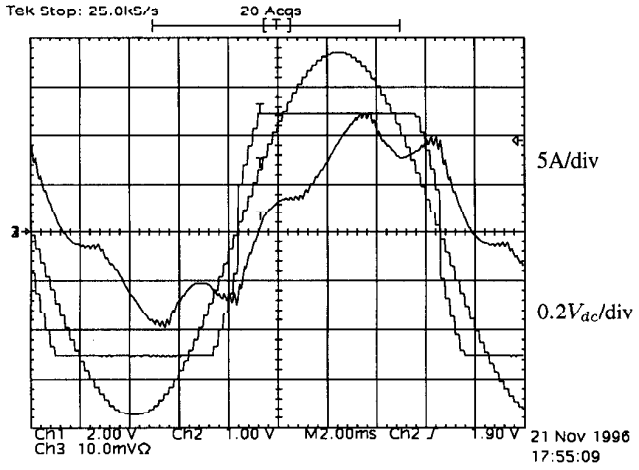

Fig. 18. GDPWM modulation wave and motor current waveforms in the overmodulation range (M_i — 0.986, 60 Hz, 100%T_{eR}).

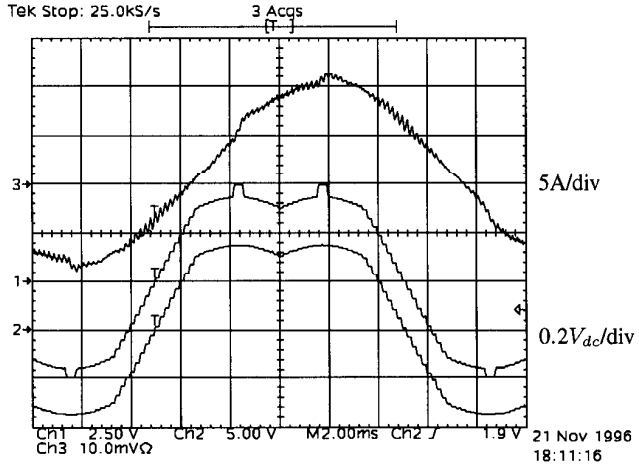

Fig. 19. Experimental SVPWM modulation wave, PEM controlled modulation wave and the motor current waveforms for M_i = 0.815, 49 Hz under a 12μ s minimum pulse width control condition.

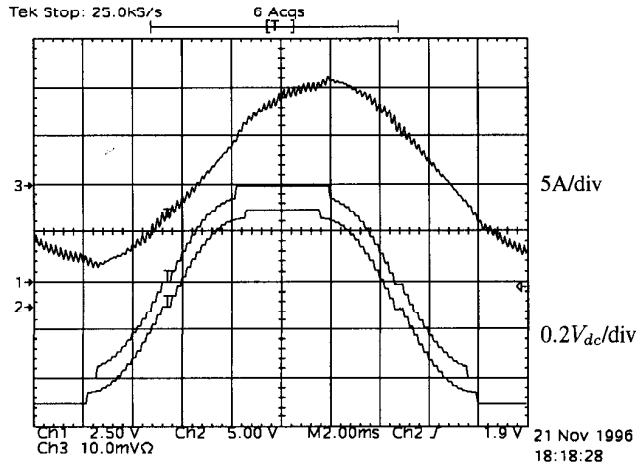

Fig. 20. Experimental GDPWM modulation wave, PEM controlled modulation wave and the motor current waveforms for M_i — 0.867, 53 Hz under a 12 μ s minimum pulse width control condition.

the drive performance and reduce the switching losses. The operating characteristics of the GDPWM method have been verified in the laboratory tests. The losses, harmonic distortion and other characteristics have been both experimentally and theoretically investigated and reported. The transition modulation index value from SVPWM to GDPWM was investigated and an approach to estimate this value has been proposed.

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