Research Report

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A PEBB Based Inverter-System Integration

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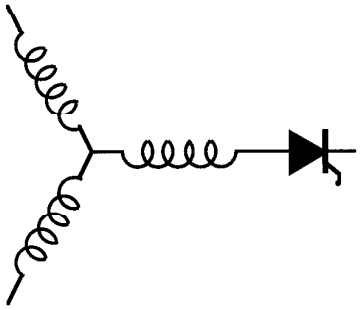

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A PEBB Based Inverter - System Integration

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Abstract

The Power Electronic Building Block concept is devised to facilitate greater modularity in power electronic systems. Device level PEBBs are integrated to form application level PEBBs based on the commonly used voltage source inverter topology. APEBBs form the building blocks for more complex and larger systems such as a DC power distribution network. In this work, performance requirements of an APEBB for successful system integration are developed. A simulation analysis of the stability and dynamic response of a DC distribution network based on APEBBs is presented. Finally, EMI issues pertaining to and possible solutions for APEBBs are discussed.

Introduction

The Power Electronic Building Block refers to widely accepted standardized *'minimal group of power semiconductor switch configurations'* [1] which would satisfy most low to medium power application requirements. A PEBB can be also defined as a complete converter module which satisfies the requirements of a large variety of power converters at low to medium power ranges. Such a converter module is then termed as an Application Level PEBB or APEBB. The advantage of an APEBB is that the principles of operation of commonly used converters such as the three phase voltage source inverters are well understood and successfully applied. Use of APEBBs is expected to lead to a great deal of simplification in the design of large and complex systems.

In this work, a particular application of power electronics - multiple inverters, some with motor loads, working off a common DC bus are considered for development of the APEBB concept. A simulation study is carried out of a Zonal Electrical Distribution System (ZEDS) using behavioral model of APEBBs in order to illustrate the system wide stability and performance issues that need to be addressed.

Electromagnetic interference is emerging as a problem especially with the advent of faster devices. EMI within a PEBB has to be controlled if APEBBs are to find widespread application. Solutions to the EMI problem range from reducing EMI generation within a PEBB by better device level design, to reduction of generated EMI by appropriate control strategies. Soft switched topologies can also offer significant benefits in terms of EMI reduction.

APEBB Configuration

An APEBB is envisaged as a multi-tiered system with a hierarchical control structure. The APEBB constitutes of device level PEBBs and relevant control and sensor circuits. Therefore, power semiconductor technology as well as gate drive and control circuitry need to be concurrently developed and successfully integrated. For example, it is expected that devices will be required to switch faster and at higher temperatures. For instance, if Silicon Carbide (SiC) switches with typical switching times of 20ns as opposed to 200ns for currently available IGBTs are used, switching speeds of 200 kHz are possible as compared to 20 kHz with conventional IGBTs (hard switching). This in turn requires faster and improved gate drives. Again, higher switching speeds require faster control loops and hence faster signal processing techniques. Finally, improved isolation techniques and better thermal management techniques are required to permit operation at higher temperatures. EMI spectrum issues at the projected higher switching frequencies need to be addressed.

Hard switched topologies form the basis for most power converters in the drives applications area although soft switching topologies such as the resonant DC link inverter (RDCL) or resonant AC link converters also find application. Fig. 1 shows the a proposed structure of the device level PEBB based three phase voltage source inverter.

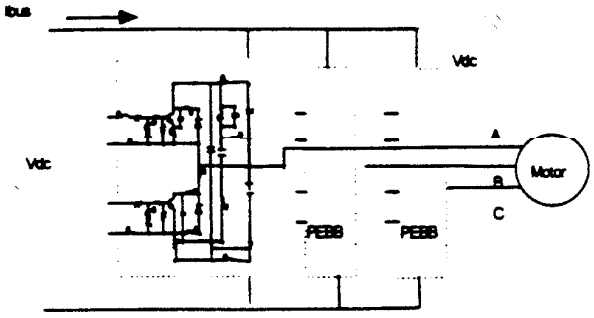

Fig. 1 PEBB based three phase voltage source inverter.

A functional block diagram of a motor drive APEBB can be devised as shown in Fig. 2. Within the APEBB, there are several sub-PEBBs which are described briefly.

1. Device level PEBBs with integrated gate drives are connected at a standard power interface.
2. Sensor blocks (within switch PEBBs) provide the required feedback and some of the control signals.
3. Low level gating logic (also standardized) works off the sensors and standardized auxiliary power supplies.
4. Programmable application controller controlled by the system controller or local independent operation. This controller can be programmed to work as a field oriented or a volts/hertz controller or implement any scheme compatible with the power circuit topology.
5. The input/output filter PEBBs. These are be purely passive LC networks. For isolated industrial applications, input

filtering is sufficient only to prevent instabilities due to common power line disturbances. In multiple converter environment, additional filtering PEBBs may be required.

6. Heat exchange/cooling. This block refers to heat sink design and/or external cooling required for a specific APEBB which depends on the power level and packaging.

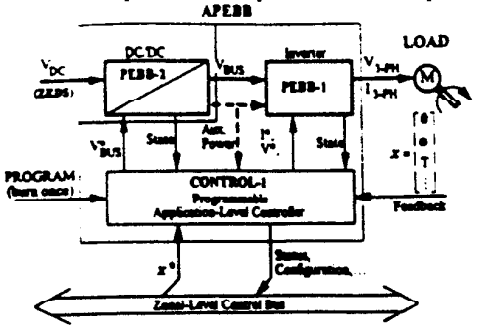

Fig. 2 Functional schematic of an APEBB.

Fig. 3 shows the PEBB-1 block of Fig. 2. Note that the applications controller can be programmed to identify the type of topology within the APEBB during commissioning and the control does not have to be customized for each topology. The block labeled as PEBB-2 can be made to provide galvanic isolation between the load and the DC distribution system. As a DC-DC converter, it may be may be configured to provide local energy storage for greater dP/dt (power slewing) capability for critical loads or to permit four quadrant operation of the APEBB or to improve input characteristics.

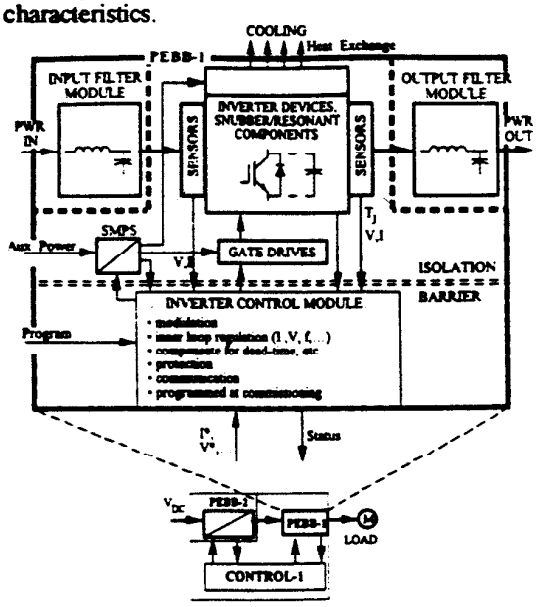

Fig. 3 Internal structure of an APEBB.

APEBB Based System Integration.

An APEBB forms the basic block from which more complex systems can be synthesized. The actual structure of an APEBB itself depends on the system configuration. For example, if several motor drive APEBBs are connected to the same DC bus, stability of the entire network requires that the input filter of each APEBB assume uniform characteristics. The goal of system integration is to make the APEBB a true building block so that the system designer can interconnect several APEBBs without a need for system stability or interaction studies. This can be achieved by standardizing specifications for input filtering and dynamic impedance of each APEBB, thereby minimizing system design effort. The primary concerns in system integration are stability, dynamic response/ power slewing capability and harmonic currents.

A maximally flexible and scalable architecture would permit the addition of APEBBs at any system node within the power flow capability of the network. This translates to a requirement that each APEBB have uniform terminal characteristics independent of the network configuration. The system controller evaluates the stability of the entire network based on the terminal characteristics of the APEBBs only using software algorithms. Under non-autonomous control, the system controller downloads this information to every other APEBB on the network over the communications channels. In the autonomous control case, the operation of each APEBB is determined by local conditions - thus an APEBB controller has to distinguish between the two modes of control. The control scheme for such operating conditions can closely parallel those that have been proposed and verified for autonomous UPS operation in an AC network [4].

The Zonal Electrical Distribution System (ZEDS) is an excellent benchmark in illustrating system integration issues. Fig. 4 shows the schematic of the typical ZEDS. There are three APEBBs (without input filters) with ratings of 10 kVA, 100 kVA and 250 kW connected to a single unregulated 750VDC bus. The values of the distributed parasitic line inductance and resistance can only be estimated prior to commissioning. For the simulation study, the value of the corner frequency of each APEBB branch (z_1, z_2 and z_3) was selected to be 5kHz, 500Hz and 150Hz respectively. The node voltage V_o developed across the parasitic capacitance C_p is common to each APEBB subsystems and needs to stable irrespective of all APEBB operations. Also, this node is fictitious and unavailable for shunt compensation.

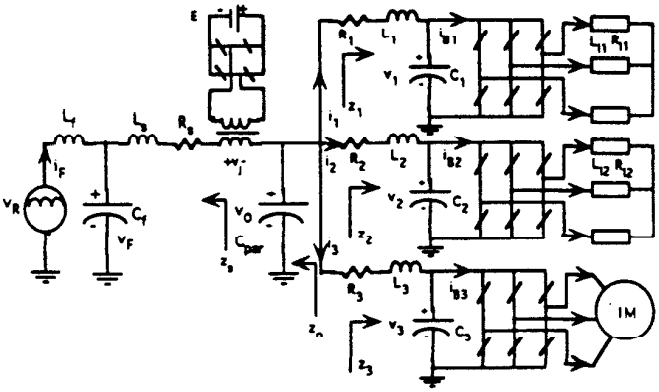

Fig. 4 ZED System with series active damping.

To derive stability conditions for the entire ZEDS consider fig. 5 which shows two cascaded subsystems with stable

transfer functions F_a, F_b and output and input impedances of z_o and z_{in} respectively. Stability of the overall system is guaranteed if the following condition is satisfied[2,3].

$$1+\frac{z_o(s)}{z_{in}(s)}\neq 0 \qquad (1)$$

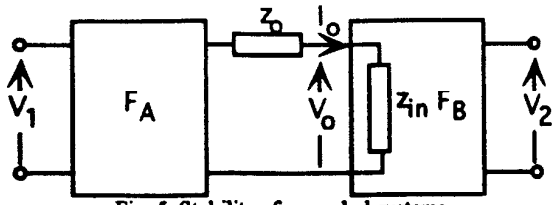

Fig. 5 Stability of cascaded systems.

Alternately, the graphs of $z_o(\omega)$ and $z_{in}(\omega)$ should be non intersecting at all frequencies. This principle can be extended to the entire ZEDS under consideration. The ZEDS will be stable if the following condition holds:

$$1+\frac{z_o(s)}{z_{123}(s)}\neq 0 \qquad (2)$$

$$\text{where } z_{123}(s)=\frac{z_1z_2z_3}{z_1z_2+z_2z_3+z_3z_1} \qquad (3)$$

The input impedance of each APEBB branch is given as:

$$z_j(s)=(R_j+sL_j)+\frac{(1/sC_j)Z_{inv,j}(s)}{1/sC_j+Z_{inv,j}(s)} \quad j=1,2,3 \qquad (4)$$

where $Z_{inv,j}(s)$ is the inverter input impedance. There are several models for the inverter input impedance but for stability purposes, it suffices to model the inverter as a harmonic current source. Hence, $|Z_{inv,j}(s)|>>1$ and thus,

$$z_j(s)=(R_j+sL_j)+\frac{1}{sC_j};\ j=1,2,3 \qquad (5)$$

For the simulation case under study, the largest inverter was switched at 200 Hz whereas the 100 kVA inverter was switched at 2 kHz and the 10 kVA inverter at 20 kHz. The nominal system voltage waveforms are shown in fig. 6. Also, for the simulation study, each APEBB was operated under an open loop PWM scheme without an overall system controller. The ripple voltage at V_o is extremely large (>150V, 20%). Inverter modulation produces harmonic currents which are injected into the system producing a ripple at V_o. The gain between the inverter DC currents and V_o is given as:

$$z_{h,j}(s)=\frac{V_o(s)}{I_{h,j}(s)}=\frac{z_{123}(s)}{1+sC_jR_j+s^2L_jC_j} \quad j=1,2,3 \qquad (6)$$

Thus, the series inductance filters out the high frequency components at V_o. Conversely, the line reactance also limits the *di/dt* and consequently the power slew rate since at constant voltage, power transfer rate *(dP/dt)* is determined by *di/dt*. Hence, conditions which require a large power transfer such as starting of the motor load on the largest APEBB will produce a voltage sag at V_3 since power cannot flow from the rectifier end towards the load instantaneously. An energy storage element in the APEBB with large power rating is another solution to reducing large voltage sags. This can be

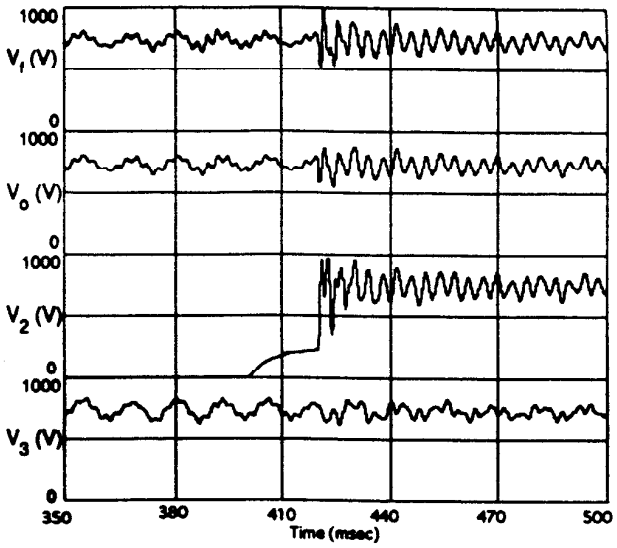

Fig. 6 ZED System voltages (uncompensated case).

accomplished by using the PEBB-2 block in fig. 2 as a DC-DC converter.

The ripple content of V_o is determined by the magnitude of $I_{h,j}$ and $|z_{h,j}|$. The largest APEBB will inject the maximum harmonic currents, largely at low frequencies due to the low switching frequency (to minimize losses) of the APEBB. Since z_{123} in (3) is the parallel combination of the APEBB branch impedances, its values is dominated by the smallest of the line impedances. This suggests that APEBB with lowest branch impedance will sink the maximum harmonic currents and so the rating of that APEBB branch will increase irrespective of the load rating at that APEBB This is clearly an undesirable feature of an APEBB based system.

Active damping of dominant harmonics is an attractive solution for a ZEDS because individual APEBB controls do not then have to be constrained to minimize input DC current harmonics. If the harmonic interactions are minimized, the APEBB ratings will also be reduced. For this purpose, a series voltage injection scheme is proposed (represented as dependent voltage source v_j in fig. 4). An APEBB implementation of a single phase VSI is made to inject a voltage V_j into the DC grid. It can be shown that if this voltage V_j is made to satisfy the condition: $V_j=V_f-V_o^*-L_s\frac{di_s}{dt}-R_si_s$ where V_o^* is the reference voltage, then $V_o=V_o^*$. The reference for a PWM scheme is generated from local feedback signals V_f, I_s and parameters L_s, R_s. Differentiation of i_s improves response to rapid changes in load power but can be neglected if L_s, R_s are small. Since V_o is regulated, source impedance z_o in fig. 3 is reduced dramatically. Harmonic currents no longer are able to flow from one APEBB branch to another. Also, by reducing z_o, the power transfer capability is increased. However, filter capacitor voltage ripple frequency increases (fig. 7). An advantage of this solution is that the compensator rating is only about 10% of the load rating.

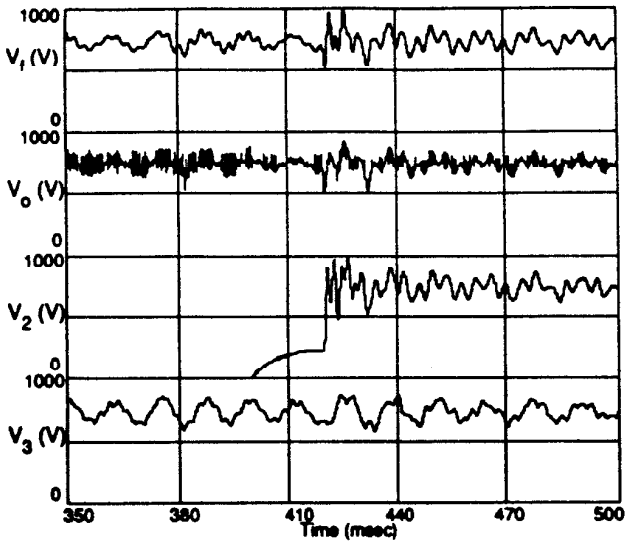

Fig. 7 ZED System voltages (series compensated).

EMI Issues with PEBB System

With the proliferation of power electronic systems, radio frequency EMI generated by power converters has become a serious concern. The chief cause for increased EMI is higher device switching speed. Soft switching topologies have been shown to reduce EMI. Audio frequency EMI are produced by modulation strategies and when conducted through parasitic paths can cause damage to motor windings and machine bearings[6]. The EMI problem is exacerbated by the recent trend towards higher efficiency machines with lower leakage inductances. It is possible to reduce the common mode voltage (a major source of EMI) produced by any inverter modulation scheme in a hard switched topology by a new scheme proposed in [7] which involves a modification of the three phase VSI topology (fig. 9). Fig. 10 shows the neutral voltage spectrum obtained from a modified converter using such a scheme. At the design stage of a PEBB, detailed device and integrated gate drive modules models can be used to predict and prevent EMI generation. One coupling path for conducted EMI is the capacitive path formed by the heat sinks between the devices and chassis. With integrated gate drives and sensors EMI problems are likely to worsen in a PEBB. Opto-coupling of all interface signals is a likely solution for some of the EMI concerns.

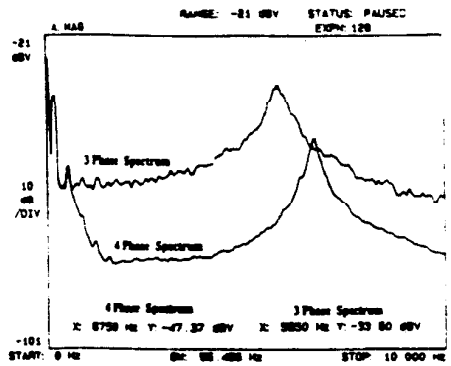

Fig. 10 Spectrum of neutral voltage V_n with proposed scheme.

Conclusions

APEBBs can be integrated into larger complex systems with due consideration to increased filtering requirements. The stability of resulting systems can be analyzed with existent methods. Since standardized input characteristics of APEBBs cannot assure satisfactory system performance, APEBB based active filtering solutions may prove to be the optimal solution. EMI within device PEBBs has to be reduced by design. Soft switching topologies and control strategies involving topological modifications can be incorporated into APEBB structure to minimize EMI.

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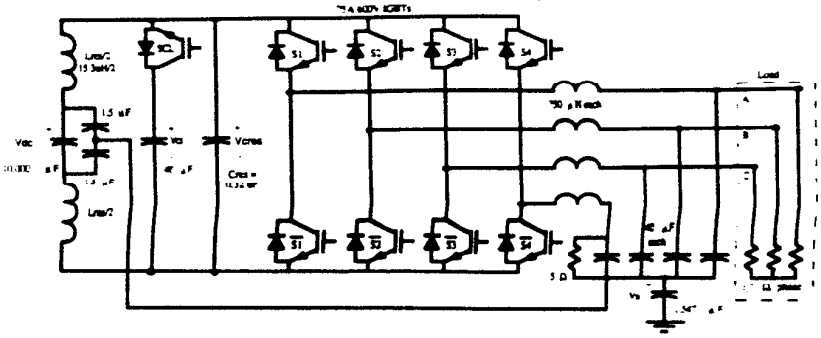

Fig. 9 Four leg inverter with three phase load.