Research Report

97-15

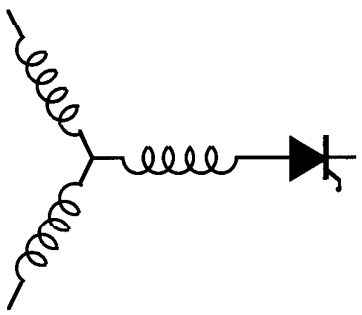
Pulsed Dc-Link Current Converters - A Review

***E.R. daSilva, **Y. Murai, T.A. Lipo, *L.P. deOliveira, *C.B. Jacobina**

Wisconsin Power Electronics
Research Center
University of Wisconsin-Madison
Madison WI 53706-1691

*Federal University of Paraiba
C.P. 10.105
Campina Grande, PB
58.109-970 Brazil

**Gifu University
1-1 Yanagido, Gifu
Gifu 501-11
Japan



Wisconsin
Electric
Machines &
Power
Electronics
Consortium

University of Wisconsin-Madison
College of Engineering
Wisconsin Power Electronics Research Center
2559D Engineering Hall
1415 Engineering Drive
Madison WI 53706-1691

IEEE Industry Applications Society
Annual Meeting
New Orleans, Louisiana, October 5-9, 1997

Pulsed DC-Link Current Converters - a Review

E.R. da Silva*, *Senior Member*, Y. Murai**, *Senior Member*, T.A. Lipo***, *Fellow*, L.P. de Oliveira*, and C.B. Jacobina*, *Member*
* Dept. of Electr. Engineering, Federal University of Paraiba
C.P. 10.105, Campina Grande, PB., 58.109-970 Brasil
Tel.: +55 (83) 310-1407, Fax: +55 (83) 310-1418, e-mail: edison@dee.ufpb.br
**Dept. of Electr. and Computer Engineering,
Gifu University, 1-1 Yanagido, Gifu
Gifu 501-11, Japan
Tel.: + 81-58-293-2703, Fax: + 81-58-230-1894
*** Dept. of Electr. and Computer Engineering,
University of Wisconsin-Madison
1415 Johnson Dr., Madison, WI 53706, USA
Tel: + 1 (608) 262-0287, Fax: +1 (608) 262-1267, e-mail:lipo@engr.wisc.edu

***Abstract** - This paper presents a systematic review and generic classification of the Pulsed DC-Link Current (PDCLC) converters having a pulsed dc-link current waveform. The operating principles, performance evaluation, and a comparison of the principal features of the existing and new proposed topologies are discussed. An extensive bibliography is presented in the paper.*

1. INTRODUCTION

The development of self-commutated switches, as the GTO and IGBT, during the past decade has allowed a better use of pulsewidth modulation (PWM) in current source rectifiers, inverters and AC-to-AC power converters. These converters have a constant current in the dc-link as a common property. They have regenerative capabilities and inherent short circuit protection, and buffering of the converter output from supply voltage variations. Besides these features, the voltage-regulated current source inverter exhibits the same high performance features as the corresponding voltage source inverter topology, with similar waveform quality as well as dynamic performance [1]. The switches in the PWM converters, however, must be turned on and off frequently while conducting current, thus increasing the switching losses. These losses can be reduced by snubbers, but considerable energy is still dissipated through these circuits during the turn on of the switch. Instead, a variety of techniques have been proposed to reduce the amount of losses in current source converters. Some of these techniques use many extra components [2]. However, the pulsed dc-link current (PDCLC) converter uses a relatively small number of extra components. In these converters the current in the dc-link is pulsed in either resonant or resonant transition modes so that soft-switching can be achieved. Figure 1 presents generalized structures for PDCLC converters in which the current is shaped by an Auxiliary Wave-Shaping Circuit (AWSC) placed at positions A and B of the structures, generating different configurations. Their switches commutate under either zero-current-switching (ZCS) or zero-voltage-switching (ZVS). A brief discussion of PDCLC converters is presented in [3] but, except for [4] which compares only some features of four topologies, the authors are not aware of either classification or comparative studies of these possibilities.

This paper presents a systematic review and generic classification of Pulsed DC-Link Current (PDCLC) converters for the pulsed dc-link current waveform, i_s, in Fig. 1. The operating principles, performance evaluation, and a comparison of the existing and new proposed topologies are presented.

II. TOPOLOGIES FOR PDCLC CONVERTERS

The existing PDCLC converters can be grouped in terms of their pulsed current waveform i_s (Fig. 2) and referred to by their AWSCs. In these AWSCs the switches will be represented by both SCRs and GTOs. The GTO representation will distinguish the cases in which the switch is required to be of the self-commutated type. They will be now on referred to as auxiliary switches, while those in the power converters will be referred to as main switches.

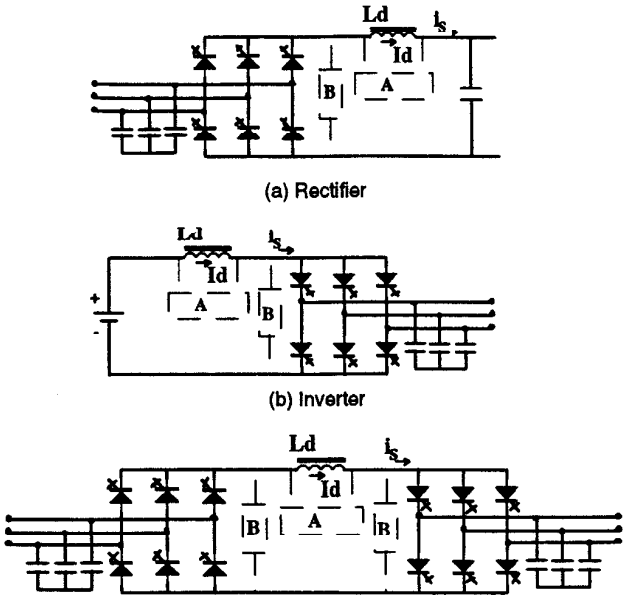


Fig. 1. Converter configurations with dc-link pulsed current

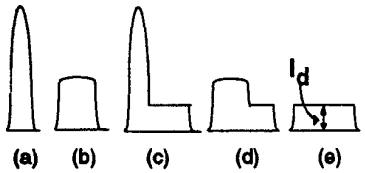


Fig. 2. Types of pulsed waveforms

A. AWSC of type A (Fig. 3)

A.1. Resonant Pulse (Fig. 2a): The AWSC for the series resonant dc-link current (SRDCLC) converter [5,6] corresponds to the circuit I in Fig. 3 (a). In this converter the resonant tank elements C_r and L_r are introduced such that the switch turn-on and turn-off transitions in the power circuit naturally occur at the zero current crossing. With switching losses substantially reduced, this converter has a high dynamic performance resulting from high frequency switching. The zero current interval width in the train of pulses produced is nearly constant and the pulse width is fixed. However, it suffers from high RMS current values relative to the dc-bias current I_d. Its operating stability depends upon the capacitor voltage at the moment in which main switches are triggered as well as on the dc-bias current level I_d indicated in Fig. 1(a). Therefore this level has to be controlled.

A.2. Resonant Clamped Pulse (Fig. 2b): Consider configuration in Fig. 1(a). In the SRDCLC, when the switches in the inverter commutate from low voltage phase to higher voltage phase because of different phase demand, unexpected extraordinarily high-peak pulses may occur. Therefore, clamping is a crucial issue because even regular resonant peaks can reach six to seven times the load current. The AWSCs II and III were proposed to limit both regular and irregular current peaks in the SRDCLC converter. The AWSC II generated the Actively Clamped Series Resonant DC-Link converter, ACSRDCL, in which the clamping level is established by extra inductor L_a [7]. The AWSC III generated the Series Resonant DC-Link with a Saturable Core converter, SRDCLSC, in which the clamping level is imposed by design of the saturable core SR [8]. One feature of the SRDCLSC is that the clamping level is automatically adjusted by the load currentIn these converters, a maximum pulse width can be imposed and a pulse split used to keep switching frequency from decreasing, if necessary [9].

A.3. PWM Resonant Pulse (Fig. 2c): The PWM-SRDCLC converter (represented by the AWSC IV in Fig. 3c) [10] allows for synchronization with external PWM signals and retains the advantages of the SRDCLC converter. The auxiliary thyristor and diode allow the PWM operation. Its main drawbacks continue to be high voltage and current stresses over its main devices.

A.4. PWM Clamped Resonant Pulse (Fig. 2d): Although ACSRDCL and SRDCLSC convertors limit the current peak they can not adjust the pulse width and synchronize with external PWM signals. The PWM-ACSRDCL (AWSC V) [11] and the PWM-SRDCLSC (AWSC VI) [12] converters overcome this drawback.

A.5. Quasi-Square-Wave with Resonant Transition (Fig. 2e). The flat-topped quasi-square current pulse with resonant transition greatly reduces the output RMS value and results in nearly the same output performance as can be achieved by the conventional current source GTO converters. Two sub-groups can be considered:

1) Constant Zero Current Interval (CZCI). In these topologies (Fig. 3e), the switching period varies with the pulse-width adjustment as the notch has a nearly fixed width. The converters that use AWSCs VII [13] and VIII [14] differ only by the location of the resonant inductor and their operation is quite similar. However, they allow different modifications in their structures [14,15]. In AWSCs IX [16] all currents are clamped at 1 p.u. relatively to I_d current but it uses three switches while Circuit X [17] uses only a set of auxiliary diode-switches. Also in XI [18] currents in the main switches

of the circuit are clamped at 1 p.u. relative to the dc-link current I_d with just one extra switch. The difference is that all other converters mentioned operate under ZCS, but the AWSC XI imposes the restriction that the main switches be of the self-controlled type so that their soft-switching instant occurs at zero-voltage. Other topologies, in which the notching width is reduced and made almost independent of the bias current I_d, are presented in [14]. Again, additional components are needed as it is the case for the circuit represented by AWSC XII.

2) Variable Zero Current Interval (VZCI), Fig. 3(f). Notches with their width controlled and fixed switching frequency operation can be achieved by addition of extra switches to the CZCI versions. In contrast to AWSCs XIII [15], XVI [19], XVII [20] and XVIIi [20], the capacitor polarity in AWSCs XIV [14] and XV [21] is always adequate to divert the current from the DC link. However, AWSC XIV uses four switches that operate in the thyristor mode while in AWSC XVI two auxiliary switches are replaced by diodes and the remaining switches must be of the self-controlled type. The new topologies indicated as XVII and XVIII [20] use less switches than the other do. Nevertheless, it should also be kept on mind that a larger ripple in the bias current i_d is expected in AWSC XVIII because one of the auxiliary thyristors connects the bias inductance to ground when fired. On the other hand, AWSC XVII requires that both the auxiliary switch in anti-parallel with the bias inductance and the switches of the front-end rectifier in Fig. 1(c) be of the self-controlled type. In this case the soft-switching occurs under zero-voltage. However, operation in the thyristor mode for the switches of the inverter allows less voltage stress over the resonant capacitor, as shown in the simulated results presented in Fig. 4. Reference [14] introduces other topologies of which the maximum frequency of operation is less dependent on the bias inductance current level than those presented here.

Figures 5 to 8 present experimental results for AWSCs I, III, VI and VII.

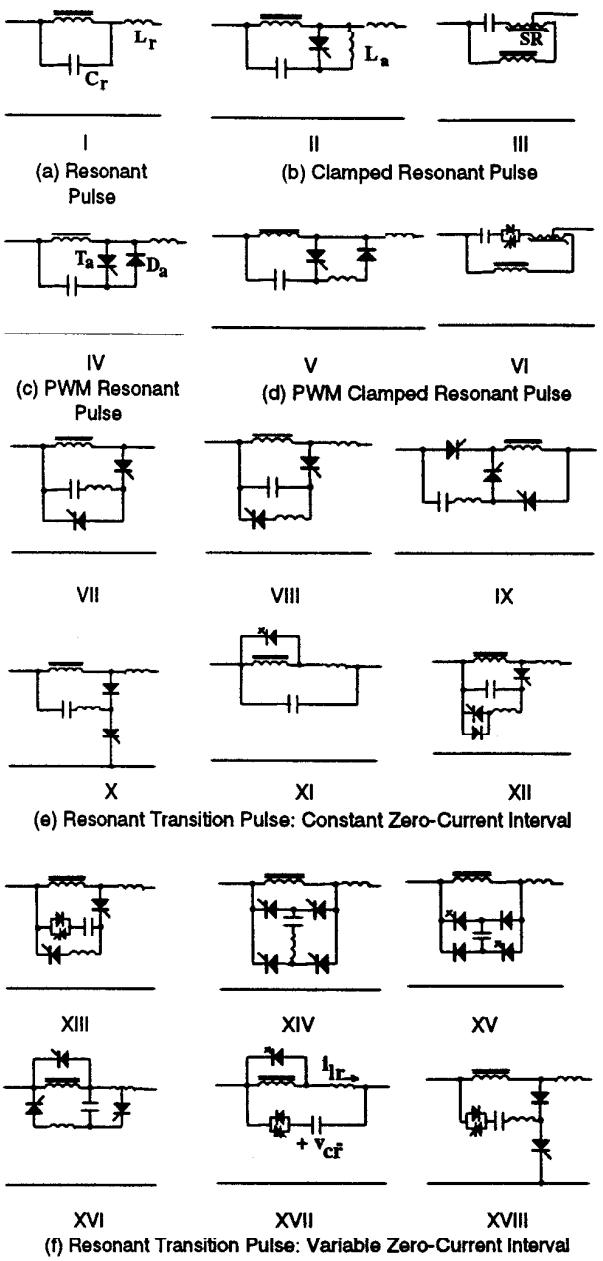
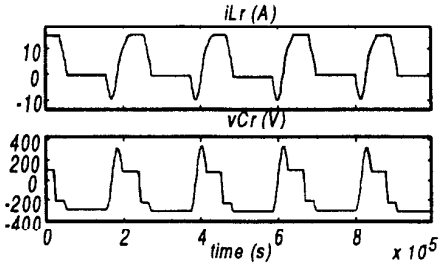


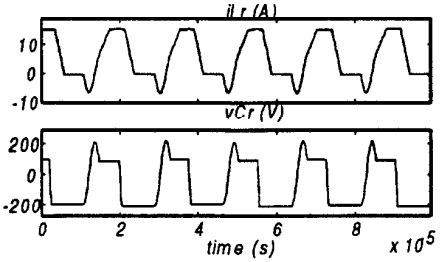
Fig. 3. Auxiliary Waveshaping Circuits (AWC) for Position A

B. AWSC type B (Fig. 9)

AWSCs XVIX to XXI represent the auxiliary circuits of type B that applies to the AC-AC converter in Fig. 1(c). With AWSC XVIV and XIX [22] the switches of the input and output converters commutate under ZCS and with AWSC XX input and output current can be controlled independently. In case of AWSC XXI the converter switches must be of the self-controlled type, their soft-switching occurring at zero-voltage [23]. On the other hand, most of concepts used at position A can be applied to position B in case of both rectifier and inverter circuits, as exemplified by AWSC XXII for an inverter topology [24]. One point is that the rectifier-inverter structure allows more control flexibility than an isolated inverter for the same bias current control. It is important to note that new principles have arisen with the use of AWSCs of type B. This is the case of the neutral commutated current source rectifier [25] and of the rectifier in [26], in which the switches commutate under zero-voltage-switching (ZVS) mode. Circuit XXIII [27] was applied to an inverter bridge



(a) Inverter operating under ZVS



(b) Inverter operating under ZCS

Fig. 4. Principal waveforms for AWSC XVII

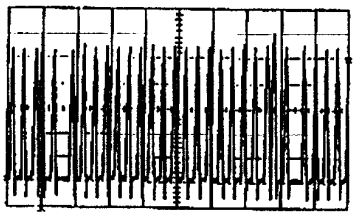


Fig. 5 Pulsed current for AWSC I
I_d = 5A, 5 A/div, 0,2 μ s/div

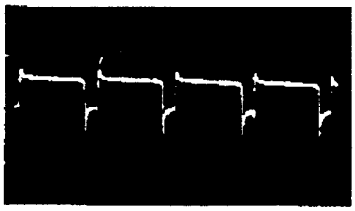


Fig. 6. Pulsed current for AWSC III with clamping factor of 1.2,
I_d =5A, 50 μ s/div

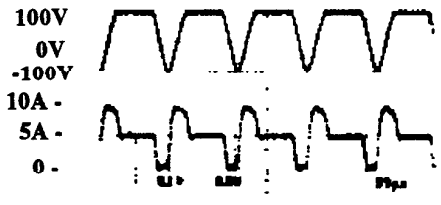


Fig. 7.AWSC VI with clamping factor of 2, I_d = 5A, 10 kHz
Top: resonant capacitor voltage. Bottom: Pulsed current

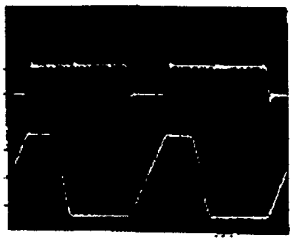


Fig. 8. Waveforms for AWSC VII. Top: pulsed current (A), I_d = 5 A.
Bottom: resonant capacitor voltage (V). Hor.: 20 m s/div

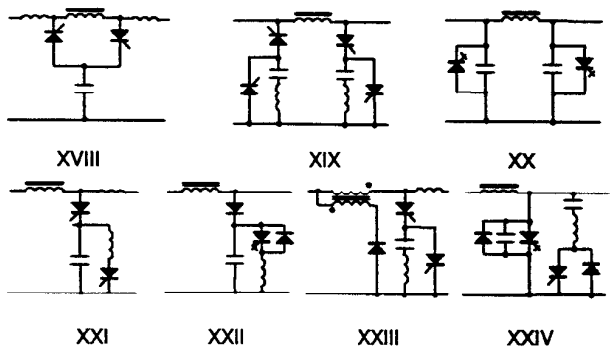


Fig. 9. Auxiliary Wave-Shaping Circuits (AWSC) for position B

operating under zero-voltage-switching (ZVS) mode. In AWSC XXIV [28], the transformer not only clamps the capacitor voltage and sends the trapped energy back to the source but also allows the converter to operate with fixed pulse frequency, reducing the size of the dc link inductance and output capacitors. Finally, the AWSC XXVI represents a case in which one auxiliary switch commutates under ZVS while the other commutates under ZCS. This possibility was adapted from [29].

III. CONTROL AND MODULATION STRATEGIES

A number of different control strategies have been employed to control PDCLC converters. Its choice depends not only on the system requirements but also on the topology of the AWSC used. A typical scheme that uses the AWSC VIII to control an induction motor with input and output sinusoidal currents is shown in Fig. 10. The inverter has the role of controlling frequency and the phase angle corresponding to the motor speed, while the rectifier has the role of controlling both DC biasing current I_d and maintaining unity power factor at the input at same time. Also, the rectifier and inverter require PWM control to produce input and output sinusoidal voltage and current. Figure 11 presents typical output waveforms for a scheme with the AWSC VII.

A simple tracking control can be used to regulate

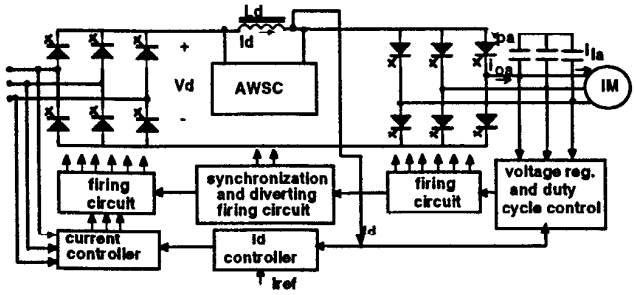


Fig. 10. Control diagram of converter using the AWSC VIII

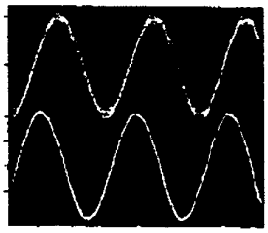


Fig. 11. Output waveforms for a converter AWC VII (Three-phase induction motor). Top: line voltage (V) Bottom: line current (A). Hor.: 10 ms/div

current i_d from the front-end rectifier control [6] but, depending on the AWSC used, other control may be required. When the SRDCLC and PWM-SRDCLC converters are used, a trimming control is needed to limit regular and irregular peaks of current, additional components being used for that purpose [30]. When regular and irregular peaks of current are avoided by clamping current circuits such as ACSRDCL and SRDCLSC, a pulse-split principle [8] may be needed to generate a very smooth sinusoidal waveform because of the possible low switching frequency. Also regulation of the bias current I_d by adequate control of the output voltage of the rectifier avoids voltage stress due to the capacitor energy exchange. For that purpose, a control of the type +E/0/-E can be used for instance [7,31].

The unity power factor in the input is done by selecting the switches to conduct the current pulses to establish the sinusoidal current waveforms with the signal of input phases under the PWM pattern. Converters that produce resonant and resonant clampled pulses use a modulation scheme that is based on the concept of pulse density modulation (delta modulation) because of the lack of pulse-width adjustment. Employing the AWSC CZCI that generates Quasi-Square-Wave current pulses with Resonant Transition is attractive as they nearly synchronize with external PWM. Different good PWM techniques based either on the carrier method [32-34] or space vectors [35,36] have been applied to current source converters. Also space vector modulation has been used together with the line commutation strategy so that only one commutation is assisted by the diverting circuit during one switching interval [27], When an AWSC of type CZCI is used the reduction of the notch width to a minimum is of interest. The phase currents shown in Fig. 12 for this case correspond to the switches as indicated in Fig. 13(b). However, a better result can be achieved when the type VZCI is used and the zero current during the adjusting notch is considered as a zero vector [20]. Figure 13(a) shows the phase currents obtained with this approach. In these figures, τ_1, τ_2 and τ_0 indicate the interval of time for application of active vectors and zero vectors, respectively, while T_R represents the duration of the zero-current interval. A

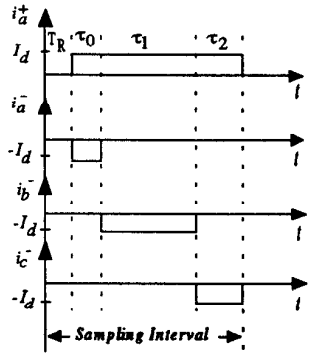
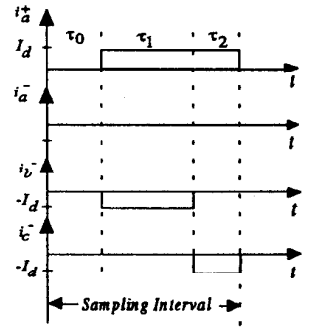
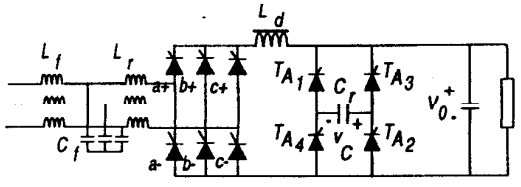


Fig. 12. Technique presented in [27]



(a)



(b)

Fig.13. (a) Technique presented in [20] and (b) rectifier that allows ZCS line commutation

modified rectifier that uses the AWSC XV and operates in this manner is presented in Fig. 13(b). Simulated results for the corresponding phase currents with unity power factor are shown in Fig. 14.

IV. COMPARATIVE STUDIES

The PDCLC converter family has been suggested for super conducting magnetic energy storage (SMES) systems [37], for dc [38] and ac motor drives [15], and for electric vehicle drives [28]. They have also been suggested as active filters and static VAR compensators and HVDC systems [39].

To compare the features of the different PDCLC converters the following aspects should be emphasized: (1) number of components, (2) PWM techniques used, (3) zero-current and/or zero voltage switching, (4) control complexity, (5) capability of constant frequency operation, (6) suitability for high power level, (7) losses. A number of these features have been roughly mentioned in this text, others are readily apparent but some of them require more detailed analysis. Tables I and II summarize the typical features for most of topologies with the AWSC in position A. The maximum rectifier output voltage and the bias current are taken as the base for normalizing the voltages and currents, respectively.

The analysis of converters with the AWSCs considered show that the typical maximum voltage stress over main switches is 2 p.u., or more, except for converters with the circuits X, XI, XVII, and XVIII [20]. AWSC IX causes the largest voltage stress (as much as 6 p.u.) to achieve stable operation [4]. With AWSCs XI and XVII the voltage rating is limited to the supply voltage. The analysis also shows that the auxiliary devices for these AWSCs need to be rated at only 1 p.u., but for most of other AWSCs these devices are submitted to more than a 2 p.u. voltage. However, by restricting some switching states from occurring at the same time, such switch voltages can be limited.

Alternatively, the high current peaks in the main switches obtained with the use of AWSCs I and IV can be clamped by use of AWSCs II, III, V and VI. However, as with all other AWSCs these currents are limited to the link current. However, this is not the case for the auxiliary devices. In most of AWSCs with more than one auxiliary switch, at least one of these switches suffers from a resonant current peak identified in Table I as H (high) or M (moderate). AWSCs IX (three auxiliary switches), XIV (four auxiliary switches) and XV (two auxiliary switches) are the exceptions. For the AWSCs XI and XVII this peak is limited.

IGBTs and GTOs are recommended to be used for the main power circuit and their switching losses can be reduced by ZCS since this reduces the effect of current tailing [21]. However, most of the topologies allow the use of SCRs and can handle higher power. The above discussion shows that in converters that employ AWSCs XI and XVII, the VA ratings of devices are reduced to those of the hard switched converters. This makes these converters suitable for high power but they are limited to IGBT and GTO power range. For higher power the clamped structures seem to be a good choice at the expense of moderate VA ratings.

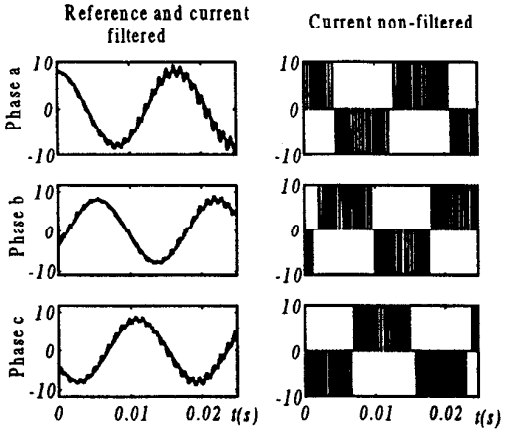


Figure 14. Simulated results for the technique and circuit in Figure 13

Minimum global losses must also be considered as a criterion of choice. However, such a topic requires a more accurate analysis and will not be treated in this paper. Finally, the control complexity depends not only upon the topology used but also on the system requirement, as discussed in the previous section.

CONCLUSION

In this paper a systematic review and generic classification of pulsed DC-link current converters for AC-DC, DC-AC and AC-AC power conversion have been presented. These topologies operate under ZCS and ZVS soft-switching. Many modified topologies have been proposed to overcome drawbacks such as large voltage and current peaks, no capability of constant frequency operation, etc., making them attractive for utilization in different application areas. Also, many control strategies and PWM strategies have been developed to improve the performance of these systems.

REFERENCES

[1] G. Joos and J. Espinoza, "A high performance

TABLE I
COMPARISON OF FEATURES OBTAINED WITH AWSCs IN POSITION A

	I*	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII	XIII	XIV	XV	XVII	XVIII
A**	-	1S 1D	-	1S 1D	1S 1D	1S 1D	2S	2S	3S	1S 1D	1S	2S 1D	3S 1D	4S	2S 2D	2S 1D	2S 2D
B (p.u.)	2	2	2	2	2	2	>3	>3	>4	<2	1	>3	>3	>3	>3	1	<2
C (p.u.)	-	2	-	2.5	>2	2	3	3	>3	3	1	3	3	3	3	1	3
D (p.u.)	H***	M****	M	H	M	1	1	1	1	1	1	1	1	1	1	1	1
E (p.u.)	-	1	-	1	1	1	1/H	1/H	1	H	M	1/H	1/H/H	1	1	M	H

* I to XVIII: AWSCs
** A - Number of switches and diodes in the AWSC; B - Voltage peak across main switches; C - Voltage peak across auxiliary switches; D - Current peak in main switches; E - Current peak in auxiliary switches
*** Resonant current peak (High)
**** Limited current peak (Moderate)

TABLE II
OTHER FEATURES OF THE AWSCs

Feature	AWSC
Operation with PDM	I to IV
Operation with PWM	V to XVIII
Good pulse controlability	IV to XII
Excellent pulse controlability	XIII to XVIII
ZCS Converter	I to X, XII to XVI, XVII
ZVS Converter	XI and XVII
AWSC that accept SCRs	all except XI, XV and XVII
Bridges with switches of controlled turn-on and turn-off only	XI and XVII

voltage-regulated CSI AC induction motor", IEEE PESC Conf. Record, 1994, pp. 501-606.

[2] R.H. Osman, "An improved circuit for accelerating commutation in current source inverters", *IEEE Trans. Ind. Appl*, vol. IA-20, Sept./Oct. 1984, pp. 1296-1300.

[3] T.S. Wu, M.D. Bellar. A. Tchamdjou, J. Mahdavi, M. Ehsani, "A Review of soft-switched DC-AC converters", IEEE IAS'1996 Conference Record, 1996, pp. 1133-1144.

[4] M.T. Aydemir, "Analysis and comparison of series resonant DC current link converters", Ph. D. Dissertation, University of Wisconsin-Madison, 1995.

[5] Y. Murai and T.A. Lipo, "High frequency series resonant dc link power conversion", IEEE IAS Annual Conf. Record, 1988, pp. 772-779.

[6] P. Caldeira, T.A. Lipo, Y. Murai, and S. Mochizuki, "Design and control of a series resonant dc link power converter drive", IPEC Conference Record, Tokyo, 1990, pp. 397-404.

[7] R. Castanheira, B.J Cardoso Fo., B.R. Menezes, P. Donoso Garcia, and A.F. Moreira, "An active current clamping circuit for a series resonant dc link power converter", IEEE PESC Conf. Record, 1994, pp. 659-666.

[8] Y. Murai, S.G. Abeyratne, T.A. Lipo, and P. Caldeira, "Series Resonant DC Link Power Conversion Using a Saturable Core", 4th EPE Conference Record, 1991, pp. 2.008-2.012.

[9] Y. Murai, H. Nakamura, T.A. Lipo, and M.T. Aydemir, "Pulse-split concept in series resonant dc link power conversion for induction motor drives", *IEEE Trans. on Ind. Appl.*, Vol. 30, No. 1, Jan./Feb. 1994, pp. 45-51.

[10] E.R.C. da Silva, G. Ledwich, M. Aydemir and T.A. Lipo, "Pulse width modulated series resonant converter", IEEE IAS Annual Conf. Record, 1992, pp. 744-749.

[11] E.R. da Silva and B.J. Cardoso Fo., "A current clamping circuit for a PWM series resonant DC link power converter". IEEE IAS Annual Conference Record, 1995, pp. 2393-2400.

[12] S.G. Abeyratne, E.R. da Silva, and Y. Murai, "PWM series resonant DC-link converter with current clamping by the use of saturable core", in IEEE PESC Conf. Record, 1996, pp. 456-461.

[13] H. Nakamura, Y. Murai and T.A. Lipo, "Quasi resonant current dc link ac/ac converter", *IEEE Trans. on Power Electronics*, Vol. 9, No. 6, Nov. 1994, pp. 594-600.

[14] E.R.C. da Silva, "Notching current current source ac/ac converters for soft switched pwm", IEEE IAS Annual Conf. Record, 1994, pp. 1001-1007.

[15] E.R.C. da Silva, "Soft-switched notching current rectifier/inverter system for induction motor drives", Proceedings of the 3rd Brazilian Conference on

Power Electronics (COBEP'95), 1995, pp. 385-390.
[16] S.G. Abeyratne, M.T. Aydemir, T.A. Lipo, Y. Murai, and M. Yoshida, "Current clamped, PWM, quasi-resonant DC-link series resonant converter", in IEEE IAS Annual Conf. Record, 1994, pp. 820-826.
[17] S.G. Abeyratne, T.A. Lipo, Y. Murai, and J.Horikawa, "Current clamped, modified series resonant dc-link power converter for a general purpose induction motor drive", IEEE APEC Conf. Record, 1994, pp. 267-272.
[18] B.O. Woo and G.H. Cho, "Soft switching four quadrant dc-link inverter generating sinusoidal waveforms", IEEE PESC Conf. Record, 1992, pp. 306-312.
[19] S.A. Chikamenahalli and J.J. Cathey, "A variable frequency resonant commutated inverter", in IEEE IECON Conf. Record, 1995, pp.272-277.
[20] L.P. de Oliveira, "Study and control of pulsed-current DC-link converters" (in portuguese) M.Sc. Dissertation, Federal University of Paraiba, 1997.
[21] G. Moschopoulos and G. Joos, "A novel soft-switched pwm current source rectifier/inverter, IEEE PESC Conf. Record, 1994, pp. 978-984.
[22] G. Ledwich, E.R. da Silva, and T. A. Lipo, "Soft switched notching current source inverters", IEEE PESC Conf. Record, 1992, pp. 1092-1097.
[23] B.O. Woo, J.D. Kim, and G.H. Cho, "Zero voltage switching AC/DC/AC converter using modified high frequency dc-link", IEEE IAS Annual Conf. Record, 1990, pp. 1243-1250.
[24] E.R.C. da Silva, G. Ledwich, T.A. Lipo, and C.B. Jacobina, "DC-link notching current inverter with soft commutation", in 9th Brazilian Conference on Automatic Control Record, 1992, pp. 80-85.
[25] G. Ledwich and F. Shi, "Neutral commutated soft switched current source converter", IEEE PESC'94 Conf. Record, 1994, pp. 714-718.
[26] J.A. Pomílio, L. Rosseto, P. Tenti, P. Tomasin, "Performance improvement of soft-switched PWM rectifiers with inductive dc filter", IEEE PESC'94 Conference Record, 1994, pp. 1425-1430.
[27] S. Buso, L. Rosseto, P. Tenti, P. Tomasin, and J.A. Pomílio, "Soft-switched current-fed PWM inverter with space vector modulation", IEEE IAS`94 Conference Record, 1994, pp. 882-888.
[28] Y. Murai, H. Ishikawa, and T.A. Lipo, "New series resonant DC-link inverter for electric vehicle drives", IEEE IAS Conference Record, 1994, pp. 443-447.
[29] G. Moschopoulos, P. Jain, and G. Joos, "A novel zero-voltage switched pwm boost converter", in IEEE PESC'95 Conference Record, 1995, pp. 694-700.
[30] Y. Murai, S.G. Abeyratne, T.A. Lipo and P. Caldeira, "Dual-flow pulse trimming concepts for a series resonant dc link power conversion", in IEEE PESC Conf. Record, 1991, pp. 254-260.
[31] G. Ledwich, E.R.C. da Silva, M. Aydemir, and T.A. Lipo, "Impact of the control strategy on component rating of series resonant dc link current converter", Proceedings of the Aegian International Conference Turkey, June 1992.
[32] T. Ohnishi and H. Okitsu, "A novel PWM technique for three phase inverter/converter", Proceedings of IPEC'83, 1983, pp. 384-395.
[33] M. Hombu, S. Ueda, and A. Ueda, "A current cource source GTO inverter with sinusoidal input and outputs", *IEEE Trans. on Ind. Appl.*, Vol. IA-23, No. 2, 1987, pp. 247-255.
[34] G. Joos, G. Moschopoulos, and P.D. Ziogas, "A high performance current source inverter", in IEEE PESC Conf. Record, 1991, pp. 123-130.
[35] S. Fukuda and H. Hasegawa, "Current source rectifier/inverter system with sinusoidal currents", IEEE PESC'89 Conference Record, 1988, pp. 909-914.
[36] G. Ledwich, "Current source inverter modulation", *IEEE Trans. on Power Electronics,* Vol.6, No. 4, 1991, pp. 618-623.
[37] K.W. Marschke, P. Caldeira, and T.A. Lipo, "Utilization of the series resonant DC link converter as a conditioning system for SMES", *IEEE Trans. on Power Electronics*, Vol. 7, No. 3, 1992, pp. 506-513.
[38] M.T. Aydemir, P. Caldeira, T.A. Lipo, Y. Murai, E. da Silva, and G. Ledwich, "Utilization of a series resonant DC link for a DC motor drive", *IEEE Trans. on Ind. Applic.*, Vol. 29, No. 5, Sept./Oct. 1993, pp. 949-958.
[39] G. Ledwich, "Resonant inverters for HVDC and FACTS", Proc. of the IEE sponsored APSCOM'93, Hong-Kong, 1993, pp. 237-242.