Research Report

97-19

A Four Level Inverter Based Drive With A Passive Front End

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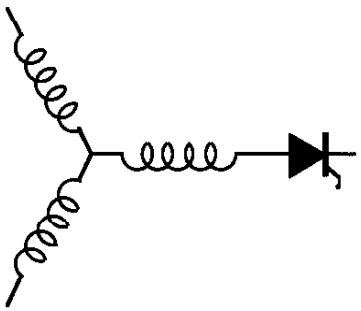

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***Abstract*—Multilevel inverters are suited for high power drive applications due to their increased voltage capability. A four level inverter is able to synthesize better waveforms and attain higher voltages while reducing the device ratings. While converter device count and kVA are high, a conventional diode bridge rectifier is a low cost multilevel drive solution for the input rectifier if suitable inverter side dc voltage balancing schemes can be devised. This paper investigates the operation of four level rectifier/inverter based drives under commonly used modulation schemes. Link voltage balancing and output voltage capability are analyzed for a four level inverter. Simulation results are presented to verify the link voltage balancing strategy in the absence of any balancing action from the rectifier.**

I. INTRODUCTION.

Multilevel inverters are based on the neutral point clamped inverter topology first proposed by Nabae et al [1]. For high power drive applications, three level inverter based drives and control scheme have been extensively studied [2-6]. The trend towards a greater number of levels is necessitated by advantages of higher voltage ratings. For example, 1200V devices are normally required in a conventional VSI with a DC bus voltage of 600V whereas using the same devices and a three level inverter, the DC bus can be rated at 1200V. With a four level inverter, the DC bus voltage can be raised to 1800V. Thus, there are clear advantages to using multilevel inverters especially when the voltages can be raised sufficiently high enough to eliminate transformers.

Associated with multilevel inverter based drives is the problem of DC link voltage balancing. However, redundant states offer a method of redistributing the charge amongst the DC capacitors. The severity of the problem varies with the application. In case of static var compensation, voltage balancing is much easier since the power flow is essentially reactive. It is possible to regulate the link voltages using a low frequency switching scheme and properly selecting the redundant states. In drive applications, the availability of redundant states will determine whether the link voltages can be balanced. Also, it is not always possible to balance the link voltages at every switching event.

In drive applications, real power flow leads to the drift of the link *'neutral'* voltages in a multilevel DC bus. Capacitor voltages can be balanced with the help of an active rectifier as discussed in [7,8,9]. Additionally, with an active rectifier, the DC voltage is reduced and the inverter modulation is relatively unconstrained by voltage balancing requirements. The drawback of this approach is that there are now two active converters which increases the cost of the drive system. Partially active rectifier topologies as in [7] are compromise solutions which have a lower kVA rating than a fully active rectifier and a lower power transfer capability.

In this paper, the passive solution for connecting a multilevel DC bus to the utility - i.e. a diode bridge rectifier front end is considered since it represents the simplest configuration of the multilevel drive. For example, a fully active 4 level rectifier/inverter system has a nominal total device kVA rating of $24V_{dc}I_{max}$, a partially active four level rectifier-four level inverter has a device kVA rating of $22V_{dc}I_{max}$ whereas a diode rectifier-four level inverter system has a total device kVA rating of $18V_{dc}I_{max}$. For larger drives, the cost benefits of reduced device kVA may prove advantageous especially when utility harmonic currents may be reduced by active filters.

II. THE FOUR LEVEL INVERTER.

Of the three prominent multilevel topologies, the diode clamped inverter topology has been found to be suitable for drive applications primarily because of reduced component device ratings and count [10] though the cascaded H bridges topology [11] is extremely modular and robust for practical applications. The four level diode clamped inverter is the only topology discussed further. (Fig. 1).

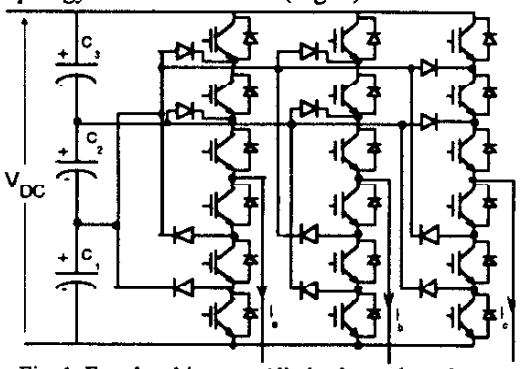

Fig. 1 Four level inverter (diode clamped topology).

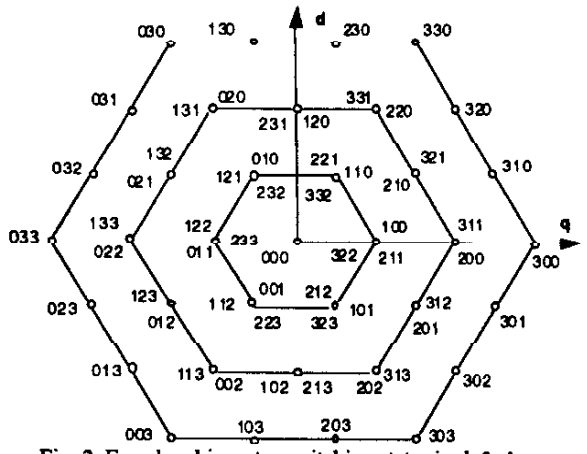

Fig. 2 Four level inverter switching states in *dq0* plane.

Fig. 2 shows the switching states of a four level inverter in the *dq0* plane which are obtained according to the transformation equations:

$$q(h_a,h_b,h_c)=\frac{2}{3}\left(h_a-\left(\frac{h_b+h_c}{2}\right)\right);\ d(h_a,h_b,h_c)=\left(\frac{h_b-h_c}{\sqrt{3}}\right)$$

$$n(h_a,h_b,h_c)=\frac{h_a+h_b+h_c}{3} \qquad (1)$$

Therefore, in a three phase four level inverter there are 64 switching states and can be classified [12] based on their properties as shown in fig. 3. Using the Dirac delta function, the phase A pole voltage can be written in terms of capacitor voltages as:

$$v_{ao}=\delta(h_a-1)V_{C1}+\delta(h_a-2)(V_{C1}+V_{C2})+\delta(h_a-3)(V_{C1}+V_{C2}+V_{C3}) \qquad (2)$$

h_a is the phase A switching function. $h_a = 0, 1, 2$ or 3. It can be deduced by KCL that $I_0 + I_1 + I_2 + I_3 = 0$. Therefore:

$$\delta(h_a-0)+\delta(h_a-1)+\delta(h_a-2)+\delta(h_a-3)=1 \qquad (3)$$

Phase B and C pole voltages can be expressed similarly. The inverter DC node currents can then be represented as:

$$\bar{I}_{DC}(t)=\bar{H}(t)\bar{I}_{ph}(t) \qquad (4)$$

$\bar{I}_{DC}(t)=[I_0(t)\ \ I_1(t)\ \ I_2(t)\ \ I_3(t)]^T$ and

$\bar{I}_{ph}(t)=[i_a(t)\ \ i_b(t)\ \ i_c(t)]^T$

and $\bar{H}(t)=\begin{bmatrix}\delta(h_a-0) & \delta(h_b-0) & \delta(h_c-0)\\ \delta(h_a-1) & \delta(h_b-1) & \delta(h_c-1)\\ \delta(h_a-2) & \delta(h_b-2) & \delta(h_c-2)\\ \delta(h_a-3) & \delta(h_b-3) & \delta(h_c-3)\end{bmatrix}$

For a three wire load $i_a + i_b + i_c = 0$, so (4) is modified to:

$$\bar{I}_{DC}(t)=\bar{M}(t)\bar{I}(t) \qquad (5)$$

where $\bar{I}_{DC}(t)=[I_0(t)\ \ I_1(t)\ \ I_2(t)]^T;\bar{I}(t)=[i_a(t)\ \ i_b(t)]^T$ and

$$\bar{M}(t)=\begin{bmatrix}\delta(h_a)-\delta(h_c) & \delta(h_b)-\delta(h_c)\\ \delta(h_a-1)-\delta(h_c-1) & \delta(h_b-1)-\delta(h_c-1)\\ \delta(h_a-2)-\delta(h_c-2) & \delta(h_b-2)-\delta(h_c-2)\end{bmatrix}$$

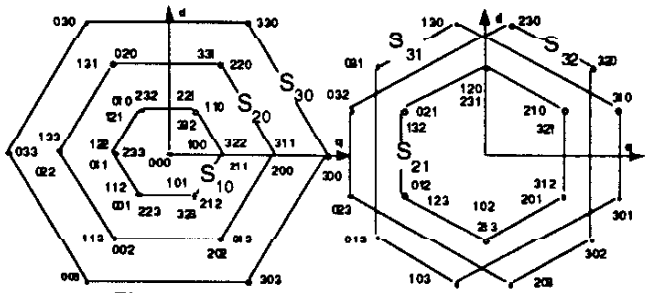

Fig. 3 Inverter switching state classification.

The DC capacitor voltages are given by:

$$C\frac{d}{dt}\bar{v}_C=\bar{F}\bar{I}_{DC}(t) \qquad (6)$$

where $\bar{v}_C=[v_{C1}(t)\ \ v_{C2}(t)\ \ v_{C3}(t)]^T$, $C = 3C_{DC}$ and

$$\bar{F}=[1\ \ 0\ \ 0;\ \ 1\ \ 1\ \ 0;\ \ 1\ \ 1\ \ 1]^T \qquad (7)$$

Therefore, from (5) and (6), we get:

$$C\frac{d}{dt}\bar{v}_C=\bar{F}\bar{M}(t)\bar{I}(t) \qquad (8)$$

Eq. (8) represents a physical system with a variable structure since the matrix $\bar{M}(t)$ is modulation dependent ($0 \le rank(\bar{M}(t)) \le 2$). The differential mode component of each capacitor voltage is then given as:

$$\Delta\bar{V}_C=\bar{V}_C-[1\ \ 1\ \ 1]^T V_{CM}=T\bar{V}_C \qquad (9)$$

where $T=\frac{1}{3}[2\ \ -1\ \ -1;\ \ -1\ \ 2\ \ -1;\ \ -1\ \ -1\ \ 2]^T$

$$V_{CM}=\left(\frac{v_{C1}+v_{C2}+v_{C3}}{3}\right) \qquad (10)$$

Since $rank(T) = 2$, only two of the three capacitor voltage deviations are independent. V_{CM} is the common mode capacitor voltage which can be considered as resulting from a common charging current. By differentiating (9) and substituting (8), one obtains:

$$\frac{d}{dt}\Delta\bar{v}_C=\frac{1}{C}\bar{T}\bar{F}\bar{M}(t)\bar{I}(t) \qquad (11)$$

Capacitor voltage unbalance in an interval $t_0 < t < t_1$ is minimized when:

$$\left\|\Delta\bar{v}_C\right\|=\left\|\int_{t_0}^{t_1}\frac{1}{C}\bar{T}\bar{F}\bar{M}(x)\bar{I}(x)dx\right\|=minimum \qquad (12)$$

A necessary condition for this to occur is:

$$\Delta\bar{v}_C\cdot\bar{T}\bar{F}\bar{M}(t)\bar{I}(t)\le 0 \qquad (13)$$

When (13) is satisfied, the capacitor voltage unbalance is guaranteed to not grow. The interval $t_1 - t_0$ is usually the switching interval over which the load current dynamics do not change appreciably. Hence, at the start of a switching interval, computations can be made about the switching state to be selected based on the currently available values of the load currents. Link voltage balancing then can be formulated as a problem in finding a suitable switching state (h_a,h_b,h_c) which will satisfy (13). There are 64 switching states and finding a switching state to satisfy (13) is, in general extremely computationally intensive. Simplification of (13) leads to a more insightful version of voltage balancing

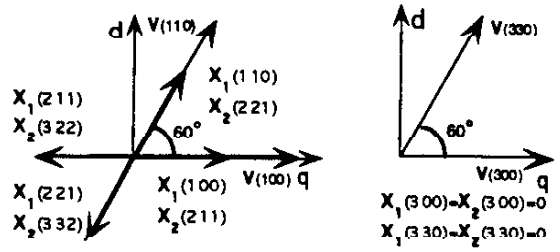

Fig. 5 Disposition of S_{30}, S_{10} voltage & X_1, X_2 vectors.

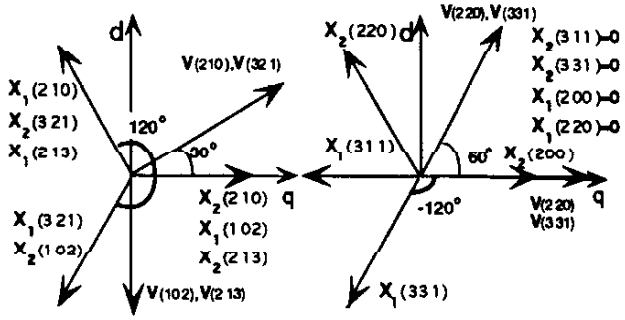

Fig. 6 Disposition of S_{21} S_{20} voltage & X_1, X_2 vectors.

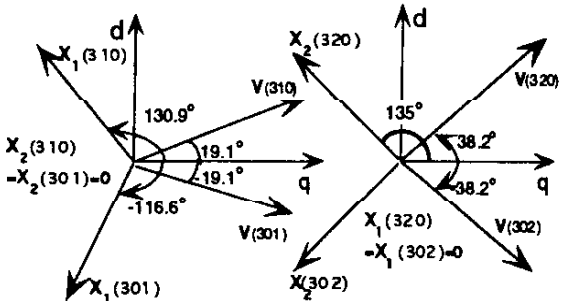

Fig. 7 Disposition of S_{10} voltage & X_1, X_2 vectors.

applied to S_{10} states. According to the balancing scheme, for $\Delta V_1 > 0$ and $\Delta V_2 > 0$, if $X_1(h_a,h_b,h_c)$ belongs to region II (or = 0) then ΔV_1 can be regulated and if $X_2(h_a^*,h_b^*,h_c^*)$ belongs to region II (or = 0) then ΔV_2 can be regulated. In fig. 7, for the load current vector as shown, state *(322)* will regulate the DC voltages most effectively. For S_{10} states, it is always possible to select a switching state which produces current of an appropriate polarity through any DC capacitor.

When a voltage vector corresponding to an S_{21} state is selected, it can be shown that for at least one switching state both DC voltages can be regulated. Thus, from fig. 9 it is

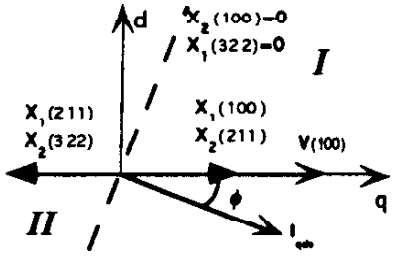

Fig. 8 S_{10} Switching state selection for voltage balancing.

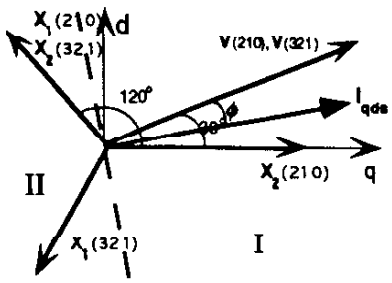

Fig. 9 S_{21} Switching state selection for voltage balancing.

evident that state *(321)* will regulate ΔV_1 and ΔV_2. A similar argument holds for S_{20} states. Graphical equivalence can therefore be derived for each of the switching state classes. For S_{30} states, $X_1 = X_2 = 0$ identically and so link unbalance never worsens as a result of selecting S_{30} states. When an S_{31} or S_{32} state is selected, two cases arise as illustrated in fig. 10. In fig. 10(a), the selection of state *(310)* results in an appropriate polarity of current to regulate ΔV_1 but selection of *(301)* with the load current at the same power factor will cause a charging current of the opposite polarity thereby worsening the unbalance. A similar result can be shown to hold for S_{32} states. When S_{30} states are selected, as stated earlier, the capacitors are charged symmetrically. Thus, when outer hexagon states are used, it follows that unbalance will result.

This is the fundamental limitation in the link voltage balancing capability of the four level inverter. Note that the limitation arises from the fact that there are now no redundant states available which will regulate the DC voltages. Assuming ideal and balanced three phase load currents, in the limiting case when only the S_{31}, S_{32} and S_{30} states are used the average values of the DC currents are given by:

$$\langle I_1 \rangle = -\langle I_2 \rangle = 6\, I \cos\phi \sin(\frac{\lambda}{2}) \cos(2\pi/3 - \lambda); \qquad (21)$$

where $\lambda = 19.11°$ and I is the peak value of the load phase currents. Also,

$$\langle i_{C2} \rangle = \langle i_{C3} \rangle - \langle I_2 \rangle = \langle i_{C3} \rangle - 0.188\, I \cos\phi \qquad (22)$$

$$\langle i_{C1} \rangle = \langle i_{C3} \rangle - (\langle I_2 \rangle + \langle I_1 \rangle) = \langle i_{C3} \rangle \qquad (23)$$

Thus, the innermost capacitor tends to discharge for any real load because $\cos\phi \neq 0$. Also, there is symmetry in the charging of V_{C1} and V_{C3}. Typically, in the absence of any balancing action, V_{C2} undergoes inversion leading to a catastrophic shutdown.

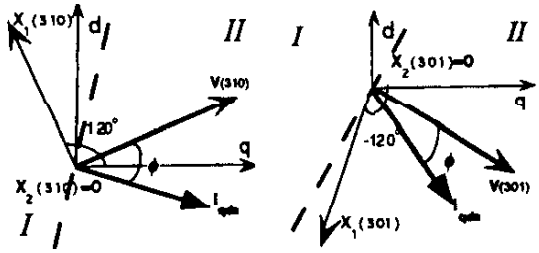

Fig. 10 S_{31} Switching state selection for voltage balancing.

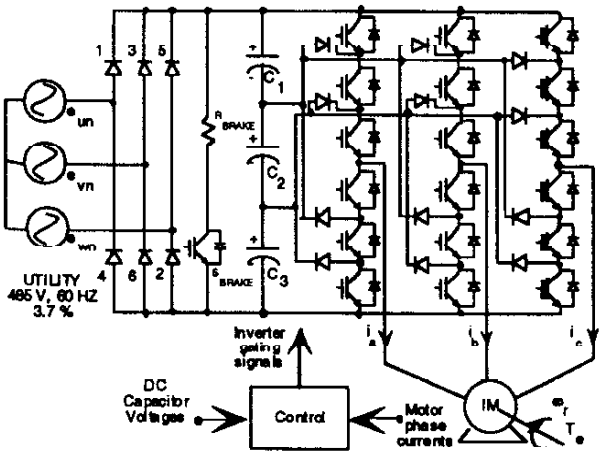

Fig. 11 Four level inverter based drive system.

IV. SIMULATION RESULTS.

Fig. 11 shows the drive system that has been simulated to verify the theory developed in the previous sections. This system is currently being constructed at the University of Wisconsin. The load is a 15 HP 8 pole 460/230V induction motor. 600V/100A IGBTs are used as the active switches. The control scheme implemented is based on the scheme outlined in the previous section. In [14], a control scheme for such a topology with R-L loads only is discussed.

Fig. 12 shows the block diagram of the control scheme. A four level PWM scheme provides the pulse pattern to a redundant state selector. The link voltage balancing scheme is the redundant state selector. Input to this block can

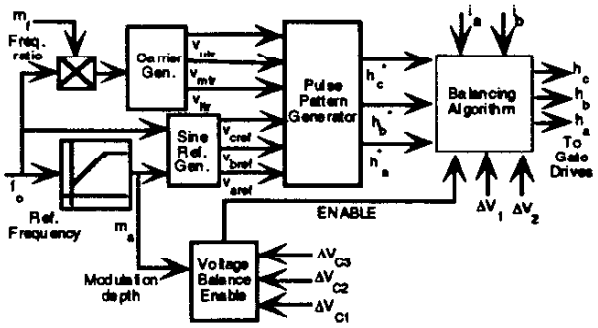

Fig. 12 Inverter control scheme.

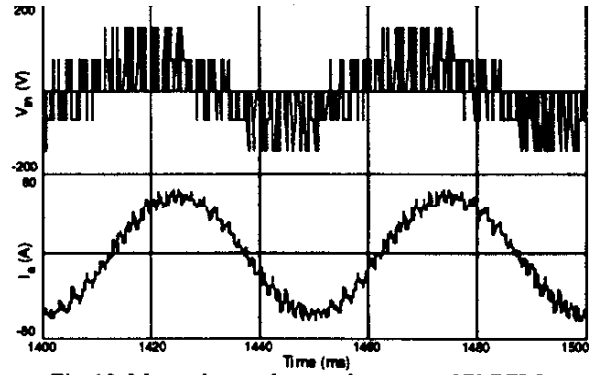

Fig. 13 Motor phase voltage and current at 273 RPM.

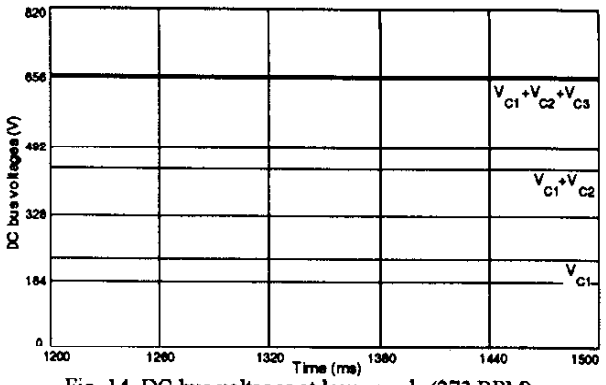

Fig. 14 DC bus voltages at low speeds (273 RPM).

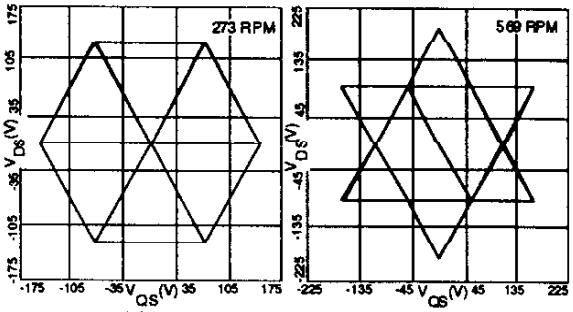

Fig. 15 V_{qs} and V_{ds} at 20 & 40 Hz.

be voltage vectors resulting from any control scheme such as current regulation or field orientation. In this particular case, a simple V/Hz control scheme was implemented. Fig. 13 shows the motor phase voltage and current for a low speed operation case. For a low carrier frequency of 420 Hz, the current THD is reasonably low at about 11%. The actual device switching frequency varies with the location of the device in the inverter pole. Depending on the load currents and link voltages, the actual device switching frequency can be as high as three times the carrier frequency if at every reference - triangle intersection a transition occurs in all phase switching functions. At low modulation indices, vectors with higher redundancies are selected i.e. only S_{10} states are being used, hence the link voltages are balanced as is shown in fig. 14.

Fig. 15 shows the motor q and d axis voltage in the stationary reference frame when the synchronous frequency

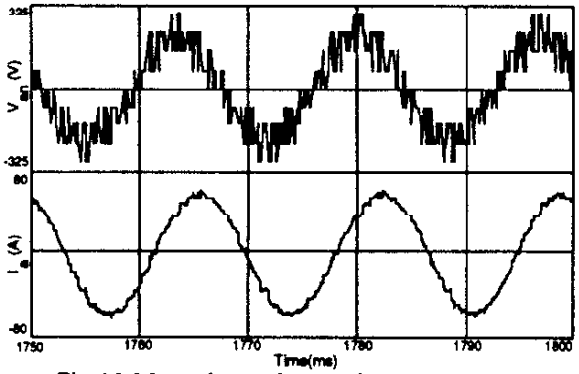

Fig. 16 Motor phase voltage and current at 60 Hz.

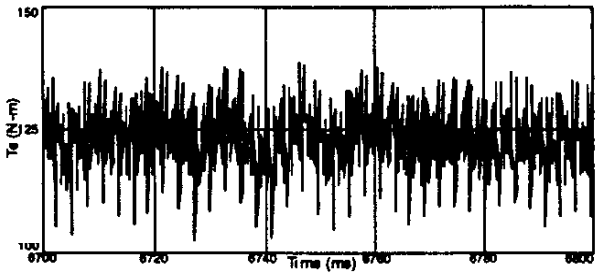

Fig. 17 Motor torque at 60 Hz rated point.

is 20 Hz and 40 Hz. As the modulation depth is increased, S_{10} and S_{21} states are selected as shown in fig. 15(b). In this case, link voltages can be still balanced because modulation in this range can be considered as a superposition of two modulations - one using only S_{10} states and the other using only S_{21} states. For a fixed 'gear ratio', as the synchronous frequency increases at constant V/Hz the current THD improves significantly because the motor leakage reactance is better able to filter the currents. This results in reduced phase current THD (4.4%) at the rated point of the motor as shown in fig. 16. Motor torque is traced in fig. 17 which suggests a peak-peak torque ripple of about 20%.

The inverter operates at the limits of its voltage capability while retaining four level inverter operation when $m_a \geq 0.75$ (approx.). Scant use is made of S_{11}, S_{12} or S_{13} states as seen in fig. 18(a) where the synchronous frequency is 90 Hz and the motor produces 80N-m torque (field weakening). Link voltages are still balanced as shown in fig. 19. The induction motor leakage reactance now filters the current further so that the current THD stays low (5.2%) even when the carrier

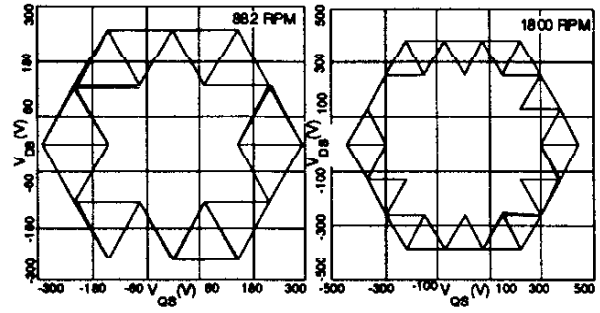

Fig. 18 V_{qs}, V_{ds} at 90 and 120 Hz operation.

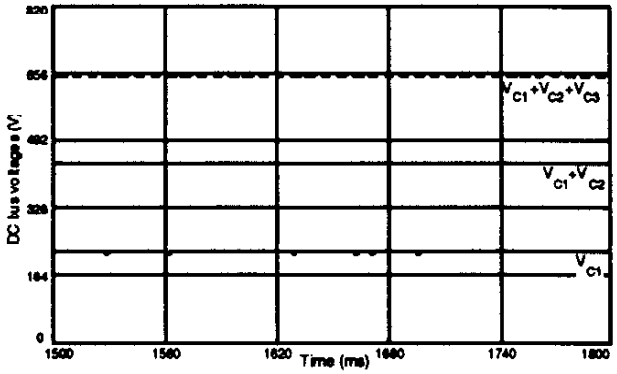

Fig. 19 Link voltages at 90 Hz.

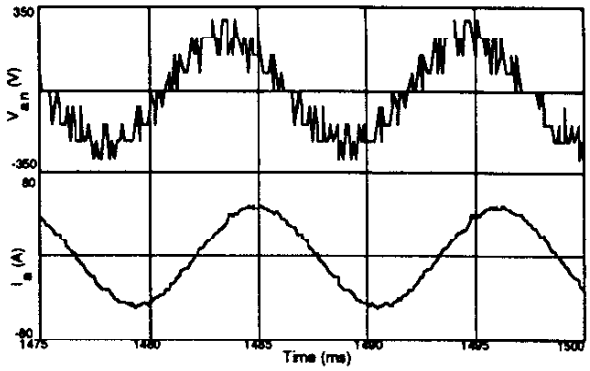

Fig. 20 Motor phase current and voltage at 90 Hz.

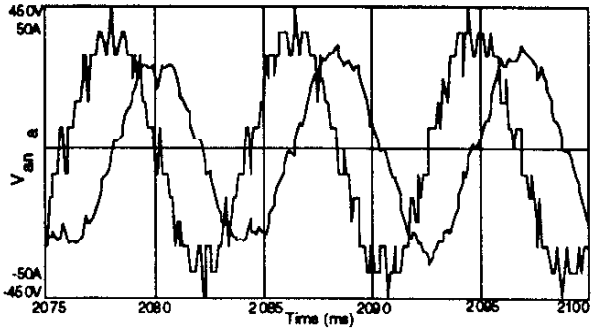

Fig. 21 Motor phase voltage and current at 120 Hz.

frequency is dropped (fig. 20). Finally, fig. 21 shows the motor phase and current under no load conditions when the inverter synchronous frequency is 120 Hz. As seen in fig. 18(b), the inverter modulation makes use of the outermost states (S_{31}, S_{32}, S_{30}) since the modulation depth is high ($\approx$ 1.33). Also at no load, the motor impedance is chiefly inductive so that $\cos\phi \approx 0$. Hence, in accordance with (21)-(23), $\langle I_{C1} \rangle = \langle I_{C2} \rangle = \langle I_{C3} \rangle \approx 0$ and so the link voltages stay balanced. This is reflected in fig. 22 showing the well regulated DC link voltages.

Although the four level inverter cannot balance the capacitor voltages satisfactorily for $m_a \geq 0.75$ and deliver real power to the load, in applications wherein higher voltages are required, the inverter can be made to operate in the two level mode i.e. selecting only S_{30} states - thereby trading off voltage THD for fundamental voltage magnitude.

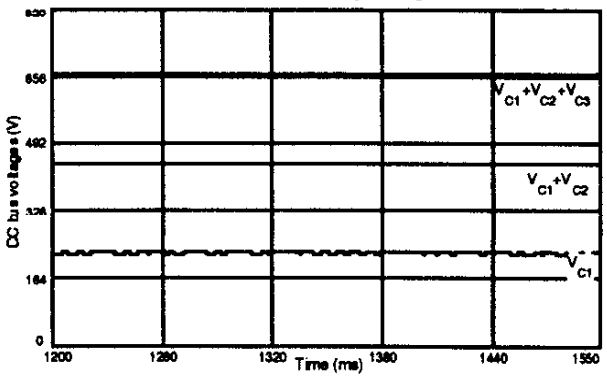

Fig. 22 DC link capacitor voltages at no load and 120 Hz.

V. CONCLUSIONS.

Four level inverters based drives with a diode rectifier front end offer the prospect of reduced total kVA ratings. A new methodology for viewing concurrent link voltage balancing and inverter modulation was discussed. It is possible to obtain low THD voltage waveforms from the four level inverter while retaining adequate link voltage balancing capability. This makes such drives suitable for applications wherein low speed operation is the dominant mode of operation. The voltage THD can be lowered at lower average device switching frequencies. Time domain simulations indicate that the control scheme for link voltage balancing outlined earlier are viable over the entire motoring region. If necessary, the voltage capability of the four level inverter can be improved by reverting the modulation to a conventional two level scheme.

REFERENCES

[1] A. Nabae, I. Takahashi, H. Akagi, "A New Neutral Point Clamped PWM Inverter", *IEEE Trans. on Ind. App.*, Vol. IA-17, No. 5, September/October 1981, pp. 518-523.

[2] J.K. Steinke, "Control Strategy for a Three Phase AC Traction Drive with Three Level GTO PWM Inverter", *Proc. IEEE-PESC '88 Conf.*, pp. 431-438.

[3] Jie Zhang, "High Performance Control of a 3 Level IGBT Inverter Fed AC Drive", *Proc. IEEE-IAS '95 Conf.*, pp. 22-28

[4] Satoshi Ogasawara, Hirofumi Akagi, "A Vector Control System Using a Neutral-Point-Clamped Voltage Source PWM Inverter", *Proc. IEEE-IAS '91 Conf.*, pp. 422-427.

[5] A. Nabae, S. Ogasawara, H. Akagi, "A Novel Control Scheme for Current Controlled PWM Inverters", *IEEE Trans. on Ind. App.*, Vol. IA-22, No. 4, July/Aug., '81, pp. 697-701.

[6] T. Takeshita, N. Matsui, "PWM Control and Input Characteristics of Three Phase Multilevel AC/DC Converters", *Proc. IEEE-PESC '92 Conf.*, pp. 175-180.

[7] Y. Zhao, Y. Li, and T. A. Lipo, "Force Commutated Three Level Boost Type Rectifier", *IEEE Trans. on Ind. App.*, Vol. 31, no. 1, Jan./Feb. 1995, pp. 155-161.

[8] Michael Klabunde, Yifan Zhao, T.A. Lipo, " Current Control of a 3 Level Rectifier/Inverter Drive System", *Proc. IEEE-IAS '94 Conf.*, pp. 859-865.

[9] Gautam Sinha, T.A. Lipo, "A Four Level Rectifier-Inverter System for Drive Applications", *Proc. IEEE-IAS '96 Conf.*, pp. 980-987.

[10] Clark Hochgraf, R.H. Lasseter, D.M. Divan, T.A. Lipo, "Comparison of Multilevel Inverters for Static Var Compensation", *Proc. IEEE-IAS '94 Conf.*, pp. 921-928.

[11] F.Z. Peng, J.S. Lai, "A Multilevel Voltage-Source Inverter With Separate DC Sources", *Proc. IEEE-IAS '95 Conf.*, pp. 2541-2548

[12] Gautam Sinha, T.A. Lipo, "Rectifier Current Regulation in Four Level Drives", *Proc. IEEE-APEC '97 Conf.*,

[13] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis", *Proc. IEEE-PESC '90 Conf.*, pp. 363-371

[14] M. Fracchia, T. Ghiara, M. Marchesoni, M. Mazzucchelli, "Optimized Modulation Techniques for the Generalized N-Level Converter", *Proc. IEEE-PESC '90 Conf.*, pp. 1205-1213.