A Four-Level Inverter Based Drive with a Passive Front End

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***Abstract*—Multilevel inverters are suited for high power drive applications due to their increased voltage capability. Specifically, as compared to three level inverters, for a given dc bus voltage, a four-level inverter is able to synthesize better waveforms with reduced device ratings. In a medium voltage drive, a conventional diode bridge rectifier is a low cost multilevel solution if the dc bus voltages can be balanced from the inverter side alone. In this paper, operation of four-level drive with a passive rectifier is investigated, and modulation constraints of the inverter, arising from the capacitor voltage balancing requirements are examined. Simulation and experimental results are presented to demonstrate the link voltage balancing strategy and the performance of the four-level drive.**

***Index Terms*—Diode clamped inverters, four level inverters, high power drives, multilevel converters.**

I. Introduction

THE diode clamped multilevel inverters are based on the neutral point clamped inverter topology proposed by Nabae *et al.* [1] and first cited in patent [16]. For high power drive applications, three level inverter based drives and control schemes have been extensively studied [2]–[6]. The trend toward a greater number of levels is necessitated by advantages of higher voltage ratings. For example, 1200 V devices are normally required in a conventional VSI with a dc bus voltage of 600 V whereas using the same devices and a three level inverter, the dc bus can be rated at 1200 V. With a four-level inverter, the dc bus voltage can be raised to 1800 V. The need for transformers for higher voltages is obviated at higher voltages.

Associated with multilevel inverter based drives is the problem of dc link voltage balancing. However, redundant states offer a method of redistributing the charge amongst the dc capacitors. In case of static var compensation, since the power flow is essentially reactive, it is possible to regulate the link voltages using a low frequency switching scheme and switching along a trajectory determined *a priori*. In drive applications, the availability of redundant states and load power factor determine whether the link voltages can be balanced. This dependency on the modulation depth implies that the availability of a switching state for re-balancing the capacitor voltages is not guaranteed.

In drive applications, real power flow leads to the drift of the link '*neutral*' voltages in a multilevel dc bus. Capacitor voltages can be balanced with the help of an active rectifier as discussed in [7]–[9]. Additionally, with an active rectifier, the inverter modulation is relatively unconstrained by voltage balancing requirements. The drawback of this approach is that there are now two active converters which increases the cost of the drive system. Partially active rectifier topologies as in [7] are compromise solutions, which have a lower kVA rating than a fully active rectifier and a correspondingly lower peak power transfer capability.

In this paper, the passive solution for connecting a multilevel dc bus to the utility—i.e. a diode bridge rectifier front end is considered since it represents the simplest configuration of the multilevel drive. For example, a fully active 4 level rectifier/inverter system has a nominal total device kVA rating of $24V_{dc}I_{\max}$; a partially active four-level rectifier-four-level inverter has a total device kVA rating of $22V_{dc}I_{\max}$ whereas a diode rectifier-four-level inverter system has a total device kVA rating of $18V_{dc}I_{\max}$. For larger drives, the cost benefits of reduced device kVA may prove advantageous especially when utility harmonic current filters are used.

II. The Four-Level Inverter

Of the three prominent multilevel topologies, the diode clamped inverter topology has been found to be suitable for drive applications primarily because of reduced component device ratings and count [10]. Though the cascaded H bridge topology [11] is extremely modular and robust for practical applications, the four-level diode clamped inverter is the only topology discussed further (Fig. 1).

The terminology in this paper is explained with reference to Fig. 2 which depicts a four-level dc bus structure and each inverter phases is modeled as 4-pole switch. The inverter switching functions shown assume values of $h_a = 2$, $h_b = 0$, $h_c = 3$. This is equivalent to stating that phase A of the inverter is connected to the upper dc neutral, phase B is connected to negative dc bus and phase C to the positive dc bus. In general therefore, the inverter pole voltage with respect to the negative dc bus can be written in terms of capacitor voltages and the switching functions as

$$\begin{aligned} v_{ao}(h_a) &= \delta(h_a-1)v_{C1} + \delta(h_a-2)\left(v_{C1}+v_{C2}\right) \\ &\quad + \delta(h_a-3)\left(v_{C1}+v_{C2}+v_{C3}\right) \\ v_{bo}(h_b) &= \delta(h_b-1)v_{C1} + \delta(h_b-2)\left(v_{C1}+v_{C2}\right) \\ &\quad + \delta(h_b-3)\left(v_{C1}+v_{C2}+v_{C3}\right) \\ v_{co}(h_c) &= \delta(h_c-1)v_{C1} + \delta(h_c-2)\left(v_{C1}+v_{C2}\right) \\ &\quad + \delta(h_c-3)\left(v_{C1}+v_{C2}+v_{C3}\right) \end{aligned} \tag{1}$$

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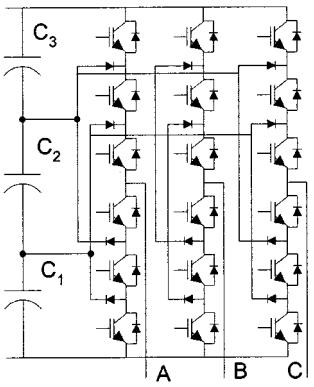

Fig. 1. Four-level inverter (diode clamped topology).

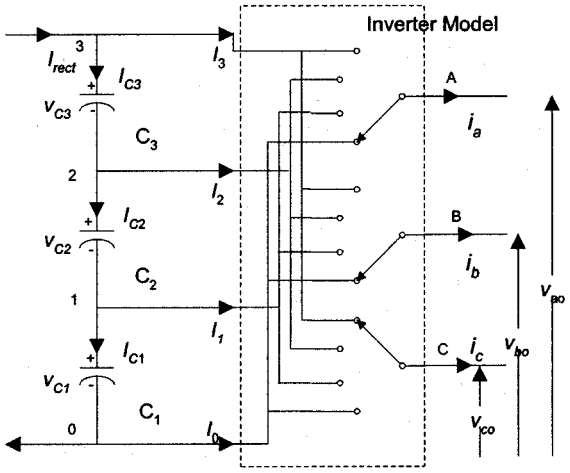

Fig. 2. Terminology for a four-level dc bus.

where $\delta(\cdot)$ is the continuous time Dirac delta function. In the steady state (nominal operating case), $V_{C1} = V_{C2} = V_{C3} = V_{dc}/3$ and therefore, inverter output phase voltage (with respect to the negative dc bus) is seen to be proportional to the numerical value of the phase switching function since

$$v_{ao} = \frac{V_{dc}}{3} \sum_{k=1}^{3} k\delta(h_a - k) = \frac{V_{dc}}{3} h_a. \tag{2}$$

The three orthogonal components of the inverter phase voltages are obtained by applying the stationary Park transformations (non power-invariant version) to the inverter output voltages

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ v_{0s} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos 0 & \cos(2\pi/3) & \cos(2\pi/3) \\ -\sin 0 & \sin(2\pi/3) & -\sin(2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \cdot \begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix}. \tag{3}$$

Fig. 3 shows the distribution of the voltage vectors of (3) in the $dq0$ plane as functions of inverter switching states h_a, h_b, h_c. The mapping represented by ignoring the last row of (3) is many-one and therefore, in a three phase four-level inverter there are 64 switching states that produce only 37 distinct voltage vectors in a three wire load. The switching states can be classified [12] based on their voltage and current properties as shown in Fig. 4. S_{10} states produce the smallest line voltages and only one non zero capacitor current. Neglecting any dc current from source converter, S_{21} states produce the next largest line voltages and cause currents of opposite polarity and unequal magnitude to flow through the inner and one of the outer capacitors. The third capacitor current is identically zero for both S_{21} and S_{20} states. S_{20} states produce larger line voltages and equal capacitor currents through two of the capacitors. S_{31} and S_{32} states produce currents of the same polarity through the inner and one of the outer capacitors, while the other outer capacitor current has the opposite polarity. S_{30} states produce the largest line voltages and correspond to the equivalent two level inverter switching states. S_{30} states also produce equal capacitor charging currents.

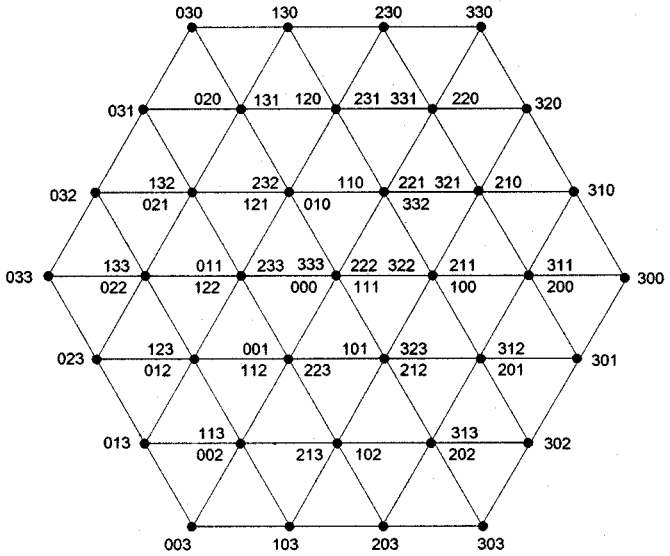

Fig. 3. Four-level inverter switching states in $dq0$ plane.

Now, using the same notation, the inverter dc currents can be expressed by the dual of (1) as

$$\begin{aligned} I_1(h_a, h_b, h_c) &= \delta(h_a - 1)i_a + \delta(h_b - 1)i_b + \delta(h_c - 1)i_c \\ I_2(h_a, h_b, h_c) &= \delta(h_a - 2)i_a + \delta(h_b - 2)i_b + \delta(h_c - 2)i_c \\ I_3(h_a, h_b, h_c) &= \delta(h_a - 3)i_a + \delta(h_b - 3)i_b + \delta(h_c - 3)i_c. \end{aligned} \tag{4.1}$$

Since $I_1 + I_2 + I_3 + I_4 = 0$, it follows that

$$\begin{aligned} I_0(h_a, h_b, h_c) = -(&I_0(h_a, h_b, h_c) + I_2(h_a, h_b, h_c) \\ &+ I_3(h_a, h_b, h_c)). \end{aligned} \tag{4.2}$$

The capacitor charging currents are related to inverter dc currents by

$$\begin{aligned} I_{C3}(h_a, h_b, h_c) &= I_{rect} - I_3(h_a, h_b, h_c) \\ I_{C2}(h_a, h_b, h_c) &= I_{rect} - I_3(h_a, h_b, h_c) - I_2(h_a, h_b, h_c). \end{aligned} \tag{5}$$

The dc capacitor voltages are then given by

$$\mathbf{C}\frac{\mathbf{d}}{\mathbf{dt}}\mathbf{V_C} = \mathbf{I_{rect}}\mathbf{I}_{bf3} - \mathbf{F}\mathbf{I_{DC}} \tag{6.1}$$

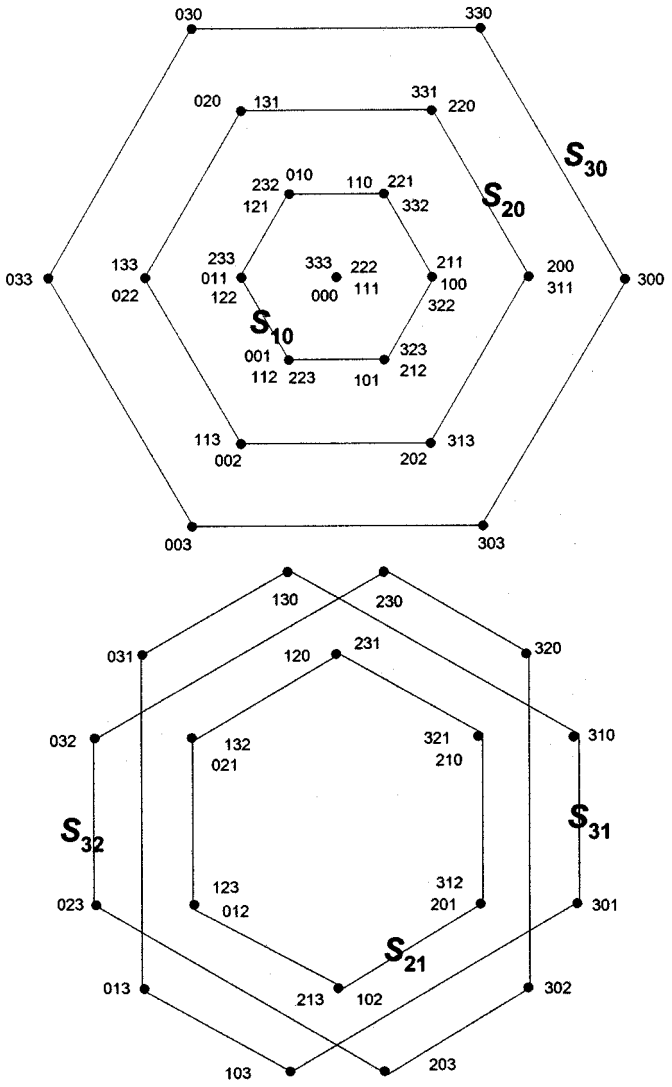

Fig. 4. Inverter switching state classification.

where $\mathbf{I_3}$ is the 3 × 3 identity matrix, and $\mathbf{I_{DC}}$ is derived from (4.1), i.e.

$$\mathbf{I_{DC}} = [I_1(h_a,h_b,h_c) \quad I_2(h_a,h_b,h_c) \quad I_3(h_a,h_b,h_c)]' \tag{6.2}$$

$$\mathbf{F} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix}, \qquad \mathbf{V_C} = [v_{C1} \quad v_{C2} \quad v_{C3}]'. \tag{6.3}$$

The capacitor voltages may be considered as the sum of a common mode voltage and a differential or relative deviation voltage i.e.

$$\mathbf{V_C} = [V_{CM}+\Delta v_{C1} \quad V_{CM}+\Delta v_{C2} \quad V_{CM}+\Delta v_{C3}]'. \tag{7.1}$$

In that case, the voltage deviations can be rewritten as

$$\mathbf{C}\frac{\mathbf{d}}{\mathbf{dt}}\mathbf{V} = \mathbf{G}\mathbf{I_{DC}} \tag{7.2}$$

where

$$G = \begin{bmatrix} -2/3 & -1/3 & 0 \\ 1/3 & -1/3 & 0 \\ 1/3 & 2/3 & 0 \end{bmatrix} \quad \text{and}$$
$$\mathbf{V} = [\Delta v_{C1} \quad \Delta v_{C2} \quad \Delta v_{C3}]'. \tag{7.3}$$

Since the third column of matrix G is identically 0, only the neutral current I_2 and I_3 have any impact on the relative voltage deviations. In the balanced link condition, $\Delta V_{C1} = \Delta V_{C2} = \Delta V_{C3} = 0$ which can be shown from (7.3) to occur only when $I_2 = I_1 = 0$. In order to derive a balancing strategy, consider an initial voltage deviation pattern at time $t = t_0$ given by; then, the deviations at a time $t = t_0 + \Delta T$ are given by

$$\Delta v_{Cj}(t_0+\Delta T) \approx \Delta v_{Cj}(t_0) + \frac{I_{Cj}(h_a,h_b,h_c)}{C_j}; \quad j = 1,2,3. \tag{8}$$

The capacitor charging currents depend on the inverter switching state according to (4). In order that the voltage deviation be minimized, it can be inferred that the capacitor voltage deviation and the charging current through the capacitor should be opposite polarity, i.e.

$$\begin{aligned} \Delta v_{C1}(t_0) I_{C1}(h_a,h_b,h_c) &\le 0 \\ \Delta v_{C2}(t_0) I_{C2}(h_a,h_b,h_c) &\le 0 \\ \Delta v_{C3}(t_0) I_{C3}(h_a,h_b,h_c) &\le 0. \end{aligned} \tag{9}$$

Therefore, a necessary and sufficient condition for voltage balancing is derived to be

$$Q = \max\{\Delta v_{C1} I_{C1}, \Delta v_{C2} I_{C2}, \Delta v_{C3} I_{C3}\} \le 0 \tag{10}$$

where the explicit dependence on the switching state and time is dropped for notional convenience. Also from (5), the capacitor currents may be expressed as

$$\mathbf{I_C}(h_a,h_b,h_c) = I_{rect}\mathbf{I_3} + \mathbf{F}\mathbf{I_{DC}}(h_a,h_b,h_c) \tag{11}$$

where

$$\mathbf{I_C}(h_a,h_b,h_c) = [I_{C1}(h_a,h_b,h_c) \quad I_{C2}(h_a,h_b,h_c) \quad I_{C3}(h_a,h_b,h_c)]'.$$

Equation (10) indicates that the capacitor currents are dependent on the switching state (h_a, h_b, h_c) selected at the time instant $t = t_0$. Together, (10) and (11) suggest the modulation strategy for concurrently balancing the link voltages as well as producing the required output voltages. The voltage balancing modulation strategy assumes that the voltage vectors required to be generated (V_{qs}^*, V_{ds}^*) are derived from an appropriate control scheme. Switching states that produce the required voltage vector are therefore derived as per

$$\begin{bmatrix} 1 & -0.5 & -0.5 \\ -0.5 & 1.25 & -0.75 \\ -0.5 & -0.75 & 1.25 \end{bmatrix} \begin{bmatrix} h_a \\ h_b \\ h_c \end{bmatrix} = \begin{bmatrix} 4.5 & 0 \\ -2.25 & 5.1975 \\ -2.25 & -5.1975 \end{bmatrix} \begin{bmatrix} \frac{V_{qs}^*}{V_{dc}} & \frac{V_{ds}^*}{V_{dc}} \end{bmatrix}'. \tag{12}$$

TABLE I
SWITCHING STATE SELECTION FOR $-(V_{dc}/3, -2V_{dc}/3\sqrt{3})$ FOR ALL LOAD CURRENT POLARITIES

Sign(i_a)	Sign(i_b)	Sign(i_c)	Sign(P(0,1,2))	Sign(P(1,2,3))	Condition	switching state
+	-	-	+	+	If $\Delta V_{C3}\, i_b < -\Delta V_{C1}\, i_a$	(1,2,3)
+	+	-	+	-	Unconditional	(1,2,3)
-	+	-	+	+	If $\Delta V_{C2}\, i_a < -\Delta V_{C2}\, i_b$	(1,2,3)
-	+	+	+	+	If $\Delta V_{C1}\, i_b < \Delta V_{C1}\, i_a$	(1,2,3)
-	-	+	-	+	Unconditional	(0,1,2)
+	-	+	+	+	If $-\Delta V_{C3}\, i_b < \Delta V_{C1}\, i_a$	(1,2,3)

In (12), there is apparently one degree of freedom for determining the switching states. A unique solution can be arrived upon by the additional constraint that only integer solutions are permitted i.e. for an N level inverter

$$h_a, h_b, h_c = 0, 1, 2, 3, \cdots, N-1. \tag{13}$$

If the inverter modulation produces a legitimate reference voltage vector, at least one integer solution of (12) is guaranteed to exist. The exact number of solutions depends on the magnitude of the voltage vector. For instance, the switching states that will produce the reference voltage vector $(V_{dc}/9, V_{dc}/3\sqrt{3})$ are $(h_a = 1, h_b = 1, h_c = 0)$, $(h_a = 2, h_b = 2, h_c = 1)$ and $(h_a = 3, h_b = 3, h_c = 2)$. The three switching states, however differ in the capacitor charging currents produced. State (110) produces the capacitor currents given as: $(I_{C1} = i_c, I_{C2} = 0, I_{C3} = 0)$, state (221) produces the currents $(I_{C1} = 0, I_{C2} = i_c, I_{C3} = 0)$ and state (322) produces the currents $(I_{C1} = 0, I_{C2} = 0, I_{C3} = i_c)$. Therefore, evaluating (13) for each switching state

$$\begin{aligned} Q(1,1,0) &= \max(\Delta v_{C1}, i_c, 0, 0), \\ Q(2,2,1) &= \max(0, \Delta v_{C2}, i_c, 0), \\ Q(3,3,2) &= \max(0, 0, \Delta v_{C3} i_c). \end{aligned}$$

The actual switching state selected will depend on the relative magnitudes of $Q(1,1,0)$, $Q(2,2,1)$ and $Q(3,3,2)$. That switching state (h_a^*, h_b^*, h_c^*) is selected which produces the minimum value of Q i.e.

$$\begin{aligned} (h_a^*, h_b^*, h_c^*) \ni Q(h_a^*, h_b^*, h_c^*) \\ = \min(Q(1,1,0), Q(2,2,1), Q(3,3,2)). \end{aligned} \tag{14}$$

A unique switching state is identified if we modify the criterion (17) to

$$\begin{aligned} (h_a^*, h_b^*, h_c^*) \ni P(h_a^*, h_b^*, h_c^*) \\ = \min(P(1,1,0), P(2,2,1), P(3,3,2)) \end{aligned} \tag{15}$$

where $P(1,1,0) = \Delta v_{C1} i_c$, $P(2,2,1) = \Delta v_{C2} i_c$ and $P(3,3,2) = \Delta v_{C3} i_c$.

One of the most common voltage deviations are: $\Delta v_{C2} < 0$, $\Delta v_{C1} > \Delta v_{C3} > 0$ and $|\Delta v_{C2}| > |\Delta v_{C1}|$. Therefore, if $i_c > 0$, state (2,2,1) would be selected, else if $i_c < 0$, state (1,1,0) is selected. In essence, that switching state is selected which causes a negative power transfer from the capacitor with the largest voltage deviation. This criterion is valid for all S_{10} states. When the reference voltage vector is such that an S_{21} or S_{20} (1 redundancy) state is to be selected, the form of the selection criterion is modified. For example, consider the case when the reference voltage vector is $(-V_{dc}/3, -2V_{dc}/3\sqrt{3})$, the corresponding switching states are (0,1,2) and (1,2,3). In this case, from (10), we get

$$\begin{aligned} Q(0,1,2) &= \max(\Delta v_{C1}, i_a, -\Delta v_{C2} i_c, 0) \quad \text{and} \\ Q(1,2,3) &= \max(0, \Delta v_{C2} i_c, -\Delta v_{C3} i_c). \end{aligned} \tag{16}$$

Once again, that switching state is selected which tends to redistribute the charges; e.g. if $Q(0,1,2) < Q(1,2,3)$ state (0,1,2) is selected. However, if $Q(0,1,2) = 0$ or $Q(1,2,3) = 0$, it is still possible to select a switching state which will tend to rebalance the capacitor voltages by considering

$$\begin{aligned} P(0,1,2) &= \max(\Delta v_{C1} i_a, -\Delta v_{C2} i_c) \quad \text{and} \\ P(1,2,3) &= \max(\Delta v_{C2} i_a, -\Delta v_{C3} i_c). \end{aligned} \tag{17}$$

Table I lists the switching states that would be selected for the deviation pattern given as: $\Delta v_{C2} < 0$, $\Delta v_{C1} > \Delta v_{C3} > 0$ and $|\Delta v_{C2}| > |\Delta v_{C1}|$.

Characteristic of the decision structure outlined is the explicit dependence of the selected switching state on the magnitude of the load currents and the voltage deviations. A feature of redundant state selection that emerges from Table I is that computations are involved in order to make a consistent voltage balancing decision—in contrast to three level case where the polarity of the neutral voltage and currents suffice. For four and higher level converters, additional computations are required even in a look-up table implementation. Therefore, in this study, a dynamic redundant state selection strategy was favored over a lookup table based approach.

When the inverter is required to produce a voltage vector that can be realized by only one switching state (S_{31} and S_{32} states), negative instantaneous incremental power transfer through each capacitor is not possible. In fact when the modulation depth $m_a (= |V_{ref,pk}|/(V_{dc}/2))$ is sufficiently high $(0.78 \leq m_a \leq 1.115)$ it can be shown that the average inverter induced capacitor DC currents are related by

$$\langle I_{C2} \rangle = \langle I_{C1} \rangle - 0.188 I \cos\phi \tag{17a}$$

where ϕ is the load power factor angle, I is the peak load phase current. Thus, except for purely reactive loads, at higher

modulation depths, the innermost capacitor discharges rapidly whereas the outer two capacitors charge up.

III. A Graphical Representation of the Link Voltage Balancing Criterion

In the previous section, a mathematical condition for link voltage balancing was derived based on the knowledge of the capacitor voltages and the load currents. As Table I indicates, the precise relationship between the selected switching states and the load current is not at all obvious. In order to develop a physical intuition for the balancing action, a graphical approach is introduced in this section. It will be seen that notions from the two level case carry over to the multilevel case and can be used to advantage in visualizing the link voltage-balancing algorithm. Assuming a three-wire load, the load phase currents are expressed in terms of the stationary d and q axis currents as

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -0.5 & j0.866 \\ -0.5 & -j0.866 \end{bmatrix} \begin{bmatrix} I_{qs} \\ I_{ds} \end{bmatrix}. \tag{18}$$

Substituting (18.i)–(18.iii) in (14), the capacitor currents can be expressed in terms of the load current vector and a set of new dimension-less vectors $\overline{X}_{qdC1}$, $\overline{X}_{qdC2}$, $\overline{X}_{qdC3}$ as

$$\begin{aligned} I_{C3}(h_a,h_b,h_c) &= 1.5(X_{qC3}I_{qs} + X_{dC3}I_{ds}) \\ &= 1.5\ \mathrm{Re}\{\overline{X}_{qdC3}\overline{I}_{qds}\} \\ I_{C2}(h_a,h_b,h_c) &= 1.5(X_{qC2}I_{qs} + X_{dC2}I_{ds}) \\ &= 1.5\ \mathrm{Re}\{\overline{X}_{qdC2}\overline{I}_{qds}\} \\ I_{C1}(h_a,h_b,h_c) &= 1.5(X_{qC1}I_{qs} + X_{dC1}I_{ds}) \\ &= 1.5\ \mathrm{Re}\{\overline{X}_{qdC1}\overline{I}_{qds}\}. \end{aligned} \tag{19}$$

The "X-vectors" of (19) are important constructs that enable a visual representation of the capacitor charging currents. The constituent terms of the vectors are given as

$$X_{qC3} = \frac{2}{3}\left\{\delta(h_a-3) - \left(\frac{\delta(h_b-3)+\delta(h_c-3)}{2}\right)\right\} \tag{20.1}$$

$$X_{dC3} = \frac{\delta(h_b-3)-\delta(h_c-3)}{3\sqrt{3}} \tag{20.2}$$

$$X_{qC2} = \frac{2}{3}\left\{\delta(h_a-2) - \left(\frac{\delta(h_b-2)+\delta(h_c-2)}{2}\right)\right\} + X_{qC3} \tag{20.3}$$

$$X_{dC2} = \frac{\delta(h_b-2)-\delta(h_c-2)}{3\sqrt{3}} + X_{dC3} \tag{20.4}$$

$$X_{qC1} = \frac{2}{3}\left\{\delta(h_a-1) - \left(\frac{\delta(h_b-1)+\delta(h_c-1)}{2}\right)\right\} + X_{qC2} \tag{20.5}$$

$$X_{dC1} = \frac{\delta(h_b-1)-\delta(h_c-1)}{3\sqrt{3}} + X_{dC2}. \tag{20.6}$$

Despite the formidable appearance of their constituent terms, the X-vectors reduce to a set of very regular vectors in the $dq0$ plane. For example, the X-vectors for all S_{10} states using the lowermost capacitor C_1 are shown in Fig. 5. Characteristic of all X-vectors is the fact that either they are zero magnitude or have a constant amplitude and are spaced at 60° intervals in the $dq0$ plane. Similarly, X vectors for an S_{21} and an S_{31} states are shown in Fig. 6. Therefore, now using (16), (20.1)–(20.6) one can generate a graphical representation of voltage balancing. For example, returning to the example wherein the reference

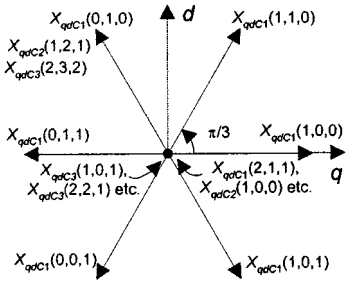

Fig. 5. X-vectors for S_{10} states.

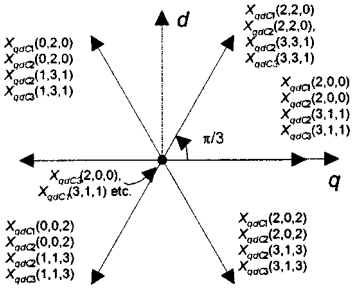

Fig. 6. X vectors for S_{20} and S_{31} states.

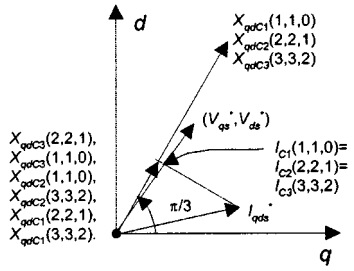

Fig. 7. Voltage balancing using X-vectors for S_{10} states.

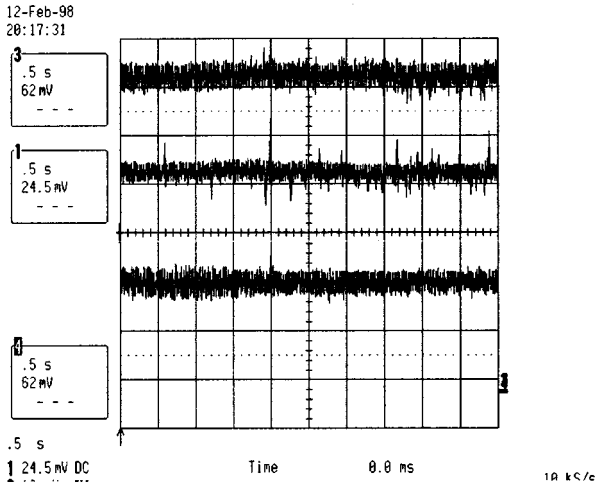

Fig. 8. Voltage balancing using X-vectors for S_{21} states.

voltage vector required is $(V_{dc}/9, V_{dc}/3\sqrt{3})$, the possible switching states are (1,1,0), (2,2,1) and (3,3,2). Hence

$$\begin{aligned} P(1,1,0) &= \Delta v_{C1} i_{C1}(1,1,0) \\ &= 1.5\Delta v_{C1}\ \mathrm{Re}\{\overline{X}_{qdC1}(1,1,0)\overline{I}^{*}_{qds}\} \quad (21.1) \\ P(2,2,0) &= \Delta v_{C2} i_{C2}(2,2,1) \\ &= 1.5\Delta v_{C2}\ \mathrm{Re}\{\overline{X}_{qdC2}(2,2,1)\overline{I}^{*}_{qds}\} \quad (21.2) \\ P(3,3,2) &= \Delta v_{C3} i_{C3}(3,3,2) \\ &= 1.5\Delta v_{C3}\ \mathrm{Re}\{\overline{X}_{qdC3}(3,3,2)\overline{I}^{*}_{qds}\}. \quad (21.3) \end{aligned}$$

If the voltage deviation are given by: $\Delta v_{C2} < 0$, $\Delta v_{C1} > \Delta v_{C3} > 0$ and $|\Delta v_{C2}| > |\Delta v_{C1}|$, the ideal balancing condition requires either $P(1,1,0) < 0, P(2,2,1) > 0$, or $P(3,3,2) < 0$. Hence as depicted in Fig. 7(a) and (b), it can be seen that permissible orientations of the current vector and the X vectors in order to determine the suitability of the switching state in balancing capacitor voltages. Here, since $\overline{X}_{qdC1}(1,1,0) = X_{qdC2}(2,2,1) = \overline{X}_{qdC3}(3,3,2)$, the projection of the load current vector on the X-vector is positive and so the switching state to be selected is (2,2,1) since $\mathrm{Re}\{\overline{X}_{qdC2}(2,2,1)\overline{I}^{*}_{qds}\} > 0$.

Consider the case when the voltage vector reference required is $(V_{dc}/9, V_{dc}/3\sqrt{3})$; this vector can be realized by using the switching states (0,1,2) and (1,2,3) and hence

$$\begin{aligned} P(0,1,2) = \max\{&\Delta v_{C1}\ \mathrm{Re}\lfloor \overline{X}_{qdC1}\overline{I}^{*}_{qds}\rfloor \\ &\Delta v_{C2}\ \mathrm{Re}\lfloor \overline{X}_{qdC2}\overline{I}^{*}_{qds}\rfloor\} \quad (22.1) \\ P(1,2,3) = \max\{&\Delta v_{C2}\ \mathrm{Re}\lfloor \overline{X}_{qdC2}\overline{I}^{*}_{qds}\rfloor \\ &\Delta v_{C3}\ \mathrm{Re}\lfloor \overline{X}_{qdC3}\overline{I}^{*}_{qds}\rfloor\}. \quad (22.2) \end{aligned}$$

Fig. 8 shows the projection of the current vector on the X-vectors of switching states (0,1,2) and (1,2,3). Since $P(0,1,2) > 0$ and $P(1,2,3) > 0$, state (0,1,2) is selected since $I_{C1}(0,1,2) < I_{C3}(1,2,3)$ and $\Delta V_{C1} > \Delta V_{C3} > 0$. To summarize, the X-vectors represent the axes along which the projection of the load current yields the capacitor current. For the same load current and voltage vector, depending on the switching state selected, the resulting capacitor currents are different—a fact illustrated by the different orientations of the X-vectors for states (1,1,0), (2,2,1) and (3,3,2). The X-vectors for the two level inverter are coincident with the X-vectors for the S_{10} states. Physically, the X-vectors provide a measure of the real power that is flowing out of the dc capacitors.

IV. Verification of Link Voltage Balancing Strategy

In the previous two sections, a theoretical framework of redundant state selection for dc capacitor voltage balancing was described. The proposed scheme has been verified both by simulation studies as well as a hardware implementation of a four-level inverter drive. Simulation studies were carried out using the Advanced Continuous Simulation Language tool in order to identify the behavioral characteristics of the control strategy outlined and determine any limitations or constraints imposed by voltage balancing.

Fig. 9 shows the drive system that has been simulated to verify the theory developed. In [14], a similar topology was discussed

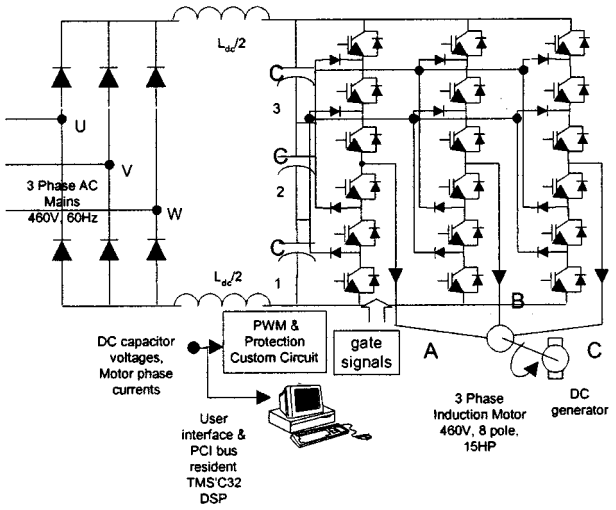

Fig. 9. Drive topology.

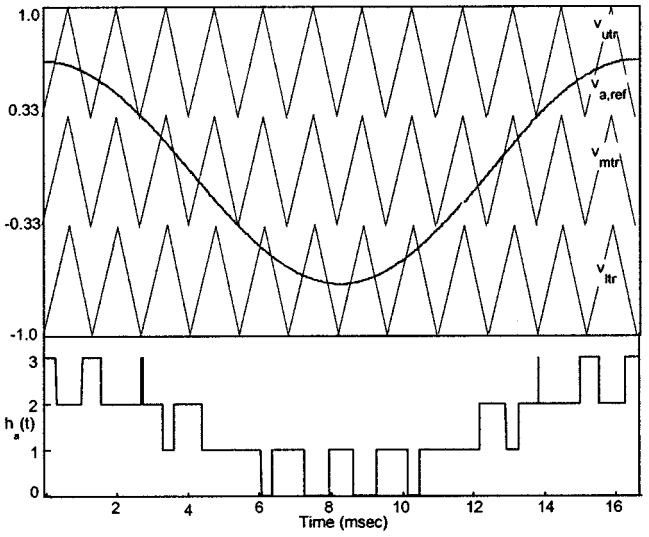

Fig. 10. Four-level sine triangle PWM.

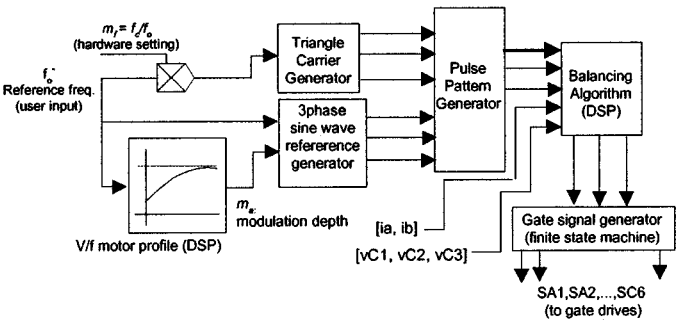

Fig. 11. Control block diagram of drive.

but only R-L loads were considered. In this system configuration, a dc filter inductance is added to stiffen the dc bus. The motor is operated under an open loop constant V/Hz control scheme. This determines the voltage reference command of the inverter as a function of the reference frequency. The phase switching functions were derived from a sine triangle PWM scheme based on the multilevel sine triangle PWM scheme first

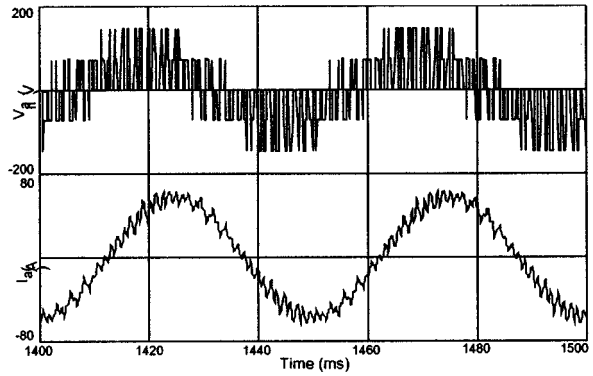

Fig. 12. Simulated plots of motor phase voltage and currents for low speed operation (273 RPM).

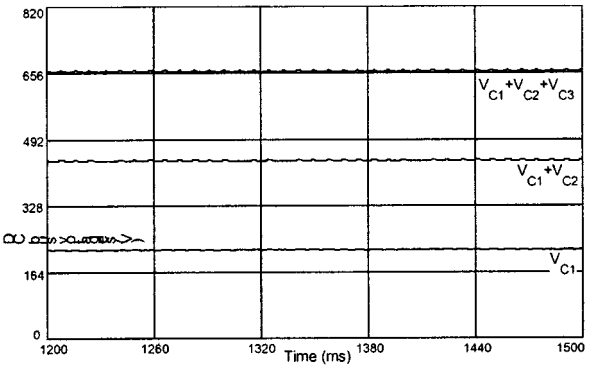

Fig. 13. DC link voltages for low speed operation.

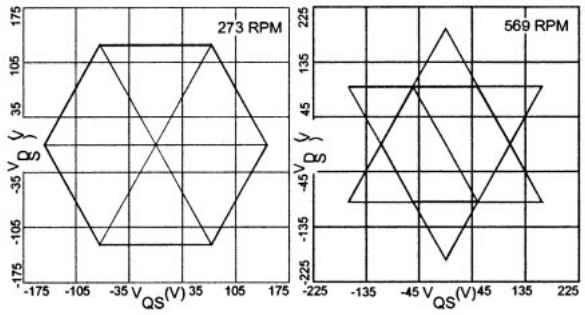

Fig. 14. q and d axis voltages for 20 and 40 Hz operation.

proposed in [13]. Fig. 10 shows the disposition of the triangle carrier waves and the reference phase sinusoid. This scheme produces at its output the three phase switching functions according to:

$$\begin{aligned} h_a &= 3, \quad \text{if } v_{a,ref} \geq v_{utr} \\ h_a &= 2, \quad \text{if } v_{utr} \geq v_{a,ref} \geq v_{mtr} \\ h_a &= 1, \quad \text{if } v_{mtr} \geq v_{a,ref} \geq v_{ltr} \\ h_a &= 2, \quad \text{otherwise.} \end{aligned} \tag{23}$$

Switching functions for the other phases are determined similarly. This switching pattern is the input to the voltage balancing control block. If current regulation or field orientation schemes are implemented, the equivalent voltage reference commands must be converted to phase switching functions according to (12), (13). The overall control scheme for the drive is shown in Fig. 11. The link voltage balancing block implements the redundant state selection based on the principles outlined earlier.

Fig. 12 shows the motor phase voltage and current for a low speed operation case. For a low carrier frequency of 420 Hz, the current THD is about 11%. At low modulation indices, vectors with higher redundancies are selected i.e. only S_{10} states are being used, hence the link voltages are balanced as is shown in Fig. 13. Fig. 14 shows the motor q and d axis voltage in the stationary reference frame when the synchronous frequency is 20 Hz and 40 Hz. As the modulation depth is increased, S_{10} and S_{21} states are selected as shown in Fig. 14(b). For a fixed 'gear ratio,' as the synchronous frequency increases at constant V/Hz the current THD improves significantly because the motor leakage reactance is better able to filter the currents. This results in reduced phase current THD (4.4%) at the rated point of the motor as shown in Fig. 15. It was found that unconditional stability could be guaranteed by simulation studies to $m_a < 0.67$. This is because voltage vectors with redundant states cannot be selected often enough in order to redistribute the charges. Further, the link voltage balancing capability diminishes rapidly with increasing power factors.

The laboratory prototype of the four-level inverter is implemented using 1200 V, 100 A IGBT's. The load is a 15HP, 460-V, 8-pole induction motor. The motor is loaded by a 10HP dc generator with separate field excitation. Numerous design and implementation details are involved in the design of the drive and will be discussed in future publications. Four-level sine triangle PWM was implemented using custom hybrid circuitry and a Texas Instruments TMS320C32 based floating point DSP resident on a PCI bus on a computer formed the control engine of the drive. Capacitor voltages are sensed using differential amplifiers and special design effort was directed at reducing the noise in the voltage and current measurement.

Fig. 16 shows the motor phase voltage, inverter pole voltage, motor phase current and the line-line voltage at a low modulation depth and frequency of operation (450 RPM). The load current spectrum is traced in Fig. 17 and the typical THD's recorded were in the order of 2–4%. All results used a constant carrier frequency of 1.4 kHz. At this carrier frequency, the device switching frequencies were in the range of 300–700 Hz depending on the device location. This is an attractive feature of the four-level inverter as the switching losses can kept low.

In Fig. 18 the balanced dc link voltages are traced for a typical operating point. The robustness of the algorithm is illustrated in Fig. 19 which shows the initial capacitor voltages to be unequal i.e. $V_{C1} \approx V_{C2} = 2V_{C3}$. As soon as the link voltage balancing starts to act, the capacitor voltages are driven toward their nominal values. Thus, the proposed balancing scheme is capable of fundamentally redistributing charges amongst the dc capacitors. Fig. 20 shows the important waveforms at the rated operating point of the motor at $m_a = 0.6$ and V_{dc} adjusted to produce the rated line voltage.

The proposed strategy starts to fail at $m_a > 0.6$ instead of 0.67 and this can be attributed to the following factors (i) As the voltage balancing strategy is dependent on the current and voltage magnitude, incorrect balancing decisions are made as a result of the noise corruption of sensed currents. (ii) During

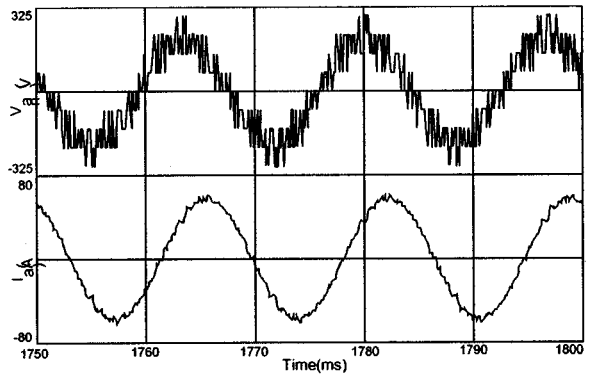

Fig. 15. Waveforms at rated operating point.

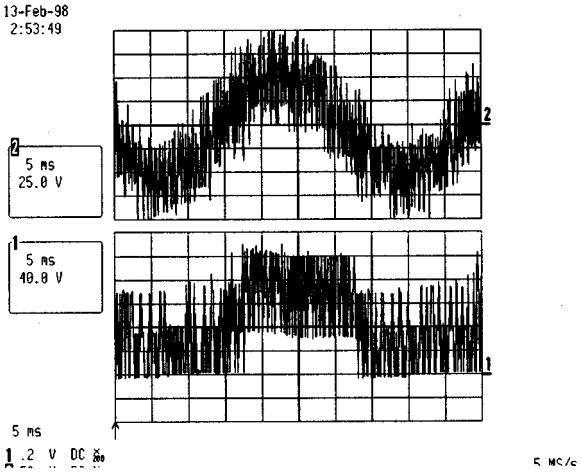

Fig. 16. Experimental waveforms at 450RPM operation. (a) Current (5 A/div) (b) Line voltage (50 V/div).

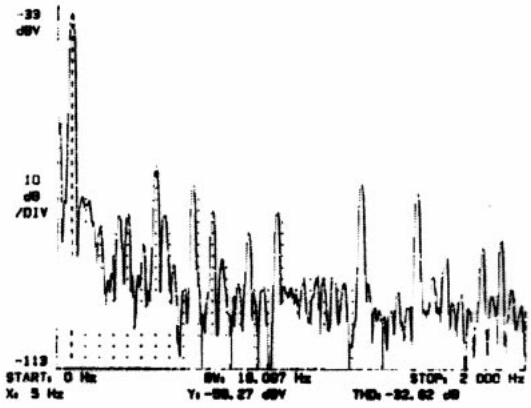

Fig. 17. Current spectrum at rated point of induction motor.

the transition from one voltage vector to another, the inverter has to dwell on one or more intermediate switching states. Depending on the blanking time, load current power factors and gate switching sequence, unequal charges are pumped into or withdrawn from the capacitors—this exacerbates the link voltage unbalance even at low m_a. The latter effect is confirmed by the fact that on increasing the triangle carrier frequency, the modulation depth at which voltage balancing cannot be effected does not change appreciably. At high m_a, an

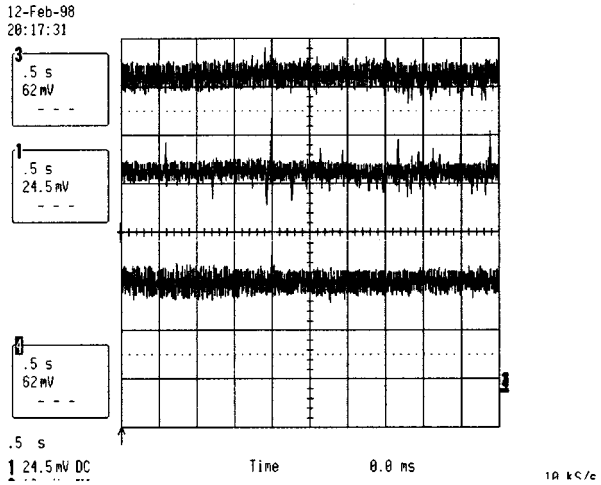

Fig. 18. Balanced dc link voltages in steady state.

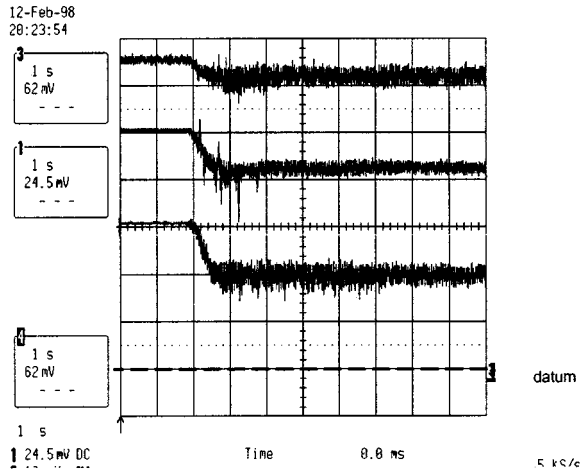

Fig. 19. Dynamic restoration of link voltages using balancing algorithm.

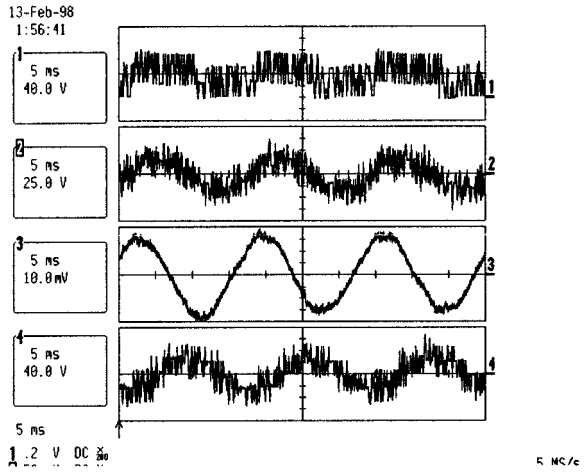

Fig. 20. Waveforms at the rated operating point of the motor. (a) Inverter pole voltage (100 V/div). (b) Motor phase voltage (100 V/div) (c) Motor phase current (5 A/div) (d) Line to line voltage (100 V/div).

alternate modulation strategy has been proposed in [15], which significantly improves the dc bus utilization in the four-level inverter. Dynamic link voltage balancing produces a pattern of

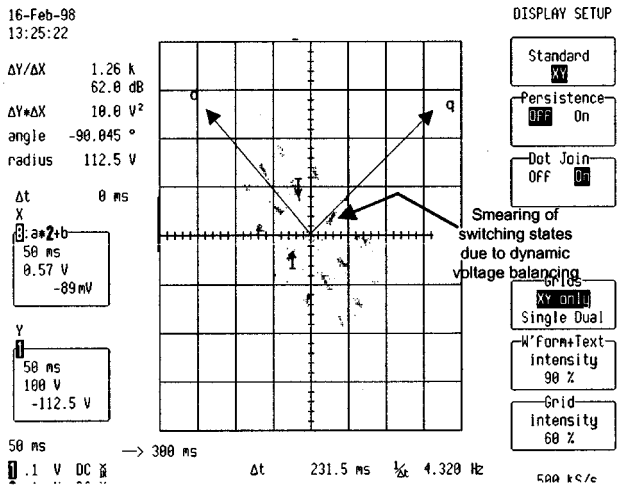

Fig. 21. $V_{ds} vs. V_{qs}$ in the steady state at 60 Hz.

switching states that are dispersed about the nominal values. This can be seen by comparing Fig. 2 with Fig. 21 which shows the voltage vectors actually produced by the inverter. The smearing of voltage vectors is due to the fact that the capacitor voltages are dynamically varying. In fact, the difference in the voltage vectors produced by redundant states (2,1,0) and (3,2,1) can be shown to be

$$\begin{aligned}\Delta\overline{v}_{qds} &= \overline{v}_{qds}(2,1,0) - \overline{v}_{qds}(3,2,1) \\ &= \Delta v_{C3} + j\left(\frac{\Delta v_{C1} - \Delta v_{C2}}{3\sqrt{3}}\right) \end{aligned} \tag{24}$$

Clearly, there is an error in the applied voltages due to unequal capacitor voltages. Thus in any multilevel inverter based control scheme, link voltage balancing may produce additional voltage distortion at the inverter output which can be compensated for by a suitable closed loop voltage control scheme.

V. Conclusion

Four-level inverters based drives with a single diode rectifier front end offer the prospect of reduced total drive kVA's as compared to a drive solution with a fully controllable converter. The basis for redundant state selection for voltage balancing was presented and a new graphical method for visualization of the concurrent link voltage balancing and inverter modulation introduced. It is possible to obtain low current and voltage THD's from the four-level inverter while retaining adequate link voltage balancing capability. This makes such drives suitable for applications wherein low speed operation (at constant V/Hz) is the dominant mode of operation or voltage de-rating is acceptable. Experimental and simulation studies confirm the validity of the control strategy presented and demonstrate the viability of the drive. Though bus utilization is an issue, space vector schemes can partially overcome this limitation and are discussed in another publication.

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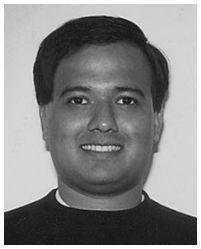

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