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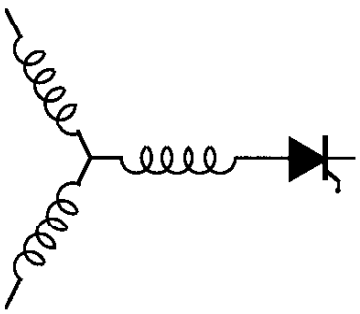

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A New Control Strategy for the PWM Current Stiff Rectifier/Inverter with Resonant Snubbers

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Abstract - In this paper, a three phase current stiff type converter topology employing resonant snubbers with one auxiliary switch is reviewed. A new four quadrant control/modulation scheme is introduced for this topology leading to significant improvement on the utilization of the main devices over previously reported techniques. Voltage and current stresses on the main devices are reduced to the same levels observed in classical snubber topologies. Another benefit is the reduction of the ratings of the resonant snubber inductance and auxiliary device. Simulation results are included to illustrate the improvement introduced with the proposed control scheme.

I. Introduction

Current Stiff (CS) type converters are usually employed in high power drive systems (hundreds of kW and MW range) at medium voltage levels. These converters possess sustained regeneration capability and improved overall reliability due to the inherent overcurrent and short circuit protection and the unidirectional nature of the devices [1-2]. The absence of electrolytic capacitors also contributes for improved reliability, since these components have been pointed out as the element limiting the number of operating hours in Voltage Stiff type of converters [3-4]. Another feature of the CS converters is their inherent low ac side voltage dv/dt due to its ac side capacitor filters [2]. This is an important characteristic considering the present EMI restrictions at the point of connection with the utility system and also EM compatibility with the load. The main drawbacks of classical PWM CS converters are related to their low switching frequency, limited to the range of a few hundred Hz in conventional GTO based topologies, mainly due to restrictions imposed by the switching power losses [5-6]. As a result, large dc bus inductors as well as large ac side filter capacitors are required (typically in the range of 0.2 to 0.5 pu [7]), increasing converter cost and leading to low input power factor.

Recent advances in high power fast switching devices as the HVIGBT's [8] and the introduction of the MTO's [9] suggest that these devices may become an alternative to the GTO's in the near future. However, at the present stage of development, these devices require the use of snubbers to meet their SOA requirements and switching losses remain an issue limiting the converter switching frequency [9].

An interesting CS converter topology employing resonant snubbers was recently introduced [10]. Its power circuit is depicted in fig.1 for a three phase rectifier. This topology is in fact a minimum realization of the Current Stiff Inverter/Rectifier employing resonant snubbers with auxiliary devices, initially introduced by McMurray [11]. This topology is compatible with PWM and a minimum amount of auxiliary devices are added to the basic converter topology. A serious drawback that arises from the control presented in [10] is that the main converter devices are subjected to voltage stresses in excess of twice the peak line voltage .

In this paper, it is presented a new control strategy for the minimum part count realization of the CS converter topology resonant snubbers with auxiliary devices, where the voltage stress on the main converter devices is shown to be reduced to peak line-to-line voltage. The new proposed control method also leads to reduction in the ratings of the resonant snubber components when compared to the results shown in [10]. A four quadrant space vector modulation strategy that minimizes the total number of switchings per period is presented, also contributing to the reduction of switching losses. Simulation results are included to illustrate the converter operation under this new control scheme.

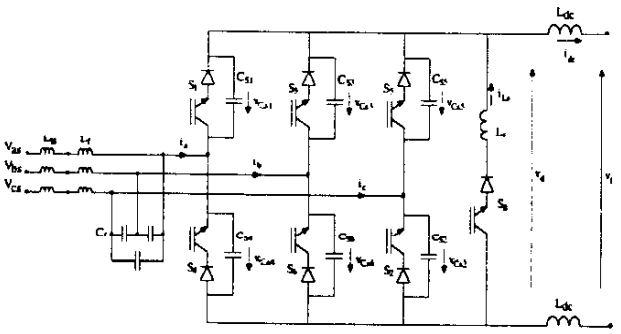

Fig. 1. Current Stiff converter with resonant snubbers. Rectifier front-end.

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II. CONVERTER OPERATION AND CONTROL

A. Commutation sequences

In the operation of the CS converter depicted in fig. 1, two commutation sequences are identified, as pointed out in [10-11]. The first and simplest one makes use only of the snubber capacitors to complete the current commutation process and is referred to in this text as the *passive commutation sequence*. Whenever the auxiliary active switch is turned on to assist the current commutation process, an *active commutation sequence* takes place.

Passive commutation occurs whenever the incoming device is reversed biased. As a consequence, when the outgoing device is turned off the incoming device does not enter conduction immediately. The dc bus current flows through the snubber capacitors of the device group undergoing commutation, driving the voltages across those capacitors in the positive direction (forward bias). The incoming switch starts conducting (turns on) when the voltage across it crosses zero. Fig. 2 illustrates the passive commutation process, from device pair $\{S_1,S_2\}$ to $\{S_1,S_6\}$. It is assumed $v_a>v_b>v_c$.

If the basic condition for the passive commutation to take place is not met (incoming switch is not reverse biased), an active means to discharge the snubber capacitor connected to the incoming device(s) is provided to achieve zero voltage turn-on. It basically consists in charge transfer through a resonant mode introduced by switching in the snubber inductor L_s. In reference [10] it was proposed to achieve the required conditions to perform the active commutation by turning off all the main devices and allowing the required snubber driving voltage conditions to build up from the dc bus current flowing through the snubber capacitors. As a result, the main devices are subjected to voltage stresses that may exceed twice the peak of the line-to-line ac side voltages. This worst case situation happens when an active commutation from the null current vector takes place.

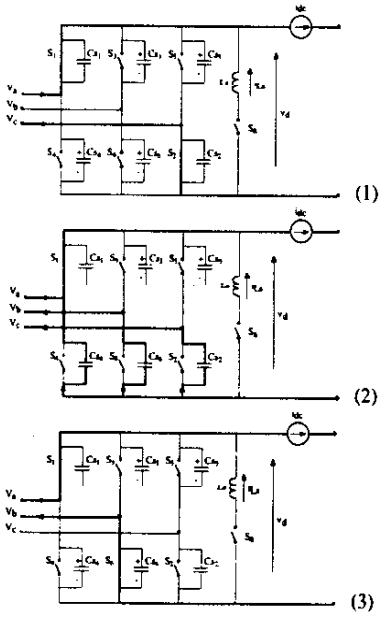

Fig. 2. Passive commutation sequence.

The active commutation sequence presented in this paper introduces a voltage clamping mechanism that limits the voltage across the main devices to the peak amplitude of the line-to-line voltages eliminating any extra voltage stresses. This is accomplished by introduction of an intermediate state of the main converter with devices on in both positive and negative groups during the interval where the required energy levels build up in the snubber components.

Fig. 3 illustrates this operation sequence, where the current commutates from the pair $\{S_1,S_4\}$, current vector $\mathbf{i}_0$, to $\{S_1,S_2\}$, current vector $\mathbf{i}_1$. It is again assumed that $v_a>v_b>v_c$, implying that S_2 is forward biased. From fig. 1, it is seen that the snubber components form the structure of a zero current switch. Necessary condition for the operation of S_a in the zero current switching mode (ZCS) are:

i) $v_d<0$ at turn-on (forward bias);

ii) $v_d>0$ at the end of the commutation interval.

These snubber driving voltage conditions can be established actively through proper control of the main converter devices. Analogous to the result shown in [12], the dc side voltage at any instant is given by the scalar product:

$$v_d = \frac{\mathbf{i}_n}{|\mathbf{i}_n|} \bullet \mathbf{v}_s \qquad (1)$$

where $\mathbf{i}_n$ is one of the converter current vectors and $\mathbf{v}_s$ is the instantaneous terminal voltage vector. The required inversion of v_d is accomplished if, for instance, active current vectors 180° apart are chosen in sequence. For the conditions in fig.3, the requirements for the ZCS turn-off of S_a imply that $\mathbf{i}_1 \bullet \mathbf{v}_s > 0$. Since $\mathbf{i}_1 = -\mathbf{i}_4$, then $\mathbf{i}_4 \bullet \mathbf{v}_s < 0$ and the turn-on condition is met if the vector $\mathbf{i}_4$ is introduced in the active commutation mode sequence.

The active commutation modes in fig. 3 are:

Mode 1 ($t<t_0$): initial condition with the device pair $\{S_1,S_4\}$ conducting; $v_d = 0$.

Mode 2 ($t_0\le t<t_1$): at $t=t_0$ a passive commutation from S_1 to S_5 starts by turning off S_1. S_5 is simultaneously turned on but does not enters conduction. Current commutates from S_1 to the positive group snubber capacitors. During this mode, the snubber voltages distribution is given by:

$$v_{Csn}(t-t_0) = v_{Csn}(t_0) + \frac{i_{dc}}{C_{eq}}(t-t_0), \quad \text{for } n=1,3,5.$$

$$v_{Csn}(t-t_0) = v_{Csn}(t_0), \quad \text{for } n=4,6,2. \qquad (2)$$

$$v_d(t-t_0) = v_d(t_0) - \frac{i_{dc}}{C_{eq}}(t-t_0) \qquad (3)$$

with $C_{eq} = 3C_{sn}$.

Mode 3 ($t_1 \le t < t_2$): at $t=t_1$ the S_5 enters conduction under zero voltage. The switch pair $\{S_5,S_4\}$ conducts, clamping the voltages across the other devices to the ac line voltage levels. This mode leads to $v_d < 0$ and S_a is forward biased.

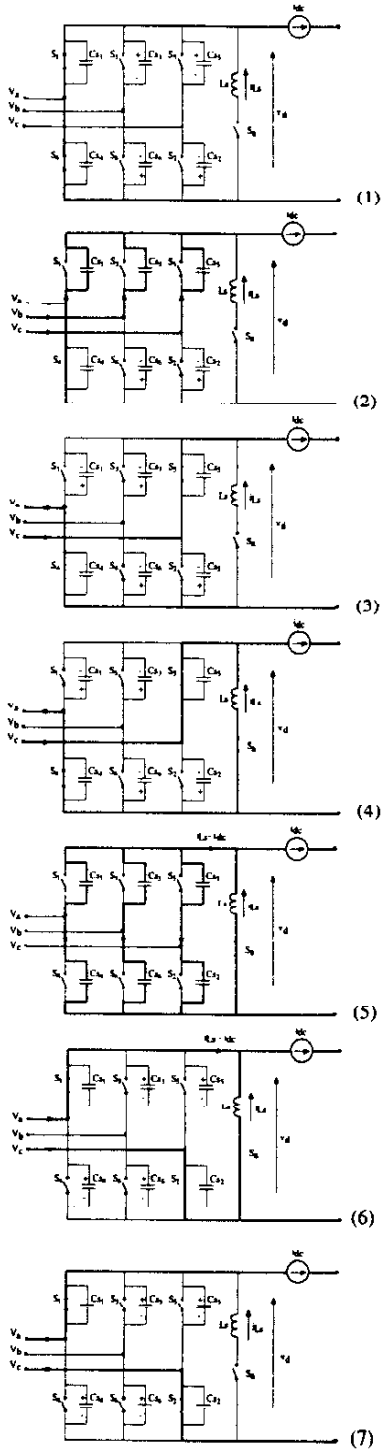

Fig. 3. Active commutation sequence.

Mode 4 ($t_2 \le t < t_3$): at $t=t_2$, the snubber device S_a is turned on. The current through the snubber inductance, i_{Ls}, ramps up driven by the voltage v_d. The line currents ramp down.

Mode 5 ($t_3 \le t < t_4$): at $t=t_3$, the snubber inductor current, i_{Ls}, reaches an amplitude equal to i_{dc}. The main conducting devices turn-off under zero current condition. Since none of the main devices is on, a null current vector is applied at the ac terminals. With all the main devices off, a resonant mode takes place. During this mode, the voltages across the incoming devices are driven down towards zero. The relevant snubber quantities are given by (assuming no losses and ideal devices):

$$v_{Csn}(t-t_3) = v_{Csn}(t_3) - \frac{v_d(t-t_3)-v_d(t_3)}{2} \quad (4)$$

$$v_d(t-t_3) = v_d(t_3)\cos\omega_o(t-t_3) \quad (5)$$

$$i_{Ls}(t-t_3) = \frac{v_d(t_3)}{Z_o}\sin\omega_o(t-t_3) + i_{dc} \quad (6)$$

where: $\omega_o = 1/\sqrt{L_s C_{eq}}$, $Z_o = \sqrt{L_s/C_{eq}}$ and $C_{eq} = 3C_r/2$.

Mode 6 ($t_4 \le t < t_5$): at t_4 the voltage across the incoming devices $\{S_1,S_2\}$ is minimum and turn on takes place under nearly or at zero voltage conditions. At this point $v_d > 0$ and i_{Ls} ramps down.

Mode 7 ($t \ge t_5$): at $t=t_5$, i_{Ls} reaches zero and S_a turns off under zero current condition. The current vector $\mathbf{i}_1$ is applied at the ac terminals and the commutation process is finished.

B. Effect of losses in the commutation processes

The passive commutation sequence utilizes the dc bus current to establish the required charge distribution in the snubber capacitors from a given initial condition. Since the energy stored in the dc bus inductor greatly exceeds the energy required for the changes in the snubber state, the effect of losses in the passive commutation sequence are negligible. The active commutation sequence, on the other hand, circulates the energy stored in the resonant snubber elements (modes 4 and 5). The effects of losses are significantly more important and must be evaluated.

The losses during mode 5 in the active commutation sequence are mainly associated with the snubber inductance ESR and the snubber device conduction losses. These terms can be modeled as an equivalent dc voltage source (v_{loss}) in series with an equivalent resistance (r_{loss}) in the snubber inductor branch.

Another non-ideal situation that must be included in this analysis is the reverse recovery current in the main devices, since it leads to deviations in the resonant snubber initial energy state. Since the main devices turn-off under zero current conditions at the end of mode 4, their reverse recovery current circulates through L_s. Hence, $i_{Ls}(t_3) = i_{dc} + i_{rr}$.

Under these conditions, the snubber capacitor voltages during mode 5 are given by:

$$v_{Csn}(t-t_3) = v_{Csn}(t_3) - \frac{v_d(t-t_3)-v_d(t_3)}{2} \quad (7)$$

$$v_d(t-t_3) = e^{-\frac{r_{loss}}{2L_s}(t-t_3)} \left\{ \left(v_d(t_3) - v_{loss} - r_{loss} i_{dc}\right)\cos\omega_d(t-t_3) + \right.$$
$$+\frac{1}{Z_d}\left[\frac{r_{loss}}{2}\left(v_d(t_3) - v_{loss} - r_{loss} i_{dc}\right) - \right.$$
$$\left. \left. - Z_o^2\left(i_{Ls}(t_3) - i_{dc}\right) \right] \sin\omega_d(t-t_3) \right\} + v_{loss} + r_{loss} i_{dc} \quad (8)$$

where: $\omega_d = \sqrt{1/(L_s C_{eq}) - r_{loss}^2/(4L_s^2)}$; $Z_d = \sqrt{(L_s/C_{eq}) - r_{loss}^2/4}$.

Notice from (6) that the increase in initial current through L_s due to the reverse recovery process in the main devices compensates the loss related terms. Zero voltage switching conditions can be guaranteed if minimum reverse recovery current requirements are fulfilled. In any case, significant reverse recovery current is present in high power devices and the detrimental effects of the circuit losses on the active commutation sequence are always reduced.

III. Space Vector Modulation

In this discussion of PWM strategies suitable for the Current Stiff converter with resonant snubbers, consider initially the vector diagram shown in fig. 4, where i_s^* is the commanded line current vector and v_s is the ac terminal voltage vector. High power factor operation is shown since this is a desired condition for the rectifier operation. The conditions in fig. 4 with $0 \le \theta \le \pi/3$, imply that the type of commutation associated with the positive and negative devices group of the converter is given by:

Positive group: $S_1 \xrightarrow{p} S_3 \xrightarrow{p} S_5 \xrightarrow{a} S_1 \ldots$

Negative group: $S_4 \xrightarrow{a} S_6 \xrightarrow{a} S_2 \xrightarrow{p} S_4 \ldots$

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where $\xrightarrow{p}$ and $\xrightarrow{a}$ represent passive and active commutation sequences, respectively.

The switching sequence above can be promptly generalized for any position of v_s in the complex plane. It is also straightforward to prove that the commutation type changes if the switching occurs in the direction opposite to the one indicated by the arrows.

It was shown in the previous section that the active commutation sequence implies the introduction of a non-adjacent vector in the switching pattern. Hence, the occurrence of active commutations has to be minimized in order to obtain minimum ripple current at the ac terminals. From the commutation description above it is seen that the total number of active commutations can be reduced to one if the positive and negative groups are synchronized. Under these conditions, a suitable switching pattern corresponds to:

Positive group: $S_1 \xrightarrow{p} S_5 \xrightarrow{a} S_1 \quad S_1 \quad S_1 \ldots$

Negative group: $S_4 \quad S_4 \xrightarrow{a} S_2 \xrightarrow{p} S_6 \xrightarrow{p} S_4 \ldots$

Current vector: $i_0 \xrightarrow{p} i_4 \xrightarrow{a} i_1 \xrightarrow{p} i_6 \xrightarrow{p} i_0 \ldots$

Notice in the switching pattern above that vector i_4 does not contribute to the synthesis of i_s^*; it is introduced only as part of the active commutation process. Extending the interval of injection of i_1, by the duration of the interval of injection of i_4 compensates for the effect of i_4 on the ac currents. This compensation scheme implies the introduction of a null average vector in the ac terminals, limiting the maximum modulation depth and dc bus current utilization. Hence, the interval of application of i_4 must be kept as short as possible. No additional constraints are introduced, since the commutation intervals correspond to a small fraction of the switching period. Another important observation is the fact that S_1 conducts for the entire interval, except for duration of the active commutation interval. In general, one device remains conducting for the entire length of any $\pi/3$ interval, characterizing this modulation scheme as a discontinuous PWM.

The switching pattern described above also leads to minimum variation of the snubber driving voltage (v_d) during mode 3, constraining it to the range $0.866\,|v_s| \le v_d \le |v_s|$. This characteristic leads to significant simplification in the design of the snubber inductor L_s and also to a fairly constant di/dt during the zero current turn-off of the main devices at the end of mode 3. This last characteristics contributes to a certain degree of control over the reverse recovery/snubber loss compensation process as discussed in the previous section.

A general modulation scheme can be derived from the example presented above. In order to derive the mappings

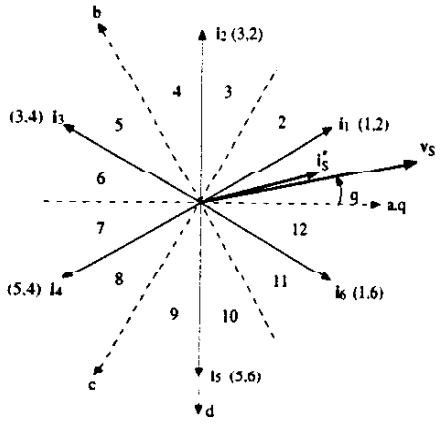

Fig. 4. Near unity power factor operation.

between the vectors $\mathbf{i}_s^*$ and $\mathbf{v}_s$ and the converter switching patterns, the complex plane containing the converter current vectors is divided in 12 sectors, as shown in fig. 4, each with a span angle of $\pi/6$. It can be shown that the instantaneous location of the terminal voltage vector, $\mathbf{v}_s$, and the commanded current vector, $\mathbf{i}_s^*$, completely define a suitable switching pattern. The mapping of the positions of $\mathbf{i}_s^*$ and $\mathbf{v}_s$ into the set of switching patterns is shown in Tables I to III, covering the converter operation as rectifier, inverter and reactive power source/load. Combined use of these three switching maps allows full four quadrant operation. These maps can also be used individually or in combinations of two, according to the application requirements. It is important to indicate here that the rectifier and inverter switching maps allow operation with displacement power factor angles in the range $-\pi/6 \le \phi \le \pi/6$. The combined used of these two switching maps is adequate for a wide range of applications including the rectifier front end in CSI drives.

Computation of the time intervals within the switching period associated with each of the current vectors involved in the modulation process is performed by direct application of the space vector modulation strategy [13]. General expressions for the modulation intervals derived for Current Stiff converters are given by:

$$t_m = T/i_{dc}\,(-i_{qs}^* \sin\theta_n - i_{ds}^* \cos\theta_n)]$$

$$t_n = T/i_{dc}\,(i_{qs}^* \sin\theta_m + i_{ds}^* \cos\theta_m)] \qquad (9)$$

where t_m and t_n are the injection intervals of the non-null current vectors $\mathbf{i}_m$ and $\mathbf{i}_n$, respectively, and $\mathbf{i}_m$ leads $\mathbf{i}_n$ by $\pi/3$; i_{qs}^* and i_{ds}^* are the components of $\mathbf{i}_s^*$ in the stationary reference frame shown in fig.4. The modulation depth is implicit in the ratios i_{qs}^*/i_{dc} and i_{ds}^*/i_{dc}.

The switching maps shown here can be implemented in hardware using programmable logic devices for minimum overhead. The required inputs are position of the vectors $\mathbf{i}_s^*$ and $\mathbf{v}_s$ in the complex plane (sector) and the timing signals from the space vector modulation computations, including the timing of the active commutation process.

TABLE I – Rectifier Mode.

$\mathbf{i}_s^*$ sector	$\mathbf{v}_s$ sector	
1,12	1,2	$\mathbf{i}_0 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_0$
2,3	1,2	$\mathbf{i}_0 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_0$
2,3	3,4	$\mathbf{i}_0 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_0$
4,5	3,4	$\mathbf{i}_0 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_0$
4,5	5,6	$\mathbf{i}_0 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_0$
6,7	5,6	$\mathbf{i}_0 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_0$
6,7	7,8	$\mathbf{i}_0 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_0$
8,9	7,8	$\mathbf{i}_0 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_0$
8,9	9,10	$\mathbf{i}_0 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_0$
10,11	9,10	$\mathbf{i}_0 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_0$
10,11	11,12	$\mathbf{i}_0 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_0$
1,12	11,12	$\mathbf{i}_0 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_0$

TABLE II – Inverter Mode.

$\mathbf{i}_s^*$ sector	$\mathbf{v}_s$ sector	
6,7	1,2	$\mathbf{i}_4 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_4$
8,9	1,2	$\mathbf{i}_4 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_4$
8,9	3,4	$\mathbf{i}_5 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_5$
10,11	3,4	$\mathbf{i}_5 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_5$
10,11	5,6	$\mathbf{i}_6 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_6$
1,12	5,6	$\mathbf{i}_6 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_6$
1,12	7,8	$\mathbf{i}_1 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_1$
2,3	7,8	$\mathbf{i}_1 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_1$
2,3	9,10	$\mathbf{i}_2 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_2$
4,5	9,10	$\mathbf{i}_2 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_2$
4,5	11,12	$\mathbf{i}_3 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_3$
6,7	11,12	$\mathbf{i}_3 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_3$

TABLE III – Reactive Power Mode.

$\mathbf{i}_s^*$ sector	$\mathbf{v}_s$ sector	
4,5	1,2	$\mathbf{i}_3 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_3$
10,11	1,2	$\mathbf{i}_5 \rightarrow (\mathbf{i}_4) \xrightarrow{a} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_5$
6,7	3,4	$\mathbf{i}_4 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_4$
1,12	3,4	$\mathbf{i}_6 \rightarrow (\mathbf{i}_5) \xrightarrow{a} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_6$
8,9	5,6	$\mathbf{i}_5 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_5$
2,3	5,6	$\mathbf{i}_1 \rightarrow (\mathbf{i}_6) \xrightarrow{a} \mathbf{i}_2 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_1$
10,11	7,8	$\mathbf{i}_6 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_6$
4,5	7,8	$\mathbf{i}_2 \rightarrow (\mathbf{i}_1) \xrightarrow{a} \mathbf{i}_3 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_2$
1,12	9,10	$\mathbf{i}_1 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_1$
6,7	9,10	$\mathbf{i}_3 \rightarrow (\mathbf{i}_2) \xrightarrow{a} \mathbf{i}_4 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_3$
2,3	11,12	$\mathbf{i}_2 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_1 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_2$
8,9	11,12	$\mathbf{i}_4 \rightarrow (\mathbf{i}_3) \xrightarrow{a} \mathbf{i}_5 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_4$

IV. Simulation Results

Simulation results obtained from SABER are presented in this section to illustrate the converter performance under the proposed control and modulation schemes describe in this paper. All results were obtained for the rectifier front end (shown in fig. 1) supplying a resistor load. The operating conditions are given by: $V_S = 2300V_{RMS}$, 60Hz; $|i_s^*| = 120A$, PF = 0.9 lagging. Converter parameters are listed in Table IV. The resonant snubber components were computed such that $dv_{Cs}/dt < 500V/\mu s$ and $i_{Ls,\,max} < 2\, i_{dc}$.

Input filter parameters were obtained from the assumption of a 5% equivalent line inductance, L_{ls}. The base values were chosen as: $V_{base} = 2300V$, $P_{base} = 1.3504\, V_{base}\, i_{dc}$.

Table IV. Converter parameters.

i_{dc}	f_{sw}	L_s	C_s	L_{dc}	L_f	C_f
150A	4kHz	60μH	100nF	10mH	1.5mH .05pu	10μF .1pu

Fig. 5 illustrates the four quadrant operation capability obtained from the control and modulation strategies discussed in the previous section. Effects of the input filter and dc bus current smoothing inductor are neglected in this plot.

Fig. 6 shows a detailed view of the active commutation sequence. Notice that the interval associated with mode 2 has been minimized in order to reduce the total interval associated with the auxiliary current vector.

Figs. 7 and 8 are introduced for a comparison between the proposed control strategy and the one presented in [10], where the relevant wavefoms associated with the active commutation process according to each strategy are shown. Voltage stress on the main devices of about 2 times peak line-to-line voltage seen in fig. 8 (control as in [10]) is completely eliminated in fig. 7 (proposed control method). The peak current through L_s is also significantly reduced (approximately by a factor of 1.5), implying reduction in the cost and size of L_s. The RMS current through the snubber inductor, i_{Ls}, in figs. 7 and 8 corresponds to 52.9A and 73.8A, respectively. This latter result shows that a reduction in the losses on the snubber components by a factor of 1.9 is obtained with the proposed control method, in comparison with the results obtained from [10]. Hence, significant reduction on the main devices and snubber components ratings are achieved with the proposed control strategy.

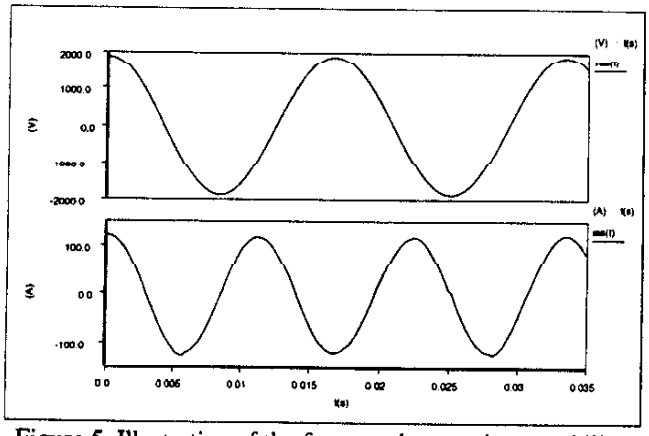

Figure 5. Illustration of the four quad. operation capability.

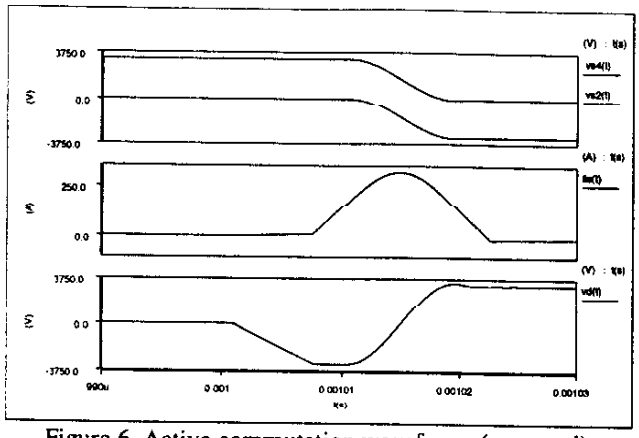

Figure 6. Active commutation waveforms (proposed).

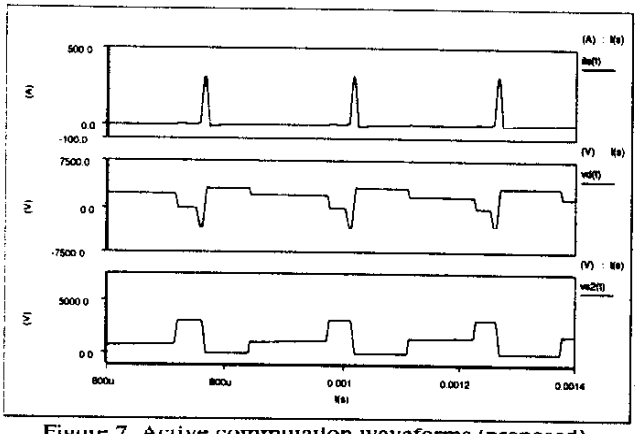

Figure 7. Active commutation waveforms (proposed).

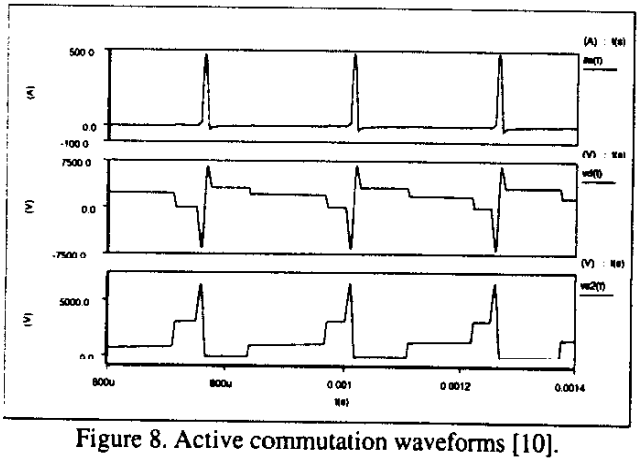

Figure 8. Active commutation waveforms [10].

Fig. 9 shows the input current waveform and frequency spectrum under the specified operating conditions and converter parameters. Low order harmonics present in the input current are due to the operating characteristics of this and other implementations of the resonant snubber in current stiff topologies, and were also pointed out in [10]. Although these harmonics have been related to dwell time in the switching process, they are in fact related to inversions in the switching sequence, following changes in the position of $\mathbf{v}_s$ as it moves in the complex plane. The effects of this non-linearity in the modulation process can be reduced by proper design of the converter parameters. In fig. 9, the amplitude of the 5th harmonic is 3.2% of the fundamental. Further improvement can be obtained with closed-loop current control and/or an accurate model of this modulation non-linearity.

V. Conclusions

Low switching frequency operation, mainly due to the switching losses, has been an important factor preventing improvement in the performance of Current Stiff converters. The introduction of the resonant snubbers with auxiliary devices in those topologies and later simplification with the reduction of the total parts count have been significant steps to overcome this limitation.

In this paper, control and modulation strategies for the operation of the three phase current stiff type converter topologies with resonant snubbers are presented. Significant improvement over previous work presented in the literature has been obtained, with the elimination of the voltage stress over the main converter devices due to the resonant snubber operation as well as reduction of the losses and ratings of the snubber components. In fact, significant overall reduction in device ratings has been obtained by proper control of the active commutation process. A four quadrant operation scheme has been also introduced for this topology. The results presented in this paper point out the CS converter with resonant snubbers as a potential alternative in high power variable speed ac drive applications.

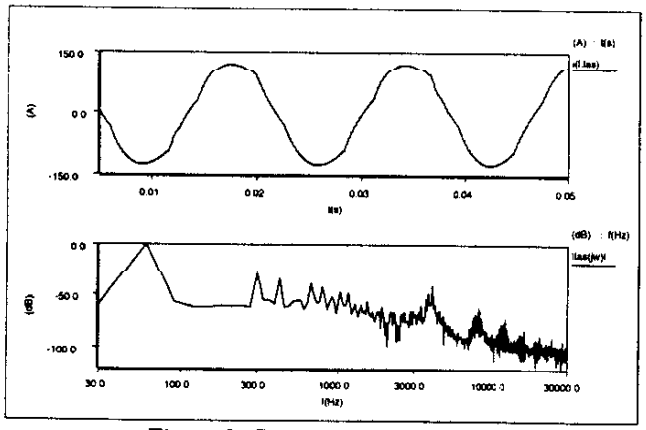

Figure 9. Converter input current.

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