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Current Stiff Converter Topologies with Resonant Snubbers

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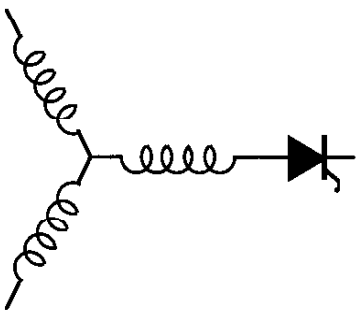

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Current Stiff Converter Topologies with Resonant Snubbers

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Abstract *- In this paper, a study of the resonant snubbers with auxiliary switches is presented as applied to three-phase Current Stiff Converter (CSC) topologies targeted for electric drives applications. Several realizations of CSC's with resonant snubbers are identified and characterized from a generalized three phase commutation cell. The modulation characteristics associated with the operation of the CSC's with resonant snubbers are analyzed using the space vector approach. Simulation results are presented to illustrate the key aspects in this discussion. Experimental results are included for selected cases.*

I. INTRODUCTION

Current Stiff Converters (CSC) are usually employed in high power levels (MW range). Among their features, it can be pointed out the CSC's sustained regeneration capability and improved overall reliability due to their inherent overcurrent and short circuit protection, unidirectional nature of the switches and the absence of electrolytic capacitors [1-3]. CSC's also present inherent low input/output voltage dv/dt, an important characteristic considering the present EMI restrictions and EM compatibility with the load. The main drawbacks of classical PWM CSC's are associated to their low switching frequency, limited to the range of a few hundreds of Hz in conventional GTO based topologies, mainly due to the switching losses [4]. Large ac side filter capacitors are required, typically in the range of 0.2 to 0.5 pu, increasing converter cost and leading to low input power factor. Another drawback of low switching frequency operation is the bulky dc bus inductor required to smooth the dc bus current.

Advances in high power IGBT's (HVIGBT) and new developments in high power devices as the MTO [5] are expected to have a significant impact in high power applications, due to their fast switching characteristics and simplified gate drive requirements when compared to GTO's. Even with those new devices the switching losses are still an issue, specially at turn-off due to the devices tail current. These high power devices also exhibit a non-square SOA, implying the use of snubbers circuits to shape their switching locus.

[1]On leave of absence from the Dept. of Electrical Engineering of the Universidade Federal de Minas Gerais, Brazil. This project is sponsored by CNPq, Brasilia/Brazil and WEMPEC, Madison/WI.

The present technology in snubber circuits employed in CSC topologies is the RCD snubber [6,7]. Among the drawbacks of this snubber configuration, it can be pointed out that: switching losses are transferred to the snubber resistor generating heat that has to be managed; no enhancement of converter efficiency is possible; size of the snubber capacitor is limited; voltage spikes at turn-off and reapplied dv/dt (when snubber diode snaps off) exist due to the series stray inductance, limiting devices and converter utilization.

The application of resonant snubbers to CSC topologies is very promising from the perspective of overcoming these limitations [8,9]. The stray inductance in series with the snubber capacitor can be greatly removed since they be placed very close to the power device. Significantly higher current turn-off and consequently power control capability follows from that. A lossless snubber reset mechanism is provided, allowing larger capacitor snubber and leading to lower SOA requirements and lower turn-off losses (increase in the overall converter efficiency). Reduction in the switching losses can be also understood as extra room for conduction losses (for the same cooling requirements), leading to an increase in the converter power control capability.

In this paper, a study of the resonant snubbers as applied to three-phase Current Stiff converter topologies for high power induction motor drive applications is presented. Several realizations of resonant snubbers in CSC's are identified and characterized from the generalized three phase commutation cell. The PWM characteristics associated with the operation of the CSC's with resonant snubbers are analyzed using the space vector approach. Simulation results are presented to illustrate the relevant aspects of this discussion. Experimental results are included for selected cases.

II. CHARACTERIZATION OF RESONANT SNUBBERS IN CSC'S

The implementation of the resonant snubbers with auxiliary switches [10,11] for both voltage stiff converters (VSC) and CSC is depicted in figs. 1a and 1b, respectively. A comparison between those two topologies shows that they are not strictly duals. The CSC implementation of the resonant snubber is obtained basically by exchanging the dc voltage input

(output) and ac current output (input) in the VSC implementation by an ac voltage input (output) and dc current output (input). Also, the forward voltage blocking, forward/reverse current conducting switches of the VSC are replaced by forward/reverse voltage blocking, forward current conducting switches in the CSC case. The same back-to-back arrangement of snubber devices shown in the VSC implementation can also be used in the CSC with advantages over the realization shown in fig. 1. The influence of the dc bus current amplitude on the commutation processes is minimized (a current boost mode is introduced), but it implies an excessive number of additional devices (12 snubber devices) in comparison with the number of additional devices required by VSC's (6 snubber devices).

Fig. 2 shows the relevant waveforms for the resonant snubber implementation for CSC's. Two commutation sequences are identified in this figure. The *passive commutation sequence* takes place whenever the incoming device is reverse biased. Otherwise, external means have to be provided to create zero voltage conditions on the incoming device during its turn-on process and the *active commutation sequence* takes place.

The passive commutation sequence starts when the conducting device is turned off. The dc bus current commutates to the snubber capacitors and the voltage across the devices ramps up. The incoming device starts conducting at the zero crossing of the voltage across its terminals.

The active commutation sequence implies the introduction of a resonant mode to drive the voltage across the incoming device down to zero. This sequence starts by turning on the snubber device. The current through the snubber inductor ramps up, reaching the dc bus current amplitude. At this instant, the outgoing device is turned off under zero current conditions. Since no device is conducting, a resonant mode between the snubber inductors and capacitors takes place. The charge in the snubber capacitor across the incoming device is transferred to the one across the outgoing device (reverse biased) and the incoming device turns on under zero voltage conditions.

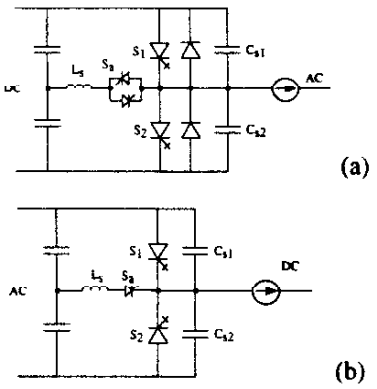

Fig. 1. Resonant snubbers with auxiliary switches.

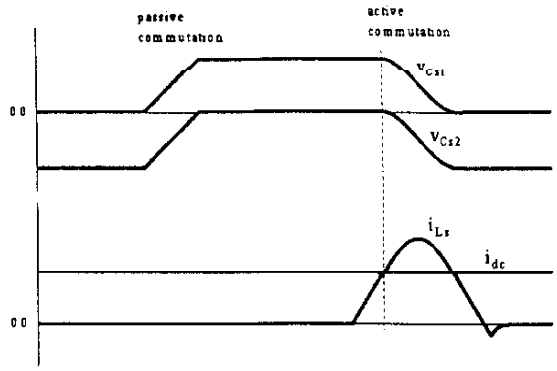

Fig. 2. Resonant snubber waveforms.

The resonant snubber implementation in CSC topologies in fig. 1b can be generalized in the form shown in fig. 3. The positive devices group of the CSC is shown in this figure, as well as one branch formed by the series connection of the snubber device, S_a, and snubber inductor, L_s. This generalization is based on the fact that the snubber driving voltage, v_{sn}, is in fact a control parameter. It is shown later that the three phase implementation from the single phase cell in fig. 1b is but one of several possibilities.

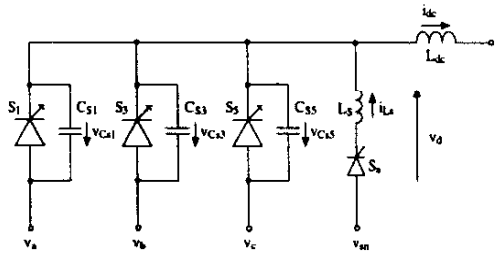

Fig. 3. Generalized CSC with resonant snubbers.

The identification of v_d in fig. 3 as a control parameter turns the focus this discussion to the active commutation sequence. A general description of the active sequence modes associated with the generalized topology in fig.3 is presented below. Without loss of generality, it is assumed that $v_a > v_b > v_c$ with $|v_a| < |v_c|$ and the ac current modulation commands a commutation from S_5 to S_1. All the circuit components are assumed to be lossless. The terminal voltages are assumed to remain constant during the commutation intervals.

Mode 1 ($t<t_1$): base condition with the device S_5 conducting.
Mode 2 ($t_1 \le t < t_2$): at $t=t_2$, the snubber device S_a is turned on. The current through the snubber inductance, i_{Ls}, ramps up driven by the voltage $-v_d = v_{sn}-v_c$ and $i_{Ls}(t_1)=0$. During this mode, the snubber inductor current is given by:

$$i_{Ls}(t-t_1) = \frac{-v_d(t_1)}{L_s}(t-t_1) = \frac{v_{sn}(t_1)-v_c}{L_s}(t-t_1) \qquad (1)$$

Mode 3 ($t_2 \le t < t_3$): at $t=t_2$, the main conducting devices turn-off under either zero current or zero voltage condition with $i_{Ls}(t_2) \ge i_{dc}$ or $i_{Ls}(t_2) < i_{dc}$, respectively. Notice that the condition

$i_{Ls}(t_2) > i_{dc}$ is due to the reverse recovery process in the main devices. Since none of the main devices is on, a null current vector is applied to the ac terminals. With all the main devices off, a resonant mode takes place. During this mode, the voltage across the incoming device is driven down towards zero. The relevant snubber quantities are given by:

$$v_{Cs}(t-t_2) = Z_o\,[i_{dc}-i_{Ls}(t_2)]\,\sin\omega_o(t-t_2) + [-v_d(t_2)]\,\cos\omega_o(t-t_2) + v_d(t_2) + v_{Cs}(t_2) \quad (2)$$

$$i_{Ls}(t-t_2) = \frac{1}{Z_o}\,[-v_d(t_2)]\sin\omega_o(t-t_2) - [i_{dc}-i_{Ls}(t_2)]\cos\omega_o(t-t_2) + i_{dc} \quad (3)$$

where: $\omega_o=1/\sqrt{L_sC_{eq}}$, $Z_o=\sqrt{L_s/C_{eq}}$ and $C_{eq} = 3C_s$.

Mode 4 ($t_3 \le t < t_4$): at t_3 the voltage across the incoming device, S_1, is minimum and turn on takes place under nearly or at zero voltage conditions. The current i_{Ls} ramps down. This mode is analogous to Mode 2.

Mode 5 ($t \ge t_4$): at $t=t_4$, i_{Ls} reaches zero and S_a turns off under zero current condition.

Eq. (2) above can be used to obtain the voltage across any of the main devices by plugging in the respective initial snubber capacitor voltage, $v_{Cs}(t_2)$. From (2), it can be shown that a sufficient condition for zero voltage switching of any incoming device in the positive group is obtained if:

$$-v_d(t_2) \ge \frac{v_{Cs}(t_2)}{2} \quad (4)$$

It is important to notice however that if the voltage across the incoming device (in this example, S_1) increases from its initial value or assumes negative values, the voltage stress on the main devices becomes larger than the standard voltage stress in CSC's, given by the instantaneous line to line voltages. From (4) and recognizing that in this example the relationship $-v_d = v_{sn} - v_c$ holds, the snubber driving voltage, v_{sn}, required to obtain zero voltage switching conditions is given by:

$$v_{sn} \ge \frac{v_a + v_c}{2} \quad (5)$$

The conditions expressed by equations (4) and (5) can be promptly generalized by recognizing v_a and v_c as the phase voltages associated with the incoming and outgoing devices, respectively. The voltage $v_{Cs}(.)$ refers to the voltage across any snubber capacitor in fig. 3. Similar analysis can be performed for the negative group of devices. In this latter case, the inequality sign in (5) must be reversed.

Equation (5) defines a sufficient condition for the turn-on of the incoming device under zero voltage, regardless of the amplitude of $i_{Ls}(t_2)$ with respect to i_{dc}. Fig. 4 show phase plane plots of the snubber quantities during the resonant mode for $i_{Ls}(t_2) = 0$, $i_{Ls}(t_2) = i_{dc}$ and $i_{Ls}(t_2) = i_{dc} + i_{rr}$ ($i_{rr}>0$ is the reverse recovery current through the main devices). In all plots, $v_{sn}=(v_a + v_c)/2$. It is seen that minimum ratings for the snubber components are obtained for $i_{Ls}(t_2) = i_{dc}$. This latter condition also leads to minimum voltage stress on the main converter devices. From the perspective of minimum snubber components ratings and zero voltage stress on the main devices, the situation where $v_{sn}=(v_a + v_c)/2$ and $i_{Ls}(t_2) = i_{dc}$ corresponds to an *optimal active commutation condition*.

From (1) and (5), the interval required to drive i_{Ls} from zero to i_{dc} (Mode 2) is given by:

$$t_2-t_1 = \frac{2\,L_s\,i_{dc}}{v_a - v_c} \quad (6)$$

From (6), it is seen that the condition $i_{Ls}(t_2) = i_{dc}$ introduces a dwell time that is an inverse function of the difference between the phase voltages associated with the devices undergoing commutation. This dwell time becomes excessive long as this voltage difference diminishes due to operation at variable ac voltage levels (variable speed ac drive applications) or due to commutation occurring close to the zero crossing of the line voltage involved in the process. If the interval t_2-t_1 is limited such that $t_2-t_1 \le \Delta t_{dw}$, then the current through the snubber inductor at the end of Mode 2 is such that $i_{Ls}(t_2) \le i_{dc}$, when the line voltage goes below a certain limit. As discussed in the previous paragraphs, this condition does not affect the operation of the snubber, so long as condition (5) is satisfied. In fact, the limitation of the duration of Mode 2 is an interesting and simple way to overcome the dwell time problems introduced by operation at low ac voltage levels in variable voltage applications without exceeding the voltage rating of the converter devices.

For rated operating conditions, on the other hand, it is desirable to eliminate any additional voltage stress on the devices, implying that optimal or near optimal active commutation conditions should be introduced. From (6) it is seen that in order to constrain the dwell time or maximize i_{Ls} within a certain time interval, the amplitude of the line voltage involved in the active commutation process has to be maximized. This condition can be obtained by restricting the active commutation process to commutations between devices associated with the maximum instantaneous line to line voltage. Although effective, this scheme introduces constraints on the converter compatibility with PWM.

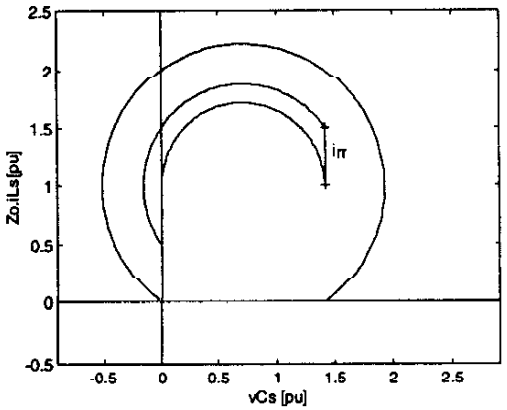

Fig. 4. Active commutation - Mode 3.

III. Three-Phase Realizations

A. Full realization

In practical implementations, the sufficient condition in (4) can be very closely approximated with the topology depicted in fig. 5 [11]. In this topology, the basic snubber structure in fig. 1 is reproduced for each pair of devices potentially undergoing commutation. The total number of snubber inductors is reduced by recognizing that the positive and negative device groups do not undergo commutation simultaneously. The snubber driving voltage condition expressed by (5) is met by means of a series connection of the ac filter capacitors and employing the center tap voltage to drive the snubber inductor/device branch.

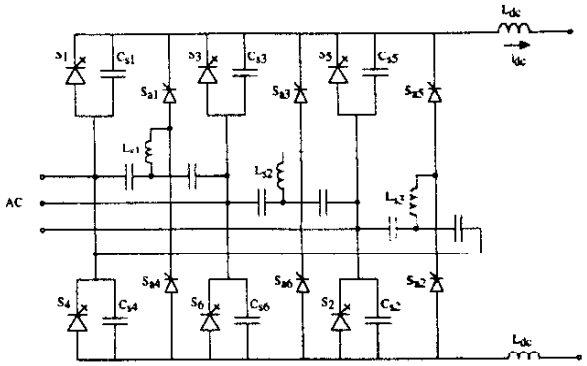

Fig. 5. Full realization of CSC with resonant snubbers.

Although suitable commutation conditions exist for any pair of devices in both positive and negative groups, significant dwell time intervals can result if the optimal commutation conditions are to be obtained, as pointed out previously. This situation is somewhat similar to the one encountered in VSC topologies with resonant snubbers at the zero crossings of the ac currents. As it was proposed in the previous section, this problem is minimized if the converter operation is constrained to a set of feasible switching patterns that maximize the snubber inductor voltages during Mode 2 of the active commutation process. This condition is met if the active commutations occur between devices associated to the maximum line to line voltage amplitude at any instant, implying that the snubber inductor voltage is not only maximized but it is also constrained to a fairly narrow range ($\sqrt{3}/2)V_{LL\_peak} \le -2\, v_d(t_2) \le V_{LL\_peak}$). Significant simplification of the design of the snubber inductor is also obtained from the minimization of the snubber voltage fluctuations.

Fig. 6 shows a space vector diagram where both unit and zero displacement power conditions are illustrated. Suitable switching sequences for both operating conditions are given by:

$$\mathbf{i}_1 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{a} \mathbf{i}_1 \ldots, \text{ for } \cos\phi = 1 \qquad (7)$$

$$\mathbf{i}_1 \xrightarrow{p} \mathbf{i}_0 \xrightarrow{p} \mathbf{i}_6 \xrightarrow{a} \mathbf{i}_1 \ldots, \text{ for } \cos\phi = 0 \text{ (lag)}$$

where $\xrightarrow{p}$ and $\xrightarrow{a}$ indicate passive and active commutation sequences, respectively. These switching patterns satisfy the constraint on the application of the active commutation between devices associated with the maximum instantaneous line to line voltage. Notice the change in the position of the null vector in the switching pattern following the change in the displacement power factor. These switching patterns can be promptly generalized for other positions of the current and voltage vectors in the complex plane. Modulation intervals can be computed from direct application of the space vector modulation equations to CSC topologies:

$$t_m = T/i_{dc}\,(-i_{qs}^* \sin\theta_n - i_{ds}^* \cos\theta_n)$$

$$t_n = T/i_{dc}\,(i_{qs}^* \sin\theta_m + i_{ds}^* \cos\theta_m) \qquad (8)$$

where t_m and t_n are the injection intervals of the non-null current vectors $\mathbf{i}_m$ and $\mathbf{i}_n$, respectively, and $\mathbf{i}_m$ leads $\mathbf{i}_n$ by $\pi/3$; i_{qs}^* and i_{ds}^* are the components of $\mathbf{i}_s^*$ in the stationary reference frame in fig. 6.

Notice that in the switching patterns (5) one device remains on for the entire switching interval. In fact, these patterns can be identified with discontinuous PWM schemes commonly used in CSC topologies. In this case, each device is kept on for an interval of $\pi/3$ rad, corresponding to the interval when the associated phase current has the highest amplitude. An advantage of discontinuous PWM algorithms is a significant reduction of the total number of commutations per period. The realization shown in fig. 5 is fully compatible with these algorithms, with minor modifications introduced to constrain the snubber inductor voltage in the active commutation sequence, as discussed above. Other switching patterns are also possible, but optimal commutation conditions are not guaranteed.

Among the drawbacks of the full realization depicted in fig.5, it can be pointed out the relatively large number of extra parts associated with the resonant snubber and the need to balance the voltages across the input filter capacitors.

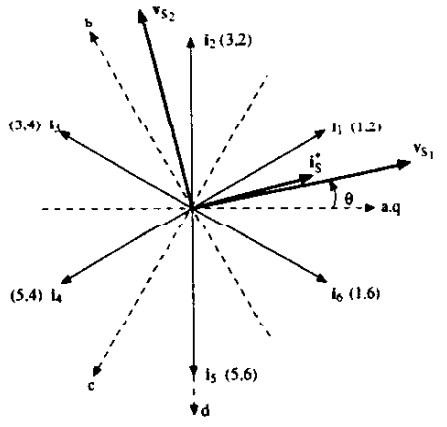

Fig. 6. Space vector diagram.

B. Reduced parts count realization

The conditions set for the operation of the full realization discussed above imply $v_{sn}(t)$ as shown in fig. 6: a low amplitude zero sequence component. Notice that $v_{sn}(t) \leq 0$ when active commutation takes place between devices in the positive group and $v_{sn}(t) \geq 0$ when it happens between devices in the negative group. Moreover, the amplitude of $v_{sn}(t)$ is significantly lower than the line to line peak voltages:

$$| v_{sn}(t) | \leq \frac{V_{LL\,peak}}{4\sqrt{3}} \qquad (9)$$

From the conditions above, one can conclude that near optimal commutation conditions are established if v_{sn} is set equal to the ac voltages neutral potential, or $v_{sn} = 0$. This approximation leads to significant simplification of the topology in fig. 5: only one snubber device and inductor is required for each of the main device groups. Also, since the tap on the ac voltages is no longer required, the total size and parts count of the ac filter capacitor is greatly reduced and voltage balancing is no longer an issue. An artificial neutral can be created from a Y-connection of a balanced set of ac capacitors, as shown in fig. 7. If an input transformer is employed, the neutral point of the secondary side can also be used, if available. It is also possible to eliminate one of the snubber inductors, following the same reasoning for the full realization, but there is a penalty in terms of higher voltage rating for the snubber devices (up by a factor of $\sqrt{3}$).

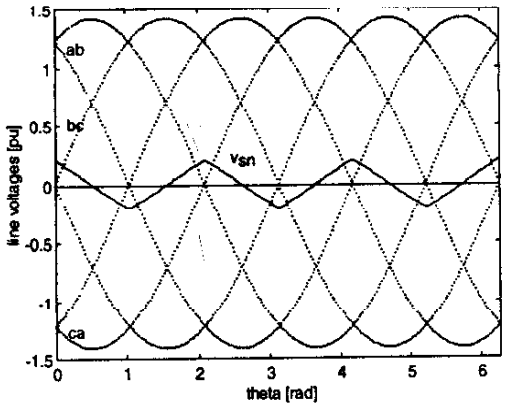

Fig. 6. Optimal snubber driving voltage.

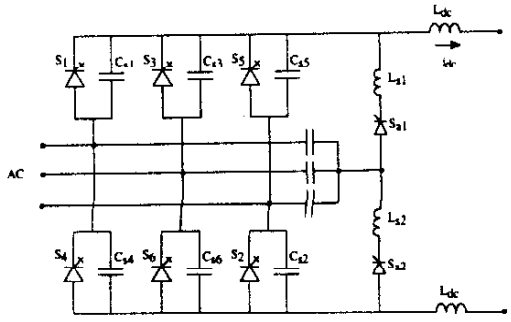

Fig. 7. Reduced parts count realization.

Besides the advantages in terms of cost and size reduction, the CSC topologies with resonant snubbers in figs. 5 and 7 are quite similar from the perspective of PWM compatibility, requiring basically the same switching patterns. For instance, the switching sequences in (5) can also be used here for the situations illustrated in fig. 5. However, since the snubber voltage $v_{sn}(t)$ is not always equal to the average of the voltage amplitude of the phases undergoing commutation, the voltage stress on the main devices increases. Phase plane plots for the limit conditions where active commutation takes place from S_5 to S_1 are shown in fig. 8. This figure shows that with the reduced parts count realization (fig.7), the maximum voltage stress on the main devices is approximately 15% larger than one obtained with the full realization (fig. 5). Although undesirable, this extra voltage stress is not severe and it is largely compensated by the significant reduction in the total parts count required for the implementation of the resonant snubber. This extra voltage stress is reduced in the presence of third harmonic in the input voltages in the variation employing an input transformer.

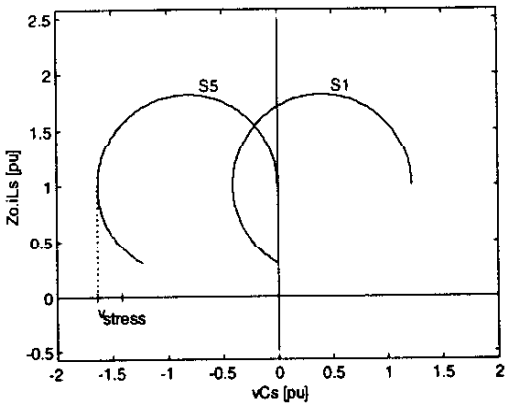

Fig. 8. Active commutation - Mode 3.
(worst case voltage stress).

C. Minimum parts count realization

Further simplification can be obtained by removing the neutral point connection to the snubber induuctor/device branch in fig. 7. After elimination of the redundancies, the minimum parts count realization depicted in fig. 9 is obtained. At the time of its first appearance in the literature [12], the optimal conditions for the active commutation process were not recognized and voltage stresses on the main devices in excess of two times the line to line peak voltage were present. A zero voltage stress control strategy was later on introduced [13,14], employing the commutation and modulation principles discussed in this paper.

A comparison between the generalized topology in fig. 3 with the minimum parts count topology in fig. 9 reveals some particular aspects of this topology. The snubber driving voltage, v_{sn}, associated with active commutations in the positive device group is defined from the state of the negative device group and vice-versa. This fact means that v_{sn} is restricted to

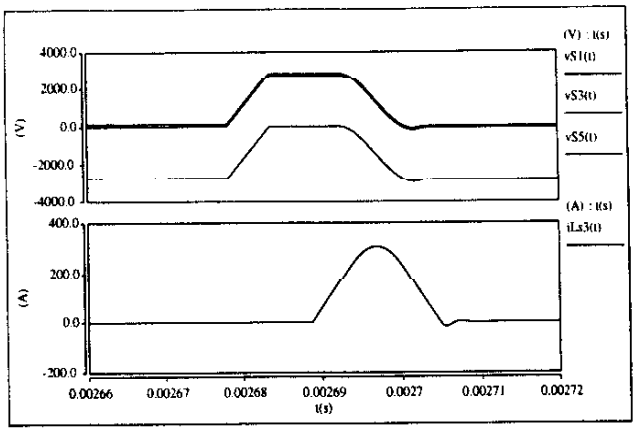

Figure 11. Full realization commutation waveforms.

input current ripple due to the active commutation process in this topology is promptly seen when compared to similar waveforms in figs. 10 and 12. 1.0 pu voltage stresses on the main and snubber devices are shown. An increase in the total number of commutations of the main devices in this topology can be verified from the plot of the voltage across S_1, where commutation in both devices groups occur at any switching period due to the more involved active commutation process.

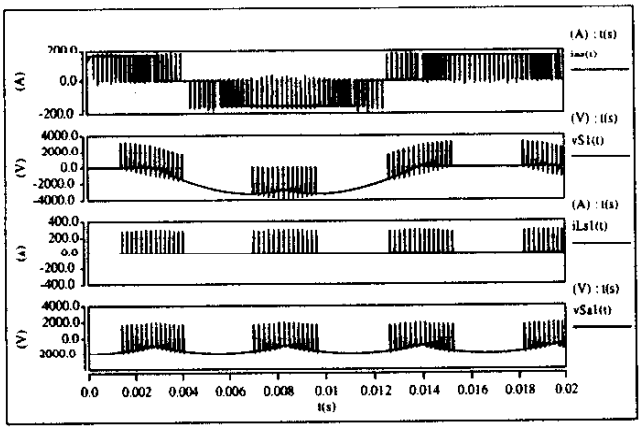

Figure 12. Reduced parts count realization waveforms.

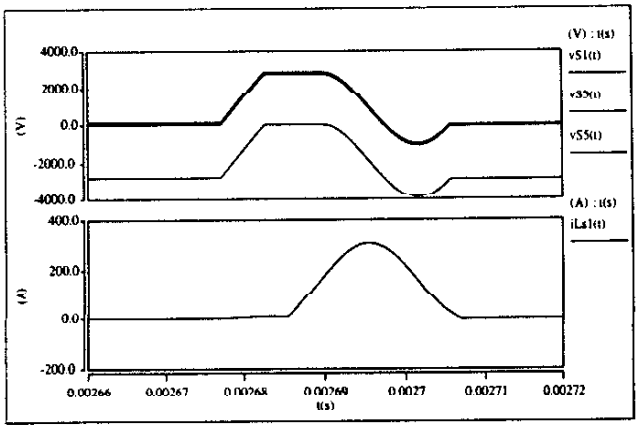

Figure 13. Reduced parts count realization commutation waveforms.

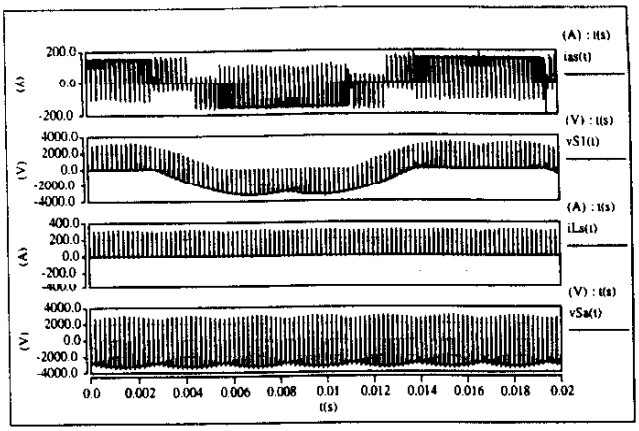

Figure 14. Minimum parts count realization waveforms.

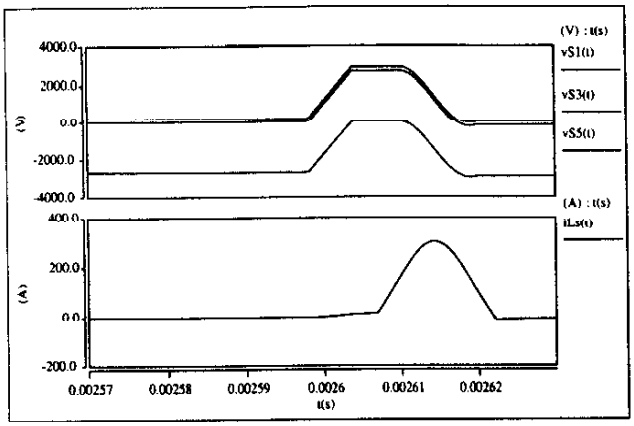

Figure 15. Minimum parts count realization commutation waveforms.

A summary of the ratings of the main converter and snubber devices for the three realizations discussed in this paper are presented in Tables I and II, respectively. Current and voltage amplitudes are expressed in RMS and/or peak values in order to give a better insight of the tradeoffs involved. RMS values of the current through the snubber device are included but should be analyzed on a relative basis since they vary with the converter switching frequency.

A lab prototype of the minimum parts count realization was implemented for further investigation of the practical

TABLE I

Realization	Main device ratings A(peak)	V(peak)	Total VA
Full	1.0	1.0	6.0
RPC	1.0	1.15	6.9
MPC	1.0	1.0	6.0

TABLE II

Realization	Snubber device ratings A(peak)	A(rms)	V(peak)	Total VA A(peak)	A(rms)
Full	2.0	0.16	1.0	12	0.96
RPC	2.0	0.30	0.58	2.32	0.35
MPC	2.0	0.38	1.0	2.0	0.38

issues involved the implemetation of CSC's with resonant snubbers. The converter switches were implemented using series connection of IGBTs and diodes with external connections. The snubber components are C_s = 27nF; L_s = 6μH. The results shown here correspond to operation under the following conditions: V_s = 100 V_{rms}; m = 0.9; cos ϕ = 1; f_s = 10kHz; L_{dc} = 2x 7mH; r_{load} = 10 Ω. The ac filter components are: C_f = 3x50μF; L_f = 3x 800μH. Notice the absence of voltage spikes across the main devices during turn-off, although high di/dt rates exist. The small oscillations seen in the commutation waveforms are mainly due to the switches ESL.

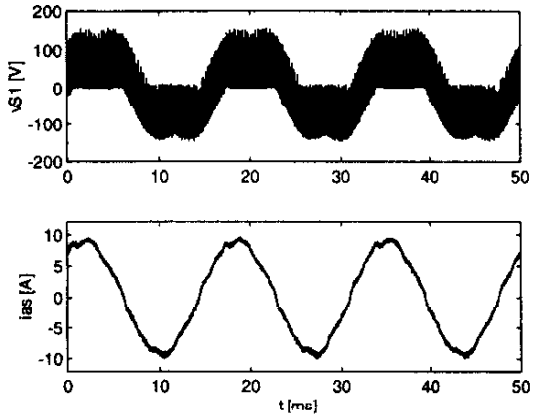

Fig. 16. Minimum parts count realization waveforms.

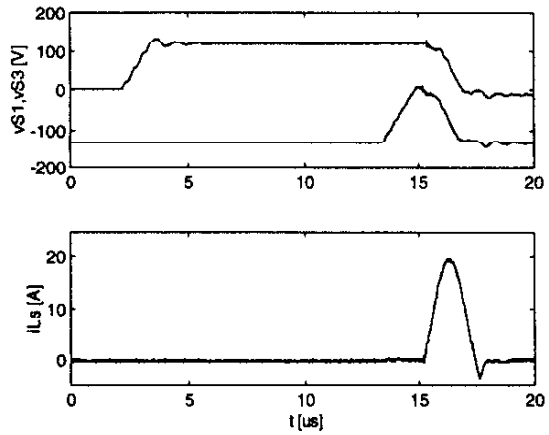

Fig. 17. Minimum parts count realization commutation waveforms.

V. Conclusion

In this paper a study on the characteristics of resonant snubbers with auxiliary switches applied to three phase Current Stiff Converters was presented. The commutation processes were reviewed. The passive commutation process is always guaranteed and only requires a minimum amplitude of the dc bus current to guarantee bounded commutation intervals. The active commutation process, on the other hand is more involved. A generalized representation of CSC topologies with resonant snubbers was introduced, leading to the derivation of not only sufficient but optimal conditions for the occurrence of the active commutation, with optimality defined in terms of minimum voltage stress on the main devices and minimum ratings of the snubber components.

Three realizations were presented and analyzed. The full realization offers flexibility and minimum stress on the main devices at the expense of a number of extras nubber devices and components. A new topology, a reduced parts count realization providing independent commutation of the positive anfa negative device groups, is introduced in this paper. Along with its possible variations, it consists in a good compromise between complexity and performance. As pointed out earlier, the reduced parts count and the full realization offer similar performance in terms of PWM capabilities. The minimum parts count realization requires only one snubber device implying active use of the main converter devices to assist the active commutation process. The ripple in the input currents and total number of switchings of the main devices per switching period increases in this topology. It is important to observe that all these realizations achieve the benefits sought in the introductory section, offering significant advantages over classical RCD snubbers.

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