Dynamic Overmodulation Characteristics of Triangle Intersection PWM Methods

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***Abstract*— In this paper, dynamic overmodulation characteristics of current-regulated carrier-based high-performance pulsewidth modulation (PWM) voltage-source inverter drives are investigated. Dynamic and steady-state overmodulation operating modes are clearly distinguished, and the requirements for obtaining high performance in each mode are shown to be significantly different. Dynamic overmodulation characteristics of the modern triangle intersection PWM methods are modeled and shown to be unique for each method. The study reveals space-vector PWM (SVPWM) exhibits a minimum voltage magnitude error characteristic. It also indicates all the advanced triangle intersection PWM methods, including SVPWM, have limited dynamic overmodulation performance. To enhance the performance, an algorithm with superior performance is adapted from the direct digital PWM approach. Detailed induction motor drive simulations and experimental results illustrate the characteristics of modern triangle intersection PWM methods and the performance gained with the new dynamic overmodulation algorithm.**

***Index Terms*— Dynamics, inverter, modulation, overmodulation, pulsewidth modulation.**

I. Introduction

VOLTAGE-SOURCE inverters (VSI's) are widely utilized in ac motor drive, utility interface, and uninterruptible power supply (UPS) applications as a means for dc⇔ac electric energy conversion. Shown in Fig. 1, the classical VSI which has eight discrete voltage output states, generates a low-frequency output voltage with controllable magnitude and frequency by programming high-frequency voltage pulses. Of the various pulse-programming methods, the carrier-based pulsewidth modulation (PWM) methods are the preferred approach in most applications due to the low harmonic distortion waveform characteristics with well-defined harmonic spectrum, the fixed switching frequency, and the implementation simplicity.

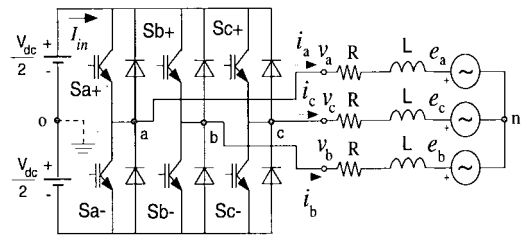

Fig. 1. Circuit diagram of a PWM-VSI drive connected to an *R–L–E*-type load.

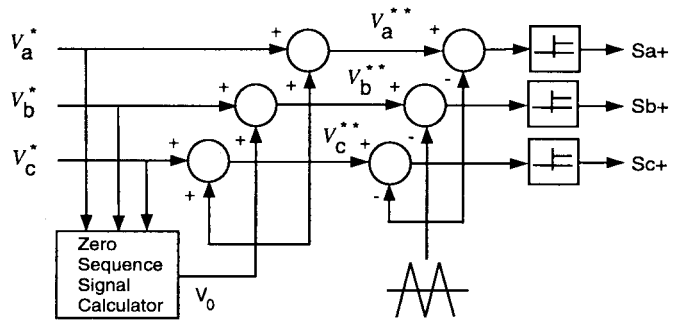

Fig. 2. The generalized signal block diagram of the triangle-intersection-technique-based PWM employing the zero-sequence injection principle.

Carrier-based PWM methods employ the "per carrier cycle volt-second balance" principle to program a desirable inverter output voltage waveform. The triangle intersection implementation technique [1] which is increasingly being implemented in digital hardware/software and the direct digital pulse-programming technique [2] (always software) are the two main methods to match the inverter output voltage with the reference value. As shown in Fig. 2, in isolated neutral-type applications, the triangle intersection method is often accompanied with a zero-sequence signal injection technique to enhance the drive performance when compared to sinusoidal PWM (SPWM). Fig. 3 illustrates the modulation waveforms of the modern zero-sequence signal injection PWM methods [3], [4]. In the direct digital PWM technique, summarized in Fig. 4, the vector-space concept aids the calculation of the inverter state time lengths providing the per-carrier-cycle volt-second balance. In this approach, the partitioning of the two inverter zero states (defined as $\zeta_0 = t_0/(t_0 + t_7)$, and $\zeta_7 = 1 - \zeta_0$)

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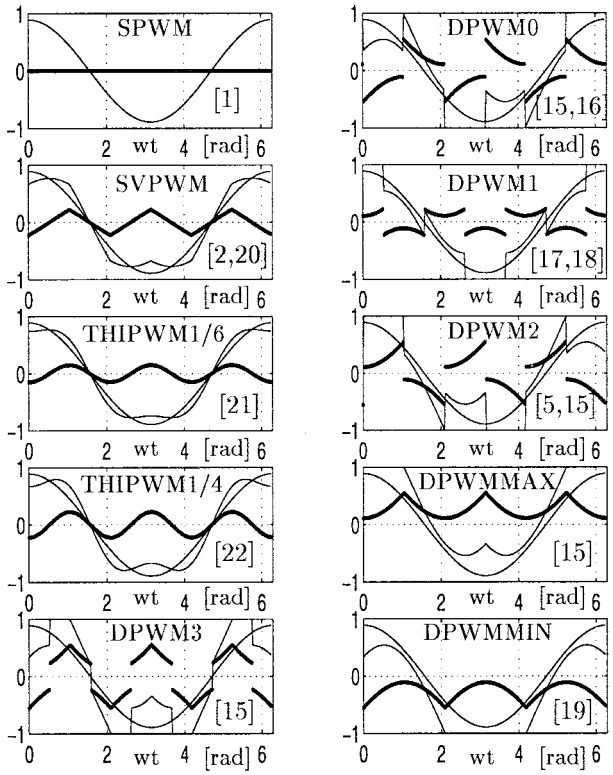

Fig. 3. Modulation waveforms of the modern PWM methods ($M_i = 0.7$).

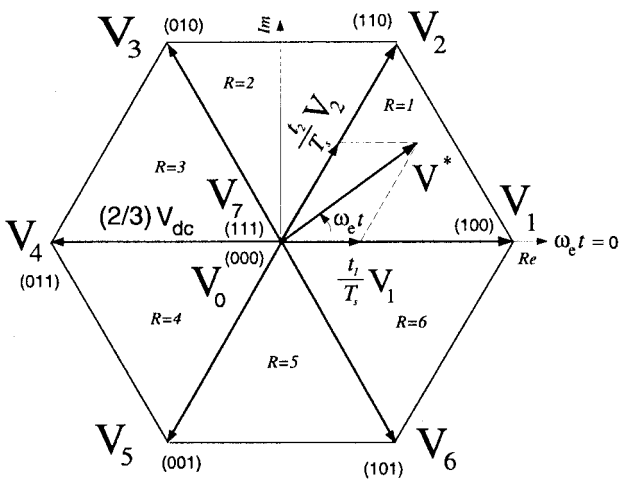

Fig. 4. The space-vector diagram illustrates the direct digital implementation principle. The upper switch states are shown in the bracket as (Sa+, Sb+, Sc+) and "1" is "ON" state, while "0" corresponds to "OFF" state.

provides the necessary degree of freedom in obtaining high performance [5]. The popular direct digital PWM methods are shown in Fig. 5 and their triangle intersection equivalents indicated [4].

In both the triangle intersection and direct digital techniques, the inverter voltage linearity is determined by the modulator characteristics. In the triangle intersection PWM technique, when the modulation signal magnitude becomes larger than the triangle peak value, and in the direct digital PWM technique when the reference voltage vector exceeds the inverter voltage

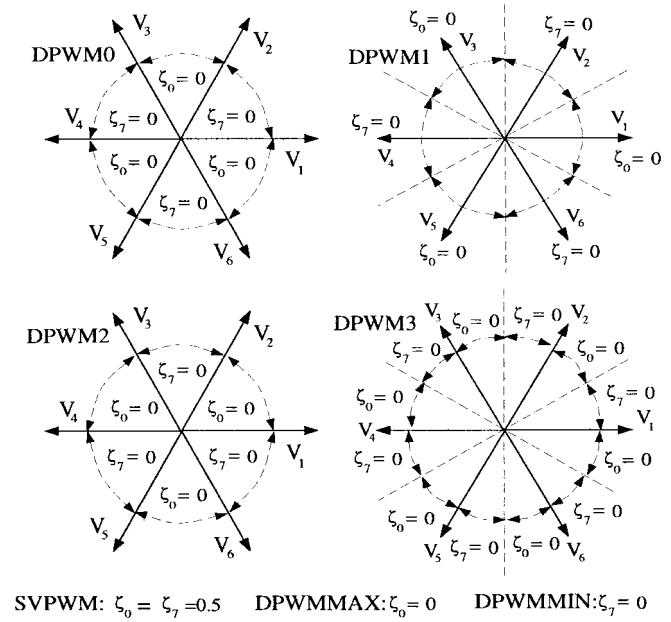

Fig. 5. Zero-state partitioning of the modern PWM methods. DPWMMIN, DPWMMAX, and SVPWM have space-invariant partitioning.

hexagon boundaries, the voltage linearity is lost. With the exception of SPWM and THIPWM1/4, all the methods illustrated in Figs. 3 and 5 are linear in the $[0, 0.907]$ modulation index range (modulation index definition: $M_i^* = |V^*|/V_{1m6\text{step}}$ where $V_{1m6\text{step}} = 2V_{\text{dc}}/\pi$ and $|V^*|$ is the magnitude of the reference voltage vector). The SPWM method looses fundamental component voltage linearity at 0.785 modulation index, and THIPWM1/4 at 0.881 [6]. Outside the linearity range, the ratio of the output voltage fundamental component to its reference value is less than unity. This ratio, the voltage gain (G), rapidly decreases toward zero as the six-step mode is approached. Furthermore, the inverter output voltage contains substantial subcarrier frequency harmonics, and drive performance degrades considerably [6]. The overmodulation range fundamental component voltage gain and waveform quality characteristics of the modern PWM methods, which are important for open-loop (constant volts per hertz) controlled ac motor drives, are well understood [6]–[8].

High-performance ac motor drive and utility interface applications require closed-loop current control algorithms with superior dynamic performance characteristics (in addition to the high steady-state performance). Shown in Fig. 6, the synchronous frame current regulator (SFCR) is the industry standard high-performance current control algorithm. Although the linear modulation range performance of the SFCR meets the requirements in most applications, in the overmodulation region the drive performance significantly degrades, and bandwidth is lost [7], [9]–[12]. Therefore, the steady-state operation of the high-performance PWM-VSI drives is confined to the linear modulation range. However, operation in the overmodulation region is allowed during transients and, in the so-called "dynamic overmodulation" region, the full voltage capability of the modulator is utilized to improve the dynamic response. For example, in an induction motor drive, the speed response

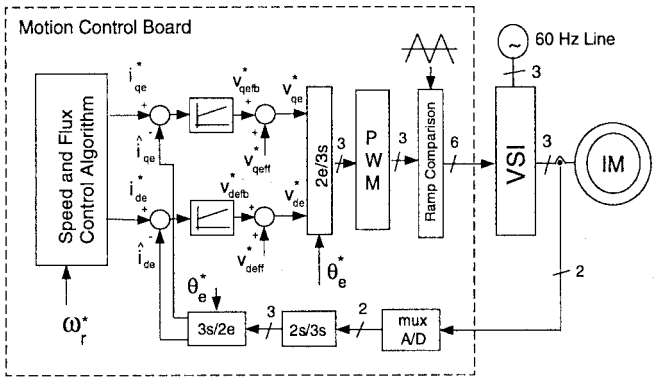

Fig. 6. High-performance induction motor drive system diagram.

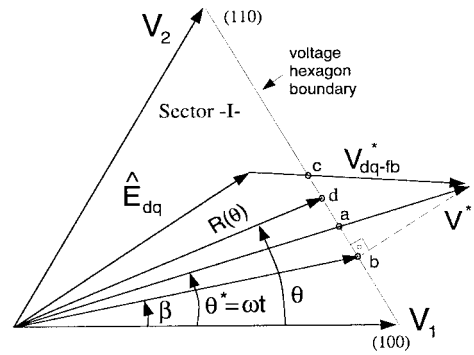

Fig. 7. Vector-space illustration of the popular direct digital PWM technique dynamic overmodulation methods. (a)MPEPWM. (b) MMEPWM. (c) DFWPWM.

and robustness to load torque variations and disturbances can be greatly improved. Since the duration of the transients can be smaller than the minimum fundamental cycle (maximum output frequency), the per-fundamental-cycle modulator characteristics are not appropriate for the investigation of the dynamic overmodulation behavior of a modulator, and the per-carrier-cycle voltage linearity is important. The dynamic overmodulation characteristics of various direct digital PWM methods were investigated in [10], [13], and [14], and various solutions with performance and implementation complexity tradeoffs have been developed. The dynamic overmodulation characteristics of the triangle intersection PWM methods of Fig. 3, however, have not been reported, and their behavior is not well understood.

This paper investigates the dynamic overmodulation characteristics of the modern triangle intersection PWM methods. Section II reviews the direct digital PWM dynamic overmodulation methods. In Section III, the dynamic overmodulation characteristics of the modern triangle intersection PWM methods are analyzed in detail. Following the discussion on the influence of these characteristics on the drive performance in various applications, the induction motor drive behavior is investigated in detail, and strong correlation is obtained between the theory, simulations, and experimental results.

II. Direct Digital PWM Dynamic Overmodulation

In the space-vector approach, employing the following complex variable transformation, the time-domain modulation signals are transformed to the reference vector V^*, which rotates in the complex coordinates at an angular speed $w_e t$

$$V^* = \frac{2}{3}(v_a^* + a v_b^* + a^2 v_c^*) = V_{1m}^* e^{jw_e t}, \quad \text{where } a = e^{j(2\pi/3)}. \tag{1}$$

In the direct digital PWM technique, the complex number volt-second balance equation in the Rth sector of the inverter voltage hexagon in Fig. 4 determines the time length of the two adjacent active inverter states R and $R+1$ ($R = 6 \rightarrow R+1 = 1$) and the total zero-state time length in the following [2]:

$$V_R t_R + V_{R+1} t_{R+1} = V^* T_s \tag{2}$$

$$t_R = \frac{2\sqrt{3}}{\pi} M_i \sin\left(R\frac{\pi}{3} - w_e t\right) T_s \tag{3}$$

$$t_{R+1} = \frac{2\sqrt{3}}{\pi} M_i \sin\left(w_e t - (R-1)\frac{\pi}{3}\right) T_s \tag{4}$$

$$t_0 + t_7 = T_s - t_R - t_{R+1}. \tag{5}$$

The zero-state partitioning is decided by the programmer and, typically, a modulator among those shown in Fig. 5 is selected with switching loss and waveform quality considerations [4], [23]. Fig. 4 indicates the per-fundamental-component voltage linearity region of all the direct digital PWM methods is bounded by the circle which touches the inverter voltage hexagon and the per-carrier-cycle voltage linearity region is bounded by the hexagon. However, once the reference voltage vector tip point lies outside the hexagon, (5) yields a negative time length, hence, an inevitable per-carrier-cycle volt-seconds error. A voltage vector on the hexagon boundary (the modified reference voltage vector) must be selected and at least one back step has to be taken to recalculate the vector time lengths that generate the modified reference voltage vector. Shown in Fig. 7, the three popular modified reference vector choices are the minimum-magnitude-error PWM (MMEPWM) method (also called one-step-optimal method) [13], [24], the minimum-phase-error PWM (MPEPWM) method [14], and the dynamic field-weakening PWM (DFWPWM) method [10], [11]. These methods were evaluated in [10] and [11] for induction motor and ac permanent magnet (PM) motor drives. The superiority of the last method and the implementation simplicity of the second were shown.

In the triangle intersection PWM technique, unlike the direct digital PWM technique, the time lengths of the inverter states are not explicitly calculated; they are an end result of the comparison between the triangular carrier wave and the modulation waves. Therefore, an overmodulation condition can be detected when the modulation wave signal magnitude exceeds the triangle wave magnitude and switching ceases. The overmodulation intervals, i.e., the reference voltage vectors lying outside the modulator hexagon exhibit unique voltage error characteristics in each triangle intersection PWM method, which will be analyzed in detail in the following section.

III. Triangle Intersection PWM Dynamic Overmodulation Characteristics

In the triangle intersection PWM technique, a reference voltage outside the triangle wave boundaries $\pm(V_{\rm dc}/2)$ cannot

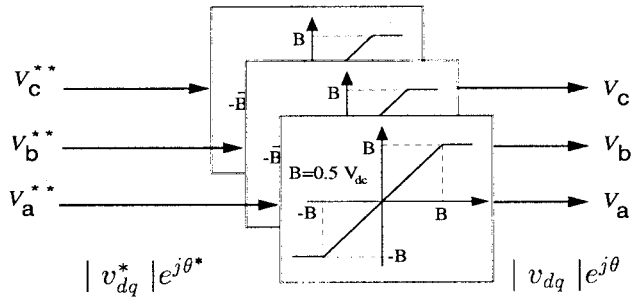

Fig. 8. The saturation block diagram of the triangle intersection PWM methods.

be generated. Modeling this saturation, dynamic overmodulation characteristics of any triangle intersection PWM method can be obtained. With this approach, by passing the reference modulation waves through the limiters shown in Fig. 8 and employing transformation (1), as indicated in Fig. 7, for any reference voltage vector $V_{dq}^* = |V_{dq}^*|e^{j\theta^*}$, an output voltage vector $V_{dq} = |R(\theta)|e^{j\theta}$ is produced. Since the zero-sequence signals of all the modern modulation methods are symmetric and periodic, characterizing the first sector of the hexagon is sufficient. Since the hexagon boundaries are known, characterizing the angular relations, $\theta = f(\theta^*, M_i^*)$ is sufficient. For example, in the first sector $R(\theta)$ can be calculated by the following:

$$|v_{dq}| = R(\theta) = \frac{V_{\rm dc}}{\sqrt{3}\sin\left(\theta + \frac{\pi}{3}\right)}. \tag{6}$$

The dynamic overmodulation characteristics of the triangle intersection PWM methods shown in Fig. 3 have been analyzed with the above approach. The characteristics of SVPWM and the six popular DPWM methods are summarized in the following, while the SPWM, THIPWM1/4, and THIPWM1/6 characteristics are omitted and detailed analysis can be found in [9].

The triangle intersection implementation of SVPWM is possibly the earliest and simplest zero-sequence injection PWM method developed [20]. This method employs the minimum magnitude test to determine the zero-sequence signal. Assume $|v_a^*| \le |v_b^*|$, $|v_c^*|$, then $v_0 = 0.5 \times v_a^*$. The analog implementation of triangle intersection SVPWM employs a diode rectifier circuit to collect the minimum magnitude signal from the three reference signals [20]. The digital implementation requires only three comparisons and a scaling to obtain this signal [25]. In either case, when the modulation signal becomes larger than the saturation boundaries $\pm(V_{\rm dc}/2)$, the saturated modulation signals can be transformed by (1) and in the first segment ($0 \le \theta^* \le \pi/3$), the output voltage vector angle can be calculated in the following:

$$\theta_{\rm SVPWM} = \arctan\left(\sqrt{3}\frac{1 + \frac{6}{\pi}M_i^*\cos\left(\theta^* - \frac{2\pi}{3}\right)}{3 - \frac{6}{\pi}M_i^*\cos\left(\theta^* - \frac{2\pi}{3}\right)}\right). \tag{7}$$

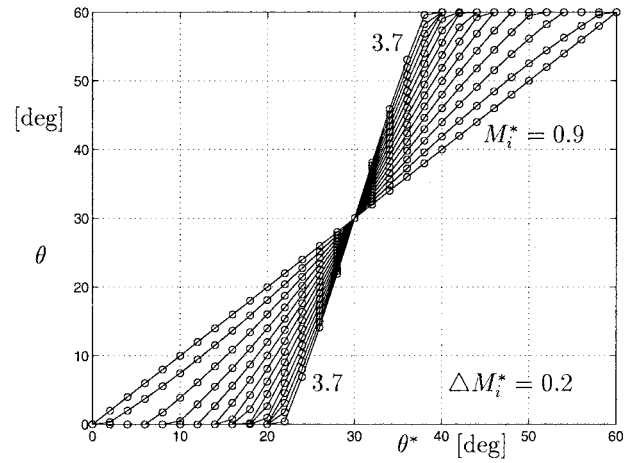

Fig. 9. SVPWM (–) and MMEPWM (o) $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

A software which graphically overlays the MMEPWM, and MPEPWM, and triangle intersection SVPWM dynamic overmodulation reference-output voltage-vector trajectories indicated a surprising result. The MMEPWM and SVPWM vectors are exactly the same. Calculated by projecting the tip point of the reference voltage vector on the hexagon side (point *b* in Fig. 7), the analytical angle relation of MMEPWM yields the following formula:

$$\theta_{\rm MMEPWM} = \beta = -\frac{\pi}{3} + \arctan\left(\frac{\pi}{2\sqrt{3}M_i^*\cos\left(\theta^* + \frac{\pi}{3}\right)}\right). \tag{8}$$

Although (7) and (8) are different in form, their numerical evaluation which is shown in Fig. 9 reveals the fact that their performance is the same. This result indicates when implemented with the triangle intersection technique, the SVPWM method provides very fast (one-step optimal) dynamic overmodulation response. The MMEPWM methods employed in practice are complex and computationally involved [13], [24]. The triangle intersection SVPWM, however, can be implemented in hardware or software with minimum complexity.

The six popular discontinuous PWM (DPWM) methods of which their waveforms are shown in Fig. 3 have found application in high-performance drives due to their low switching loss characteristics and low current-ripple characteristics [3], [23]. Dynamic overmodulation characteristics of these modulators can be modeled depending on their zero-state partitioning, which was summarized in Fig. 5. A zero-state partitioning of $\zeta_0 = 1$, which corresponds to DPWM0 and DPWMMIN in the first hexagon sector, provides the following phase relations:

$$\theta_{\rm DPWM0} = \arctan\left(\frac{\frac{6}{\pi}M_i^*\sin\theta^*}{2 - \frac{2\sqrt{3}}{\pi}M_i^*\sin\theta^*}\right). \tag{9}$$

For DPWM2 and DPWMMAX, the zero-state partitioning in the first hexagon sector is zero ($\zeta_0 = 0$) and the dynamic

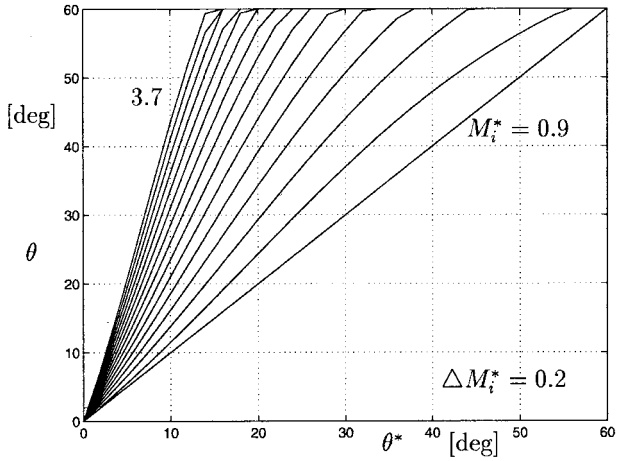

Fig. 10. DPWM0 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 1$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

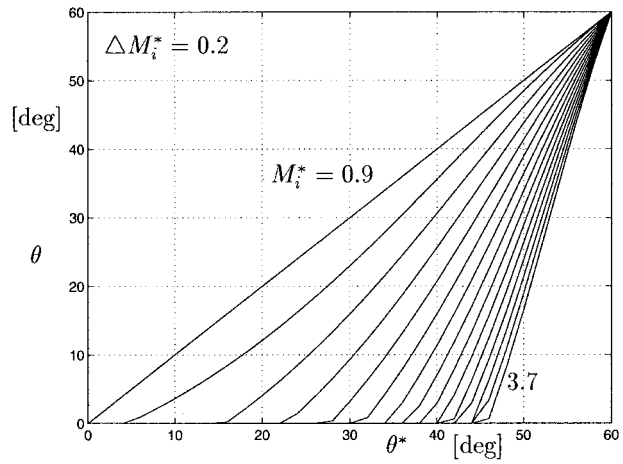

Fig. 11. DPWM2 $\theta = f(\theta^*)$ characteristics ($\zeta_0 = 0$) for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

overmodulation angle relations are calculated as follows:

$$\theta_{\mathrm{DPWM2}} = \arctan\left(\sqrt{3}\frac{1 - \dfrac{2\sqrt{3}}{\pi}M_i^*\cos\left(\theta^* + \dfrac{\pi}{6}\right)}{1 + \dfrac{2\sqrt{3}}{\pi}M_i^*\cos\left(\theta^* + \dfrac{\pi}{6}\right)}\right). \tag{10}$$

Since, in DPWM1, the zero-state partitioning is $\zeta_0 = 0$ for $0 \le \theta^* \le \pi/6$ and $\zeta_0 = 1$ for $\pi/6 \le \theta^* \le \pi/3$, the overmodulation phase relations are calculated from (9) and (10) in the following:

$$\theta_{\mathrm{DPWM1}} = \begin{cases} \theta_{\mathrm{DPWM2}} & 0 \le \theta^* \le \dfrac{\pi}{6} \\ \theta_{\mathrm{DPWM0}} & \dfrac{\pi}{6} \le \theta^* \le \dfrac{\pi}{3}. \end{cases} \tag{11}$$

The dynamic overmodulation characteristics of DPWM3 are found with the same approach in the following:

$$\theta_{\mathrm{DPWM3}} = \begin{cases} \theta_{\mathrm{DPWM0}} & 0 \le \theta^* \le \dfrac{\pi}{6} \\ \theta_{\mathrm{DPWM2}} & \dfrac{\pi}{6} \le \theta^* \le \dfrac{\pi}{3}. \end{cases} \tag{12}$$

The following phase-error definition aids the discussion on the modulator dynamic overmodulation characteristics:

$$\triangle\theta = \theta^* - \theta. \tag{13}$$

The reference and output voltage-vector phase relations of DPWM0, DPWM1, and DPWM2 are shown in Figs. 10–12 for various M_i^* values. In DPWM0, the output vector always leads the reference voltage vector, while for DPWM2, the opposite is true. Since DPWM1 is a combination of DPWM0 and DPWM2, in this case, the output vector lags the reference for the first 30° segment of the sector and leads in the following 30° segment. Note the phase error of SVPWM also changes polarity at 30°, however, the change is smoother and the error magnitude is smaller. DPWM3 follows the opposite pattern of DPWM1 and, both in DPWM1 and DPWM3, the output voltage vector experiences a jump near the midsection of the hexagon sector (avoiding the vector at $\pi/6$). For

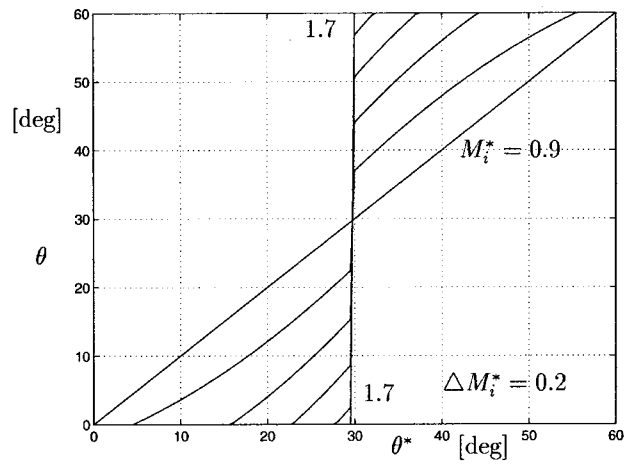

Fig. 12. DPWM1 $\theta = f(\theta^*)$ characteristics for various M_i^* values. M_i^* starts at 0.9 and increments with 0.2 units.

all the discussed methods, the behavior in the first 60° is repeated periodically in the remainder of the sectors. In all the methods, an increase in the modulation index results in phase-error increase, and the error is the largest in DPWM1. It is worth mentioning that the direct digital overmodulation technique reported in [26] (it retains the reference voltage dominant axis component) is equivalent to DPWM1. Since the phase error completely determines the dynamic overmodulation performance of a modulator, the $\theta = f(\theta^*)$ [or $\triangle\theta = f(\theta^*)$] relations are the main characteristics in predicting the modulator-dependent drive dynamic behavior.

In practice, the theoretical modulator linearity boundaries are further reduced due to the inverter blanking time and/or minimum pulsewidth constraint of the inverter drives [6]. If the narrow voltage pulses are eliminated, the output voltage magnitude becomes larger than the theoretical value and the phase-error polarity is always opposite to theoretical modulator phase-error polarity. The phase and magnitude errors are dependent on the minimum pulsewidth to the carrier cycle ratio and increase with it. Further details on modeling these second-order effects is reported in [9].

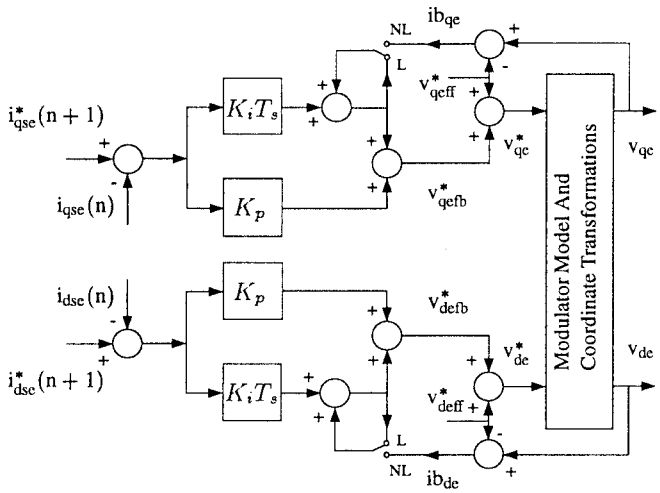

Fig. 13. Discrete-time signal flow diagram of the synchronous frame PI current controller with antiwindup.

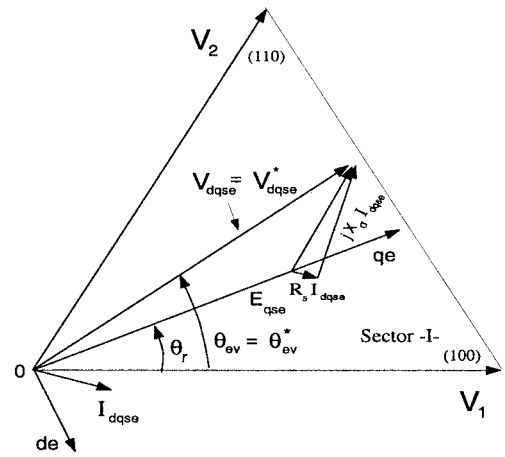

Fig. 14. Synchronous frame RFO induction motor voltage-vector diagram illustrated along with the inverter voltage-vector diagram.

IV. Drive Dynamic Overmodulation Behavior

The dynamic overmodulation performance of an ac motor drive or an ac-line-connected PWM-VSI is determined by the modulator phase-error characteristics, the drive control algorithm, and load characteristics. In the following, we first discuss the SFCR design, then investigate the system-level (SFCR–modulator–load) overmodulation behavior.

Since the conventional SFCR design assumes modulator linearity, in the overmodulation region, significant delays and overshoot can result. To minimize the performance degradation, antiwindup controllers which bound the integrator outputs of the proportional integral (PI) controllers are employed, and selecting a proper integrator limit value is vital in maximizing the dynamic performance [27]. An approach which selects SFCR integrator boundaries that keep the controller output signals on the edge of linearity was reported in [10] and [11]. In this approach, shown in Fig. 13, the SFCR discrete-time signal flow diagram antiwindup limiters are only activated in the overmodulation region. During the (n)th carrier cycle, the $(n+1)$th cycle reference voltages v_{qe}^* and v_{de}^* are calculated and transformed to stationary frame "abc" variables. In the modulator block, a zero-sequence signal is injected to the "abc" voltages to form the modulation signals. These signals are passed through the saturation limits of Fig. 8 and rotated to the synchronous frame to predict the $(n+1)$th cycle output voltages v_{qe} and v_{de}. If the reference and output signals are different (indicating a dynamic overmodulation condition), then the antiwindup signals reset the integrators to the boundary values ib_{qe} and ib_{de} (signal flow through "*NL*"), otherwise, the linear modulation operating mode resumes (signal flow through "*L*"). In the overmodulation region, the "q" and "d" channel integrators are reset to $v_{qe}-v_{q\mathrm{eff}}^*$ and $v_{de}-v_{d\mathrm{eff}}^*$ values, so that in the following carrier cycle, the calculated reference voltage vector is close to the hexagon boundary. With this approach, if the error reverses polarity, the linearity region is immediately reentered. If the error is zero or its polarity does not change, then the reference voltage remains near the modulator linearity boundary, however, it may be at a different point.

Along with the modulator and SFCR with antiwindup, the inverter dc voltage source and ac load characteristics define the system overmodulation behavior. Perhaps the most intuitive explanation of the drive behavior is to consider the effect of the phase error on the synchronous frame reference and output voltage vector "d" and "q" components. Depending on the modulator phase-error value, during a dynamic overmodulation condition the inverter output voltage vector may lead or lag the reference voltage vector, and the lead and lag conditions result in different "de"- and "qe"–axes voltages. As a result, the drift of the "de"- and "qe"-axes currents from the reference values may be quite different in the lagging and leading conditions. Therefore, the currents drift from the reference values according to the modulator phase-error characteristics. For example, with SVPWM, the drift always yields the smallest current-error vector every carrier cycle and, therefore, SVPWM is suitable for applications where the inverter ac-side current-error minimization is of prime interest. However, in most cascade-controlled drives (from the outmost to the innermost loops, position–speed–current control loops form the cascade control system) the primary goal is to maintain the motion quality. A dynamic overmodulation condition implies an increase in the demanded torque, and torque maximization is the prime concern. Since the torque maximization criteria and current-error minimization criteria may require two different voltage vectors, the influence of the modulator phase error on the drive motor torque must be clearly understood. Therefore, the motor dynamic behavior has to be considered. In this paper, mainly the induction motor dynamic overmodulation behavior will be discussed. However, the other motor drive types and utility-interfaced PWM-VSI exhibit similar characteristics, and the results of this investigation can be interpreted for those applications [9].

To establish an intuitive background for the drive dynamic overmodulation study, the steady-state behavior of the rotor-flux-oriented (RFO) indirect-field-orientation-controlled (IFOC) induction motor will be briefly discussed first. Then, the deviation from steady state and entrance to the overmodulation region will be considered. As shown in Fig. 14, during

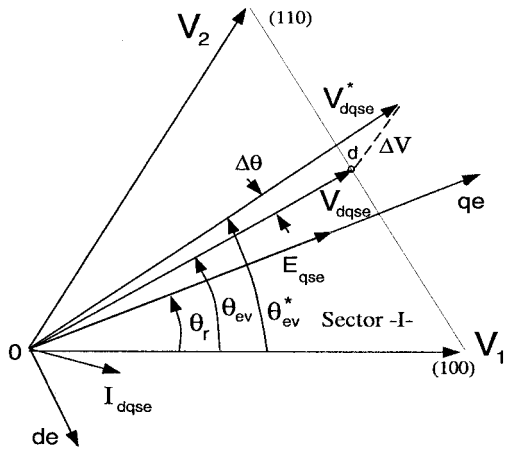

Fig. 15. Synchronous frame RFO induction motor voltage-vector diagram representing an overmodulation condition.

steady state, the reference and output voltages of the RFO-IFOC drive are in phase, and they have equal magnitude. The inverter output voltage balances the motor EMF and the voltage drop across the equivalent impedance.

As shown in Fig. 15, the RFO synchronous frame induction motor overmodulation voltage-vector diagram [28] indicates during overmodulation condition the "qe"- and "de"-axes stator voltages are different from the reference values and, as a result, the "qe"- and "de"-axes currents drift from their reference values. Thus, the motor torque linearity is lost ($T_e = K_{te}(i_{qse}\lambda_{dse} - i_{dse}\lambda_{qse})$) and motion quality degrades. For example, if v^*_{dqse}, v_{dqse}, and the "qe" axis are in the first 30° segment of a hexagon sector, and v_{dqse} lags v^*_{dqse}, then the overmodulation condition results in a smaller v_{dse} and larger v_{qse} compared to the phase-error lead condition. As a result, i_{qse} becomes larger and i_{dse} smaller than the lead case. Although this dynamic field-weakening condition may transiently increase the drive torque, motion quality degrades due to the loss of torque linearity. As the current regulation becomes poor and the field orientation condition is lost, the rotor flux varies and dynamics are excited. Beyond this point, the dynamics cannot be described with the steady-state equivalent circuit of the motor drive; therefore, a full dynamic model is required for a detailed investigation. However, the above-discussed simple model illustrates the importance of the modulator phase error and also aids in explaining the influence of the phase lag and lead conditions. The most important conclusion of this intuitive example is that, with a strong dynamic field-weakening condition or the opposite effect, the drive performance may significantly degrade. Therefore, the modulator phase error must be controlled in a manner to maintain good drive performance as much as possible.

Triangle intersection PWM methods exhibit unique phase-error characteristics; therefore, it is expected that a drive performs differently with different modulators. Since the current controller antiwindup limiters bound the reference voltage magnitude (i.e., M_i^*), the phase-error magnitude is also practically bounded. With the proportional and integral gains of the current controller selected properly, the dynamic overmodulation conditions result in reference voltage vectors with a magnitude comparable to the inverter hexagon boundaries. Therefore, the phase errors and the magnitude of dynamic overmodulation transients are also limited. Thus, the antiwindup limiters are essential in avoiding unwanted dynamics. However, the antiwindup limiters may not be sufficient to obtain high performance (any motor torque is a strong function of the phase error, and even a small phase error may result in a strong dynamic condition) and a system-level study is required. In the following section, detailed induction motor drive simulations address these performance issues.

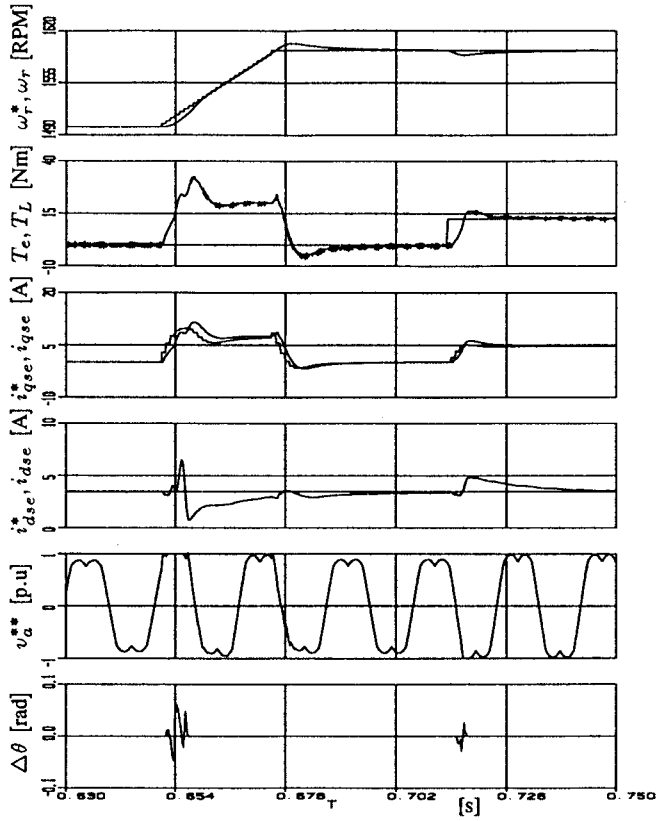

Fig. 16. Induction motor drive SVPWM dynamic overmodulation behavior under speed reference ramp change and load torque step change.

V. Computer Simulations

The theoretical modulator characterization study has been supported by detailed induction motor drive simulations. A 5-hp, 1745-r/min, 460-V, 6.9-A, four-pole induction motor with the lumped equivalent circuit parameters of $r_s = 1.97\ \Omega$, $r_r = 1.73\ \Omega$, $L_{ls} = L_{lr} = 11.2$ mH, and $L_m = 275.6$ mH is driven through a PWM-VSI drive. The inverter dc-bus voltage is 620 V, and the carrier frequency is 5 kHz. The drive employs an IFOC algorithm [28], and a fully digital synchronous frame PI current controller with voltage feedforward and antiwindup provides high-performance current regulation [9], [25]. The digital current controller employs the synchronous sampling technique with 5-kHz sampling rate. The controller bandwidth is 250 Hz. The rated synchronous frame stator "d"- and "q"-axes currents are $I_{dseR} = 3.38$ A, and $I_{qseR} = 9.12$ A. The drive speed is controlled with a digital PI controller

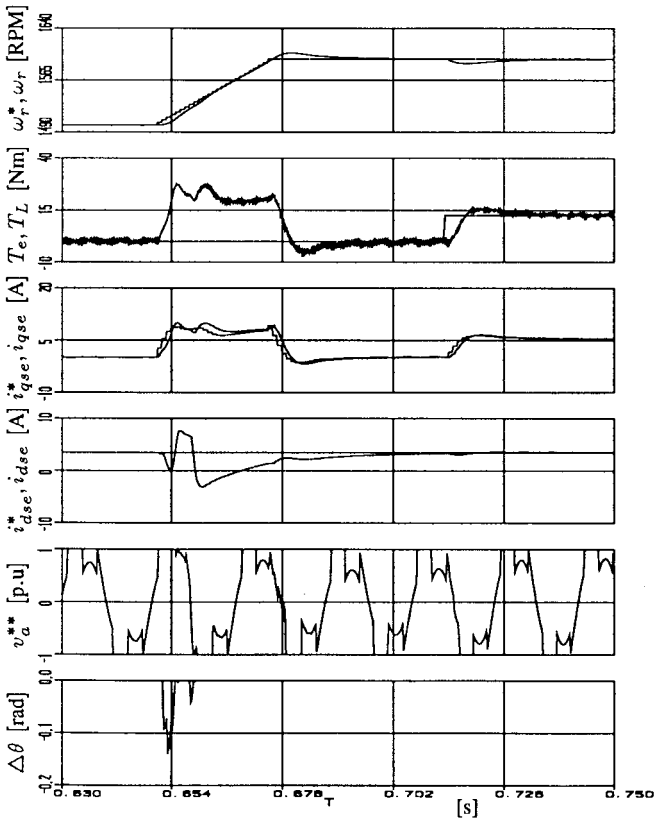

Fig. 17. Induction motor drive DPWM0 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

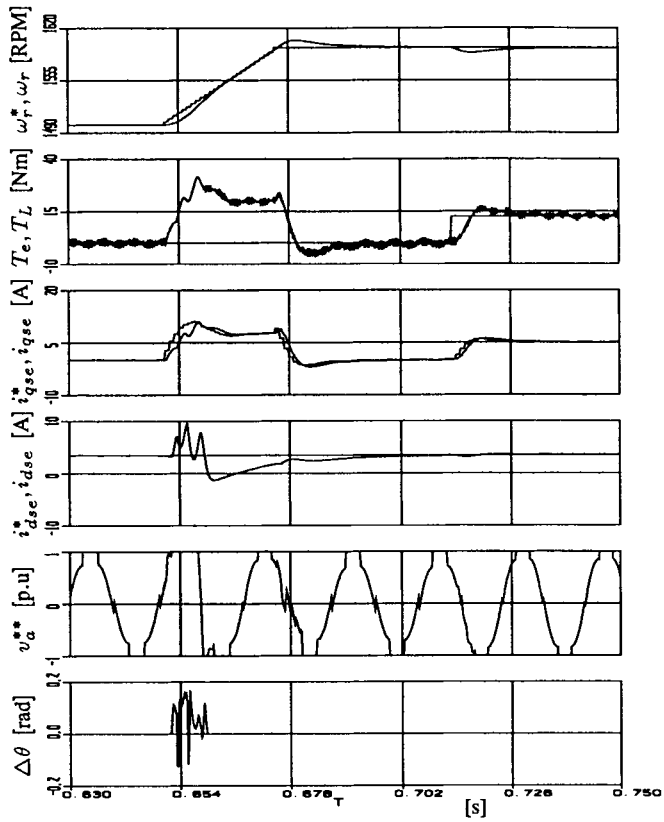

Fig. 18. Induction motor drive DPWM1 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

with antiwindup and the antiwindup limit equals the inverter maximum current capability. The speed controller sampling rate is 1 kHz and has a 25-Hz (electrical) bandwidth. The drive total inertia is $J_m = 0.05$ kg·m^2.

The computer simulations of Figs. 16–19 illustrate drive overmodulation performance with various modulators. While the drive is operating at 1500 r/min and no load, an overmodulation condition is generated with a speed reference change and application of a load torque. A speed ramp command ω_r^* at $t = 0.65$ s increases the speed from 1500 to 1600 r/min in 24 ms, and the load torque T_L increases at $t = 0.71$ s from zero to 50% of the rated motor torque. Fig. 16 illustrates the dynamics with SVPWM. The voltage-vector phase-error polarity and magnitude vary according to Fig. 9. The current controller antiwindup channels keep the reference voltage vector near the hexagon boundary (M_i^* of (7) is kept small) and the SVPWM method selects a vector close to the reference vector (one-step-optimal), resulting in a small phase error. As Fig. 16 indicates, SVPWM provides good performance.

Shown in Fig. 17, the DPWM0-modulated system always has a negative phase error, consistent with the theoretical prediction. As the output voltage vector leads the reference voltage vector more than the SVPWM case, the field current experiences poorer regulation. Although results show an increase in torque and slightly better speed response, the oscillatory behavior can eventually result in a drive failure under certain operating conditions. Shown in Fig. 18, the DPWM1-modulated system exhibits similar behavior to SVPWM, however, its phase-error magnitude is larger and the field current regulation capability degrades, as in the DPWM0 case. Although DPWM1 has a substantially higher fundamental component gain than the other modulators [6], its dynamic performance is poorer than SVPWM. Therefore, it becomes clear that the open-loop drive overmodulation performance criteria which suggests the modulator with the highest voltage gain is superior to the rest, and the closed-loop system dynamic overmodulation performance criteria which suggests the modulator with the best speed response and disturbance rejection is superior to the rest, are different and result in a different modulator selection.

Shown in Fig. 19, the DPWM2-modulated system simulations illustrate the dynamic overmodulation performance deficiency of this method. The phase error is large and always positive (lagging); the field current increases and results in reduced torque, hence, very poor dynamics. Although in induction motor drive applications the linear modulation range switching loss characteristic of DPWM2 is superior to other modulators [23], its overmodulation performance is quite poor. Therefore, operation of DPWM2 in the overmodulation region should be prohibited or control algorithm modifications are required.

The above simulation results indicate the SVPWM dynamic overmodulation performance is superior to all the other triangle intersection PWM methods. The modulator generates an output voltage vector with a small phase error and its one-step-optimal current regulation characteristic can successfully

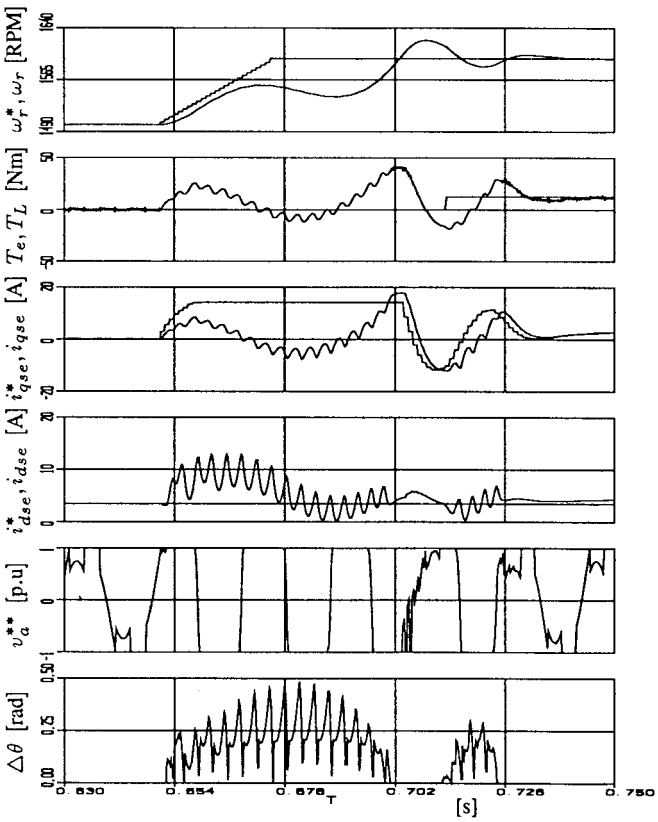

Fig. 19. Induction motor drive DPWM2 dynamic overmodulation behavior under speed reference ramp change and load torque step change.

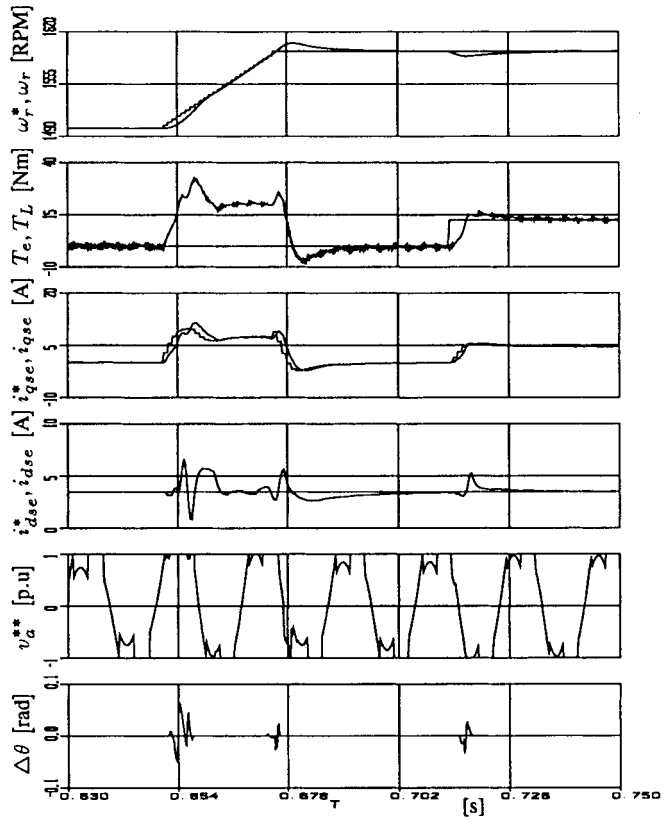

Fig. 20. Induction motor drive DPWM2 (linear mode) and SVPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

manipulate most dynamic conditions. However, very low inertia and very abrupt dynamic conditions could still not be properly manipulated, and sufficiently large phase-error intervals may result in unstable behavior and unacceptable drive performance. Therefore, the modulator choice must be carefully made.

Since the above simulation studies suggest the DPWM methods have poor dynamic overmodulation characteristics and their large phase errors result in strong unwanted dynamics, when employing these modulators, modifications to the drive control algorithm become inevitable. Since the DPWM methods have superior linear modulation range switching loss and waveform quality characteristics, a moderate increase in the control algorithm complexity and drive cost can be easily compensated with the performance gain. In this paper, two modification methods are suggested.

In the first approach, the DPWM method of choice is combined with SVPWM, and when a dynamic overmodulation condition is detected, SVPWM is activated, while in the linear region the DPWM method resumes control. Fig. 20 illustrates the drive dynamic behavior with this algorithm. As the simulation waveforms indicate, in the linear modulation region DPWM2 is active, however, as a dynamic overmodulation condition occurs, the SVPWM signals are activated and the dynamics are rapidly manipulated. Since recent commercial drives often employ SVPWM and a DPWM method in combination to improve the linear modulation range waveform quality (for small M_i, SVPWM is selected, and for large M_i, DPWM is selected) and reduce switching losses [23], the modulation-signal-generating blocks may already exist in a drive, and only an additional loop and recalculation of the modulation signals is required. In particular, implementing such an algorithm in a digital-signal-processor (DSP)-based controller is an easy task.

In the second approach, a more complex and higher performance algorithm, the dynamic field-weakening method can be adapted from the direct digital technique [10], [11]. As shown in Fig. 7, in this approach, the motor back EMF $\hat{E}_{dqe}$ (calculated from the estimated stator flux) and the PI current controller outputs V_{dqefb}^* are vectorially added and the intersection point with the hexagon (point "*c*" in the figure) is the tip point of the vector that forces the current-error vector to move in the controller reference direction. By employing this algorithm, the reference voltage vector, which is outside the inverter hexagon, is modified and returned to the inverter hexagon with a corrected phase, such that any modulation method will exactly match the modified reference vector. Therefore, the modification algorithm performs equivalently with all the triangle intersection modulation methods. The simulation waveforms in Fig. 21 illustrate the performance of DPWM2 combined with the dynamic field-weakening method. When a dynamic overmodulation condition occurs, the dynamic field-weakening algorithm is activated and the reference vector is modified and returned to the hexagon boundary, such that DPWM2 exactly generates this vector. Note that this method generates a significantly small phase error, and

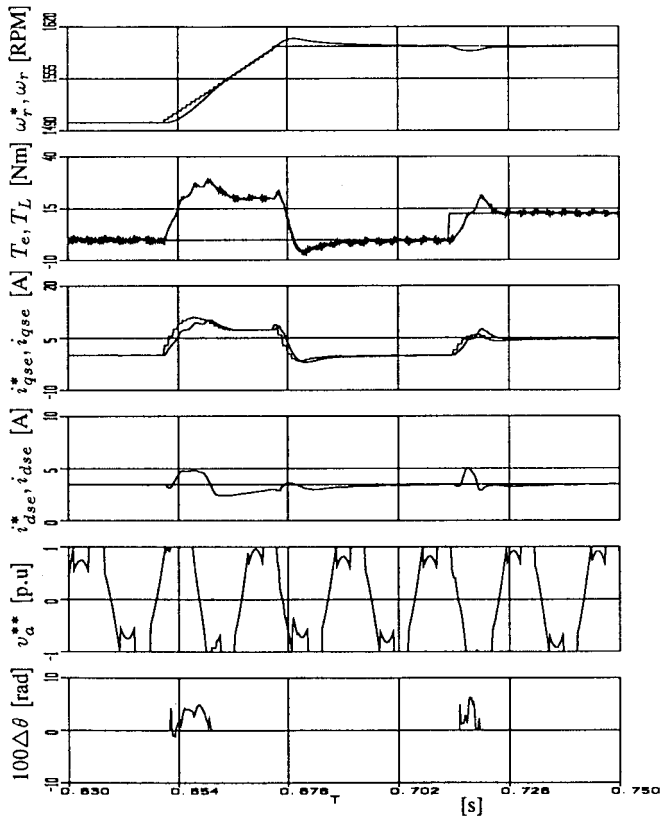

Fig. 21. Induction motor drive DPWM2 (linear mode) and DFWPWM (overmodulation) combined algorithm dynamic overmodulation behavior.

the field current experiences less transients than the SVPWM case. Also note the phase error alternates and during the speed ramp the field current increases for a short time interval. Therefore, a better term for the method would be "a phase-error regulation method." This method, however, is complex and requires a substantial amount of computations for relocating the reference voltage vector. Hence, it is only suitable for high-performance drives with fast DSP controllers.

VI. Experimental Results

The dynamic overmodulation behavior of an IFOC-algorithm-based synchronous frame current-regulated induction motor drive was experimentally investigated. Due to the laboratory limitations only an induction motor (5 hp, 60 Hz, 460 V, 6.9 A, 1745 r/min, 0.07 kg·m^2) without load and without additional inertia could be tested. A MOTOROLA 56 005 DSP (40-MHz clock cycle) based control board and a commercial PWM-VSI power structure (460 V, 21A, 620 Vdc, diode rectifier front-end type) were interfaced to form the laboratory PWM inverter drive.

An SFCR with the previously described antiwindup structure was implemented, and the carrier frequency was 5 kHz. Due to the laboratory drive limitations, only analog speed feedback information was available (the DSP read the A/D converted speed signal at 500-Hz rate), and the DSP estimated the shaft position by integrating the speed signal. The lack of accurate shaft position information significantly reduced the bandwidth of the drive. Therefore, the performance of the experimental system (it had a 5-Hz speed loop bandwidth, similar to speed-observer-based shaft-encoderless drives) and the computer-simulated system (25-Hz bandwidth, a typical vector-controlled industrial drive with shaft-encoder feedback) could not be directly compared. However, the experimental system bandwidth was sufficient to generate a notable dynamic overmodulation transient and illustrate the performance of various modulators.

In order to illustrate the dynamic overmodulation performance of the SFCR-based drive with various modulators, a dynamic overmodulation condition was forced by rapidly varying the speed reference signal. While the drive was operating at 1350 r/min (45-Hz electrical frequency) at steady state and no load conditions, the speed reference was increased to 1650 r/min (55-Hz electrical frequency) in 50 ms with a ramp function (incremented at 1 ms rate). The dynamic overmodulation test was conducted with all the discussed modulators. The experimental investigations indicated SVPWM performed best and DPWM2 worst. Therefore, these modulators deserve attention.

The oscillograms of DPWM2 are illustrated in Figs. 22–24. The saturated modulation waves indicate the drive exhibits dynamic overmodulation. Due to saturation, d- and q-axes current regulation becomes poor and the current and speed errors become large and oscillatory. Due to heavy saturation, initially, the phase currents approach the six-step mode current waveforms. However, as the speed error gradually decreases, the linear modulation region is reentered and they become sinusoidal.

The oscillograms of SVPWM are illustrated in Figs. 25–27. As the oscillograms clearly indicate, the SVPWM performance is significantly less oscillatory than DPWM2. The speed error of DPWM2 is significantly larger than SVPWM. The comparison between the d- and q-axes current errors of DPWM2 and SVPWM indicates the DPWM2 modulator performance is significantly oscillatory and a strong interaction between the current regulator and the modulator exists. Under a dynamic overmodulation condition, DPWM2 results in poor d- and q-axes voltage partitioning and results in significantly larger flux current and significantly smaller torque current. As a result, the dynamic performance significantly degrades. Therefore, it can be concluded the DPWM2 dynamic performance is inferior to SVPWM. The experimental investigation of DPWM0 and DPWM1 indicated the performance of DPWM0 and DPWM1 was better than DPWM2, however, slightly worse than SVPWM. Further details on the experimental results and the performance of DPWM0 and DPWM1 can be found in [9].

Since the experimental drive had a low speed-loop bandwidth (therefore, low controller gains), the dynamics were not as strong as the computer-simulated system. However, with a higher bandwidth, the drive dynamic overmodulation performance would become more oscillatory, and stronger interaction between the PI controllers and the modulators would become inevitable. As illustrated with computer simulations, in this case, the DPWM2 performance would become unacceptable.

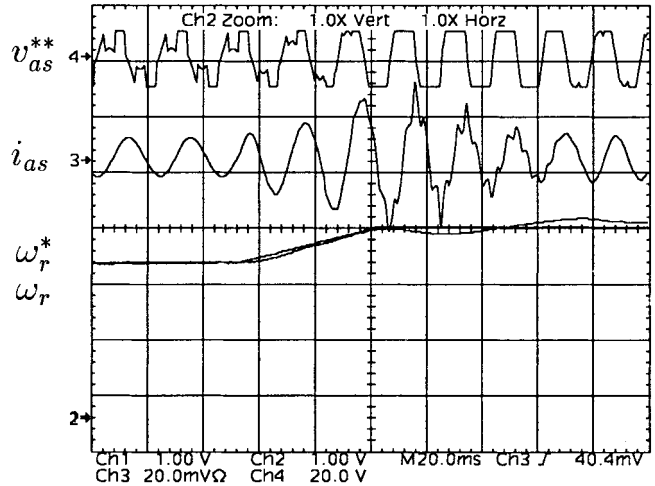

Fig. 22. DPWM2 voltage, current, speed, and speed reference oscillograms. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; ω_r^*, ω_r: 500 r/min/div.

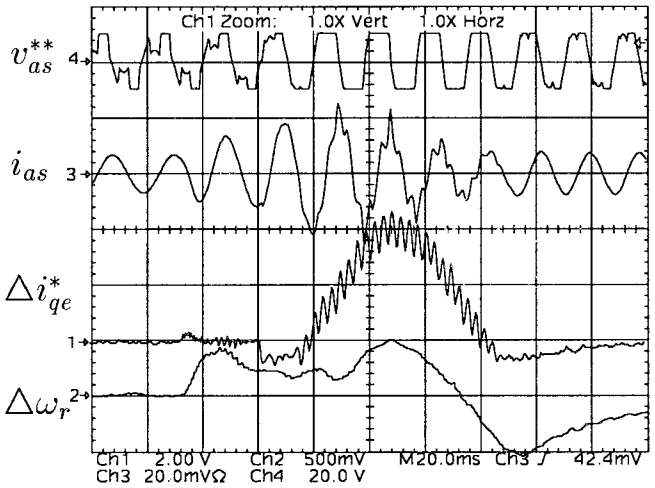

Fig. 23. DPWM2 voltage, current, q-axis current error, and speed error. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; $\triangle i_{qe}^*$: 4 A/div; $\triangle \omega_r$: 60 r/min/div.

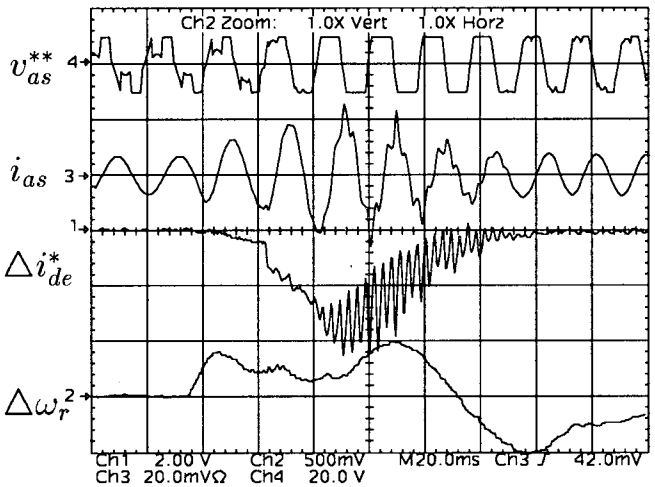

Fig. 24. DPWM2 voltage, current, d-axis current error, and speed error. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; $\triangle i_{de}^*$: 4 A/div; $\triangle \omega_r$: 60 r/min/div.

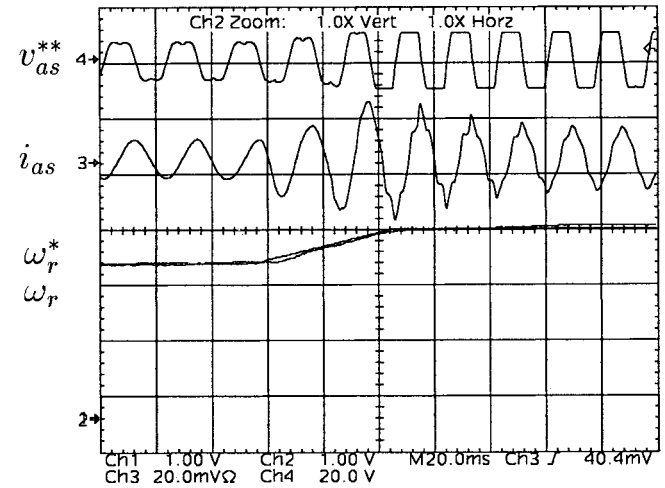

Fig. 25. SVPWM voltage, current, speed, and speed reference oscillograms. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; ω_r^*, ω_r: 500 r/min/div.

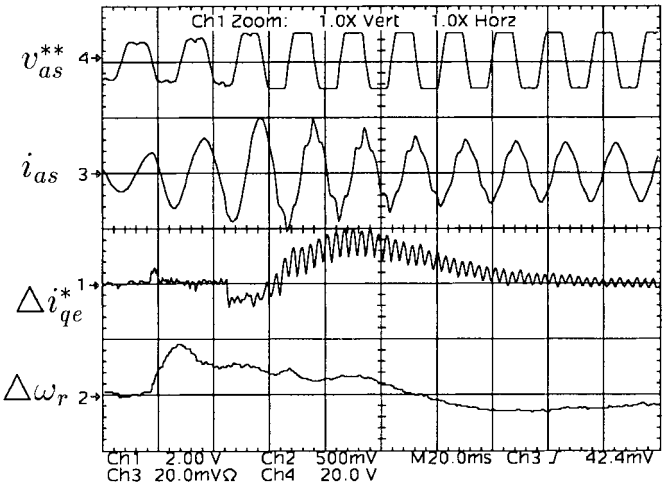

Fig. 26. SVPWM voltage, current, q-axis current error, and speed error. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; $\triangle i_{qe}^*$: 4 A/div; $\triangle \omega_r$: 60 r/min/div.

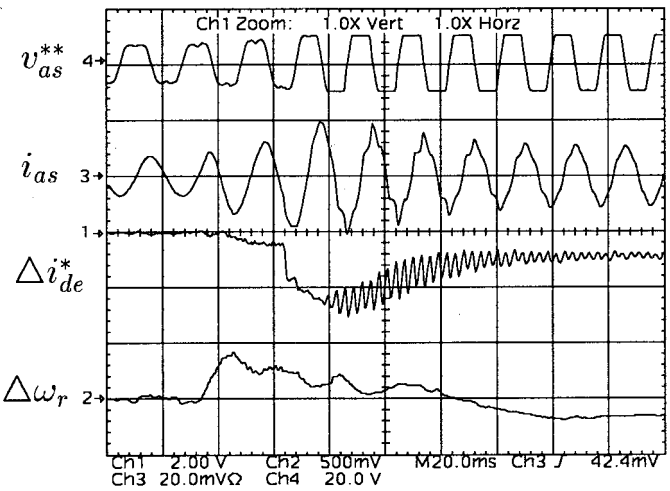

Fig. 27. SVPWM voltage, current, d-axis current error, and speed error. Scales: v_{as}^{**}: 1 V/div; i_{as}: 10 A/div; $\triangle i_{de}^*$: 4 A/div; $\triangle \omega_r$: 60 r/min/div.

VII. Conclusions

Dynamic overmodulation and steady-state overmodulation issues are different, and the modulator fundamental gain characteristics are not a sufficient performance measure to evaluate the dynamic overmodulation performance. An elegant approach is the characterization of the reference and modulator output voltage vector angle and magnitude relations. A simple technique provides analytical tools to obtain these characteristics. Each triangle intersection PWM method is shown to have a unique dynamic overmodulation characteristic. The investigation reveals the minimum voltage magnitude error dynamic overmodulation attribute (one-step-optimal) of the SVPWM method, indicating a significant implementation advantage compared to the two methods reported to achieve such performance. In a motor drive, motion quality is more important than rapid current control and the high-performance phase-error regulation approach is superior to the inherent overmodulation characteristics of the modern PWM methods. For intermediate dynamic overmodulation performance, SVPWM provides satisfactory performance, and for high dynamic overmodulation performance, a phase-error regulation method is adapted from the direct digital PWM technique to enhance the dynamic overmodulation characteristics of the triangle intersection PWM methods. In both methods, the antiwindup limiters play an important role in keeping the phase error small and maintaining high dynamic performance. The theoretical modulator characteristics were verified by detailed computer simulations and laboratory experiments.

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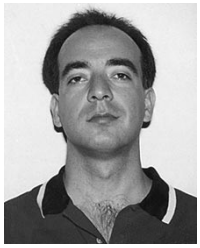

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Seung-Ki Sul (S'78–M'80–SM'98), for a photograph and biography, see p. 51 of the January/February 1999 issue of this Transactions.

Russel J. Kerkman (S'67–M'76–SM'87–F'98), for a photograph and biography, see p. 77 of the January/February 1999 issue of this Transactions.

Thomas A. Lipo (M'64–SM'71–F'87), for a photograph and biography, see p. 486 of the March/April 1999 issue of this Transactions.