A New Modulation Strategy for Improved DC Bus Utilization in Hard and Soft Switched Multilevel Inverters.

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***Abstract*—Multilevel inverters provide an attractive solution for high power, high voltage applications. While the multilevel topology permits higher voltages using devices of lower ratings, the DC link voltage balancing problem is a serious drawback which limits the applicability of multilevel topologies for motor drives. So far, redundant state selection has been the only method for regulating the capacitor voltages which results in a limited voltage capability. A new control strategy to improve the DC bus utilization, while generating low THD voltages is introduced. The proposed scheme is independent of the type of multilevel inverter topology and can be used for both hard and soft switching inverters. Simulation results are presented to demonstrate the validity of control scheme.**

I. INTRODUCTION

Multilevel inverters (MLIs) are an extension of the conventional voltage source inverter topology. They differ in that that additional intermediate DC nodes are brought out and can be switched to the output phases. Fig. 1 shows a phase leg of a hard switched and a proposed soft switched (active clamped resonant) three level inverter with a chopper circuit to stabilize the neutral voltage.

MLIs are characterized by a greater number of devices, reduced switch utilization, DC link voltage balancing problems, improved output voltage THDs and increased voltage ratings. The latter two advantages make the MLI well suited for utility applications such as a static var compensator where the possibility of eliminating the linking transformer can result in considerable cost savings.

MLIs are also being investigated for drive applications where the advantages of multilevel inverter topologies has led to considerable interest primarily for MVA rated drives where MLI voltage capabilities can be best utilized. Three level inverter based drives have been extensively investigated [1-4]. In addition, 4 and 5 level inverter based drives have been reported [5-8]. In all cases, the diode clamped inverter topology has been considered, which is derived from the neutral point clamped inverter topology first proposed by Nabae et. al [9]. Subsequently, alternate topologies such as the flying capacitor topology and the imbricated cells topology [10] were proposed. A partially active rectifier topology was also discussed in [11] and innovative three level topologies can be found in [12,13]. All topologies proposed so far are of the hard switched variety. Recently, however a three level auxiliary resonant commutated pole inverter was proposed in [14].

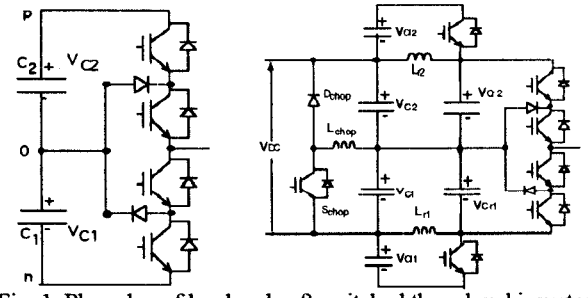

Fig. 1 Phase leg of hard and soft switched three level inverter

A serious constraint in a multilevel inverter based drive is the capacitor voltage balancing problem. Depending on the drive configuration, the DC link voltages can be balanced using alternate strategies. In case of a fully controllable drive, link voltages can be balanced from the rectifier and/or inverter. The rectifier is also made to regulate the input currents so as to minimize the harmonic currents injected into the system [4,5]. In this paper, attention will be focused on the drive topologies which have a unidirectional front end converter i.e. a conventional phase controlled rectifier or a 6*n* pulse diode bridge rectifier. Therefore, link voltage balancing must be effected from the inverter alone since the intermediate DC nodes are not accessible from the rectifier side. This drive configuration has a lower overall silicon kVA and presumably lower cost (though the requirements for front end passive or active filters may negate this advantage).

This work examines in detail the relationship between the voltage generation capability and the DC voltage balancing requirements of the inverter. It will be shown that in order to keep the link voltages balanced, some voltage capability of

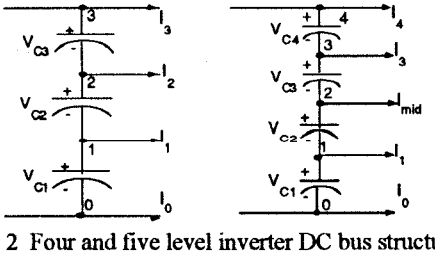

Fig. 2 Four and five level inverter DC bus structure.

the inverter will have to be sacrificed. The exact magnitude of the tradeoff will depend on the number of levels and the type of modulation scheme used. The proposed control scheme arrives at a compromise between the conflicting requirements of higher voltages and the need for balancing the capacitor voltages. Nonetheless, the inverter can be made to generate waveforms superior to those from the corresponding two level VSI but concurrently balancing the DC capacitor voltages.

II. DC LINK VOLTAGE BALANCING

From Fig. 2, generalizing for an n level DC bus, it can be seen that under nominal operating conditions, the capacitor voltages are balanced i.e :

$$V_{C_1} = V_{C_2} = \ldots = V_{C_{n-1}} = V_{DC}/(n-1) \quad (1)$$

The DC currents can be expressed in terms of the phase switching functions and the load currents as :

$$I_k = \delta(h_a - k)i_a + \delta(h_b - k)i_b + \delta(h_c - k)i_c \quad (2)$$

where $h_a, h_b, h_c = 0, 1, \ldots, n-1; \quad k = 1, 2, \ldots, n$

The phase switching functions are determined by the voltage vector required by the modulation process. Fig. 3 shows the available switching states of a four level inverter in the $dq0$ plane. Referring to Fig. 4, as a result of any modulation process, if the reference vector lies within the shaded hexagonal region, it is best approximated by the voltage vector :

$$\bar{V}_{qds} = \frac{V_{DC}}{3}(1 + j\frac{1}{\sqrt{3}}) \quad (3)$$

It is evident that the required voltage vector can be produced by two switching states - i.e. (210) and (321). In the first case, from (2), $I_1 = I_b$, $I_2 = I_a$, $I_3 = 0$ whereas in the second case $I_1 = i_c$, $I_2 = i_b$ and $I_3 = i_a$. In [15], a necessary condition for link voltage balancing was developed as

$$\Delta V_1 I_1 + \Delta V_2 I_2 \geq 0 \quad (4)$$

where $\Delta V_1 = \Delta V_{C_1} = V_{C_1} - \frac{V_{DC}}{3}$, $\Delta V_2 = V_{C_1} + V_{C_2} - \frac{2V_{DC}}{3}$

In (4), $I_1 = I_1(h_a, h_b, h_c)$ etc. i.e. the load DC currents depend on the switching function selected. This principle can be generalized for the n level DC bus and the corresponding necessary condition for charge balancing can be stated as :

$$\Delta V_1 I_1 + \Delta V_2 I_2 + \ldots + \Delta V_{n-1} I_{n-1} \geq 0 \quad (5)$$

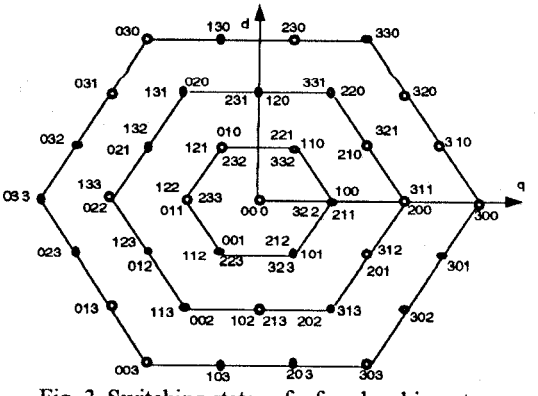

Fig. 3 Switching states of a four level inverter.

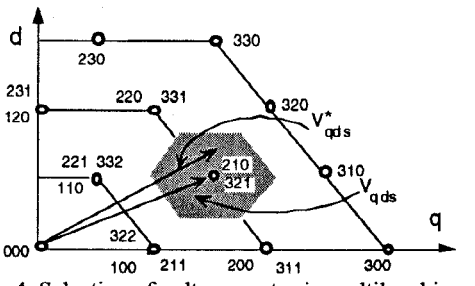

Fig. 4 Selection of voltage vector in multilevel inverter.

Eq. (5) is also a sufficient condition for link voltage balancing only for $n = 3$. For $n \geq 4$, (5) is a relatively weak condition and cannot guarantee that the DC voltages will be balanced. It therefore follows that a necessary condition for link voltage balancing is :

$$min\{\Delta V_1 I_1, \Delta V_2 I_2, \ldots, \Delta V_{n-1} I_{n-1}\} \geq 0 \quad (6)$$

Physically, applying (6) corresponds to selecting that switching state which will not cause an increase in the voltage unbalance. If this condition is consistently applied, it can be seen that starting from balanced conditions, the capacitor voltages stay balanced within a tolerance level.

III. VOLTAGE CAPABILITY OF MULTILEVEL INVERTERS

One of the main advantages of the MLI is that it is able to produce low THD voltage waveforms. This is because the MLI is characterized by a large number of voltage vectors (1 + $3n(n-1)$). The distribution of the voltage vectors is best exemplified by a consideration of the four level inverter switching states in Fig. 3. It is evident that the density of voltage vectors is greatest towards the interior of the hexagon which corresponds to operation at lower modulation depths (at constant DC bus voltage). However, even at higher modulation indices, there are still a large number of voltage vectors which is the primary reason why the THD of the MLI voltages is lower. It is now shown that at higher modulation depths, link unbalance is bound to occur. The magnitude of the unbalance depends on the load power factor and the modulation depth controls the rate at which the unbalance increases. In the following discussion, it will be assumed that a multilevel PWM scheme [16] is used to control the inverter since it is representative of most modulation schemes. Fig. 5 shows the carrier and reference voltage waveforms and phase A switching function for a four level PWM. According to this scheme, the phase A switching functions are given by:

$$h_a = 3 \quad \text{if } v_{a,ref} \geq v_{utr} \quad (7.i)$$

$$= 2 \quad \text{if } v_{utr} \geq v_{a,ref} \geq v_{mtr} \quad (7.ii)$$

$$= 1 \quad \text{if } v_{mtr} \geq v_{a,ref} \geq v_{ltr} \quad (7.iii)$$

$$= 0 \quad \text{otherwise} \quad (7.iv)$$

The phase switching functions of the other two phases are similarly defined. The DC current through node 1 over a fundamental period is a function of the switching states selected and can be expressed as:

$$\langle I_1 \rangle = \int_0^{2\pi} I_1(h_a(\theta), h_b(\theta), h_c(\theta))\, d\theta \quad (8)$$

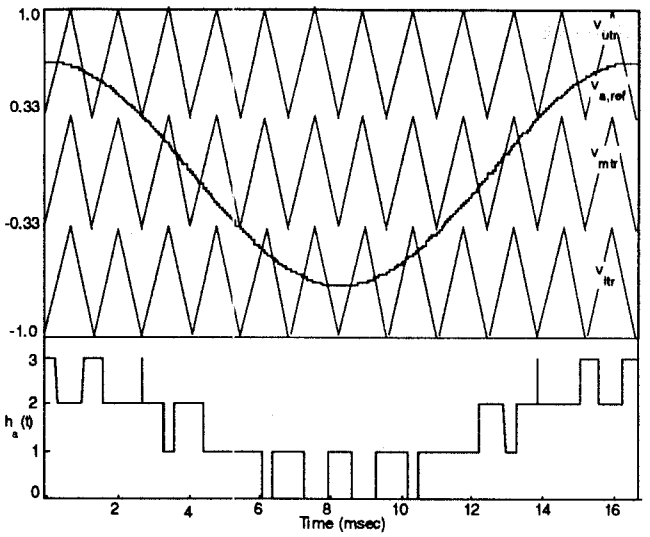

Fig. 5 Four level sine triangle PWM scheme.

Eq. (8) suggests that if one forces $h_a(\theta+\pi) = h_a(\theta) = 1$ when $i_a(\theta+\pi) = -i_a(\theta)$, then $\langle I_1 \rangle = 0$. Thus :

$$I_1(\theta) = \delta(h_a - 1) i_a(\theta) + \delta(h_b - 1) i_b(\theta) + \delta(h_c - 1) i_c(\theta)$$

However, it can be shown that for a carrier based PWM scheme, for frequency ratio $m_f = f_c/f_o$ being an odd integer:

$$\begin{aligned} h_a(\theta) = 1 \Rightarrow h_a(\theta+\pi) = 2; \quad h_a(\theta) = 2 \Rightarrow h_a(\theta+\pi) = 1 \\ h_a(\theta) = 3 \Rightarrow h_a(\theta+\pi) = 0; \quad h_a(\theta) = 0 \Rightarrow h_a(\theta+\pi) = 3 \end{aligned} \quad (9)$$

When $m_f \neq 2k+1$, it is found that $h_a(\theta) = 3 \Rightarrow h_a(\theta+\pi) = 0$ or 1. Hence, it is clear from (8) - (9), $I_1(\theta+\pi) \neq -I_1(\theta)$ and hence $\langle I_1 \rangle \neq 0$. Similar arguments prove that $\langle I_2 \rangle \neq 0$.

The dependence of unbalance on the load power factor angle ϕ is analyzed by considering the case when the reference vector (V_{qds}^*) belongs to a triangle, say the triangle bounded by states (300), (311) and (310), (Fig. 6) . The PWM scheme then produces pulses in the carrier period T such that the reference voltage vector is approximated by the three constituent voltage vectors according to:

$$T\bar{V}_{qds}^* = t_1 \bar{V}_{qds}(300) + t_2 \bar{V}_{qds}(311) + t_3 \bar{V}_{qds}(310) \quad (10)$$

where $T = t_1 + t_2 + t_3$

Assuming balanced three phase reference sinusoids, the reference vector :

$$\bar{V}_{qds}^* = m_a \left(\frac{V_{DC}}{2} \right) (\cos\omega t + j \sin\omega t) \quad (11)$$

where m_a, is the modulation depth defined as :

$$m_a = \frac{V_{ph,pk}}{V_{DC}/2} \quad (12)$$

where $V_{ph,pk}$ is load phase peak voltage. The average DC currents in the carrier period can be expressed as:

$$\langle I_1 \rangle_T = \frac{t_3}{T} \int_{t_k+t_1}^{t_k+t_1+t_3} (i_b(x))\,dx + \frac{t_2}{T} \int_{t_k+T-t_2}^{t_k+T} (-i_a(x))\,dx \quad (13)$$

where t_k is the time instant at the start of the carrier period T. If the load currents can be assumed to be constant over a carrier period, then solving for t_1, t_2 and t_3 in (10) and substituting in (13) :

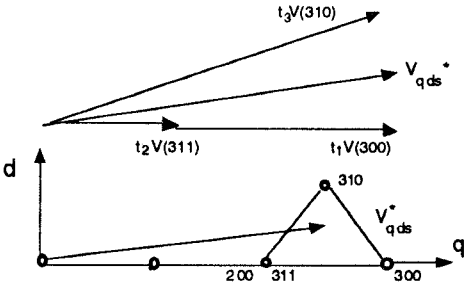

Fig. 6 Reference voltage vector in triangle 1.

$$\langle I_1 \rangle = (3\sqrt{3}/2)\, m_a I_m \,(\cos(\theta-\phi)\cos(\theta-\pi/6) + \sin\theta\cos(\theta-\phi-2\pi/3)) - 3 I_m \cos(\theta-\phi) \quad (14)$$

where I_m is the peak load phase current, $\theta = \omega t$ is the average angle of the reference voltage vector during the carrier period. If the redundant state (200) is selected instead of (311) when the reference vector belongs to the aforementioned triangle 1, the average current $\langle I_1 \rangle$ becomes:

$$\langle I_1 \rangle = \frac{t_3}{T} i_b(\theta) = (3\sqrt{3}/2)\, I_m m_a \sin(\theta)\cos(\theta-\phi-2\pi/3) \quad (15)$$

For a given power factor and reference vector, (15) ≤ (14) for $m_a \leq 1.15$ indicating that redundant state selection may reduce the unbalance. Fig. 7 shows the normalized value of $\langle I_1 \rangle, \langle I_2 \rangle$ as a function of the modulation depth for varying power factors. As expected, for a purely reactive load, the net charge $\langle I_1 \rangle, \langle I_2 \rangle = 0$. For sufficiently high modulation depths, the average charge $\langle I_1 \rangle$ asymptotically approaches 0. This is consistent with the fact that for a high enough modulation depth ($m_a > 1.33$), only S_{30} states i.e. those corresponding to the two level inverter are selected and hence no unbalance can result. At lower m_a, though the tendency to unbalance is greatest many more redundant states are available to quickly redistribute the charge.

Fig. 8 illustrates the effect of varying the carrier frequency. Once again, the dominant unbalancing tendency occurs at lower modulation depths which can be easily remedied by redundant state selection. At higher modulation indices, the tendency to unbalance is not significantly affected by the frequency ratio - hence the carrier frequency can be selected to optimize the voltage THDs and the switching losses rather than balancing the link voltages.

There is an unbalance introduced due to the asymmetric currents being drawn from the capacitors. In the limiting case when only the S_{31}, S_{32} and S_{30} states are used, the

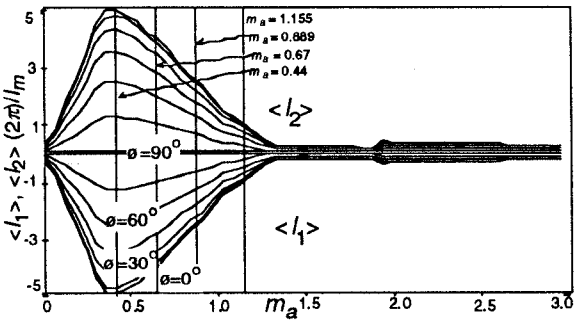

Fig. 7 Average DC currents in a four level inverter vs. modulation depth (power factor ϕ parameter).

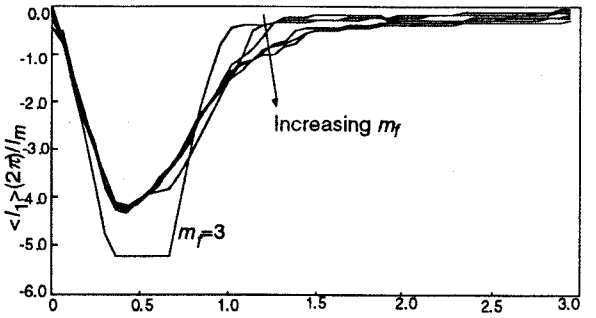

Fig. 8 Effect of carrier frequency on average current $<I_1>$.

average values of the DC currents are given by:

$$\langle I_1\rangle = -\langle I_2\rangle = 6\, I_m \cos\phi \sin(\frac{\lambda}{2})\cos(2\pi/3-\lambda); \qquad (16)$$

where $\lambda = 19.11^\circ$ and thus

$$\langle i_{C2}\rangle = \langle i_{C3}\rangle - \langle I_2\rangle = \langle i_{C3}\rangle - 0.188\, I_m \cos\phi \qquad (17)$$

$$\langle i_{C1}\rangle = \langle i_{C3}\rangle - (\langle I_2\rangle + \langle I_1\rangle) = \langle i_{C3}\rangle \qquad (18)$$

Thus, C_2 tends to discharge faster than the outer capacitors under any modulation scheme for any real load because $\cos\phi \neq 0$. Also, there is symmetry in the charging of V_{C1} and V_{C3}.

In a five level inverter, as indicated in Fig. 9, the tendency of the midpoint of the DC bus to drift is much lower than that of the other two neutrals. Again, at lower modulation indices, the midpoint voltage drift is easily countered by redundant state selection. Also the frequency ratio does not produce significant variations in the unbalancing characteristics. As with the four level case, the effect of frequency ratio on the deviation characteristic is minimal. A feature of the five level (or any odd number of levels) inverter is that the midpoint DC bus voltage does not tend to deviate significantly from the nominal value. Even though redundant state selection may eventually re-balance the capacitor voltages the ripple on the neutral voltage is larger for $n \geq 4$. Therefore, link voltage balancing for $n \geq 4$ differs significantly from the neutral voltage drift control in three level inverters.

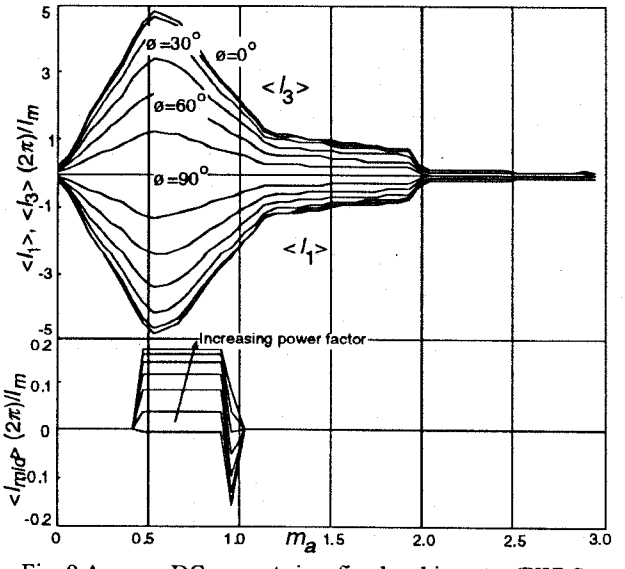

Fig. 9 Average DC currents in a five level inverter (PWM).

IV. MODIFIED SPACE VECTOR SCHEME

In the previous section, it was shown that in the example case of the four level inverter, for higher modulation depths, a net charge is drawn from the intermediate DC nodes which eventually leads to unbalance and shutdown. In this section, an alternate method for balancing the link voltages at higher modulation depths in a four level inverter is developed. As was shown earlier, with increasing modulation depths, there are not sufficient redundant states available for redistributing the charges on the link capacitors. Therefore, it is evident that to improve DC bus utilization two avenues are available:

(i) Use only the outermost voltage vectors i.e. states as (300), (330), (030), (033), (003) and (303). This is equivalent to a two level operation of the inverter and does not make use of the low voltage THD capability of the inverter.

(ii)Make use of only those voltage vectors which produce appropriate capacitor currents.

The latter approach is based on the observation of (18) that the innermost capacitor C_2 tends to discharge most rapidly whereas C_1 and C_3 charge up to half the DC bus voltage. Hence use must be made of those switching states which can constantly regulate the C_2 capacitor voltage. The S_{21} states [15] are precisely those switching states which permit the transfer of charge from the outer to the inner capacitors. Therefore, as with the conventional space vector schemes, appropriate triangular regions are delineated as shown in Fig. 10. The reference voltage vector defined in (12) lies in one of the identified 18 regions for modulation depths ≥ 0.77. Simulation studies indicate that conventional sine triangle PWM schemes work satisfactorily for modulation depths $m_a \leq 0.7$-0.75 depending on the load conditions. The space vector scheme is implemented by generating the dwell times at the voltage vectors forming the vertices of the triangle to which the voltage vector belongs. (Fig. 11). Thus :

$$\bar{V}^*_{qds} = \frac{1}{T}\left(t_1\bar{V}(300) + t_2\bar{V}(210) + t_3\bar{V}(330)\right) \qquad (19)$$

where $t_1 + t_2 + t_3 = T$ and T = computation interval. The dwell times in this particular instance can be calculated as:

$$t_1 = T\ 1.5\, m_a \cos(\theta^*) \qquad (20.i)$$

$$t_2 = T\ (3 - 2.5981\, m_a \cos(\theta^* - \pi/6)) \qquad (20.ii)$$

$$t_3 = -T\ (2 + 1.5\, m_a \cos(\theta^* - \pi/3)) \qquad (20.iii)$$

where θ^* is the angle made by the reference voltage vector

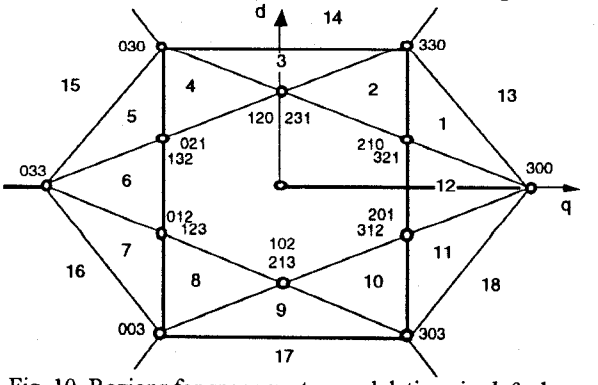

Fig. 10 Regions for space vector modulations in *dq0*-plane.

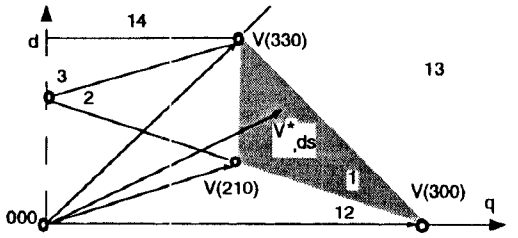

Fig. 11 Space vector implementation.

with respect to the q-axis in the $dq0$ plane. The balancing criterion (6) is used to determine which of the S_{21} states is to be used. The duty ratios when the reference belongs to the other regions can be similarly worked out. Determining to which region the reference belongs is computationally intensive but the overhead can be minimized for non current regulation (vector control) schemes. Referring to Fig. 11, if $V_{qds}^*(kT)$ belongs to region 1, $V_{qds}^*((k+1)T)$ can lie either in region 1, 13, 2 or 14. This reduces the number of regions to be considered from 18 to 4. Unlike the four level PWM scheme, not all voltage vectors of the four level inverter are used. However, the primary advantage of this scheme is that the size of the triangles being small, the harmonic content of the output voltages is still low. It should be pointed out that though it is possible to create other regions (similar to Fig. 10) - the shapes of such region are either more irregular (higher THDs) or do not contain states producing desirable capacitor charging currents. The prosposed scheme has been verified by simulations and is being currently tested in a hardware implementation of a drive. The load is a 230V/460V, 8 pole 15HP induction motor.

Fig. 12 shows the inverter pole voltage, the motor phase voltage and current for 0.5 rated torque and f_c = 90Hz. The computation frequency ($1/T$) is 720Hz. Fig. 13 shows the dq voltage vectors selected at the same operating point by the PWM and the space vector schemes. Though the THD is degraded with the space vector scheme as opposed to the PWM scheme, voltage balancing cannot be effected at such high modulation depths using the latter.

In the drive implementation, for $m_a \leq 0.7$ conventional PWM is used because sufficient redundant states are for balancing the voltages. As the commanded voltage increases,

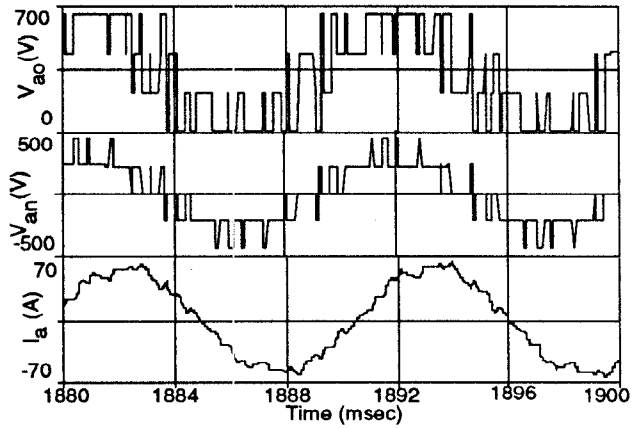

Fig. 12 Inverter pole voltage, motor phase voltage and current with modified space vector scheme.

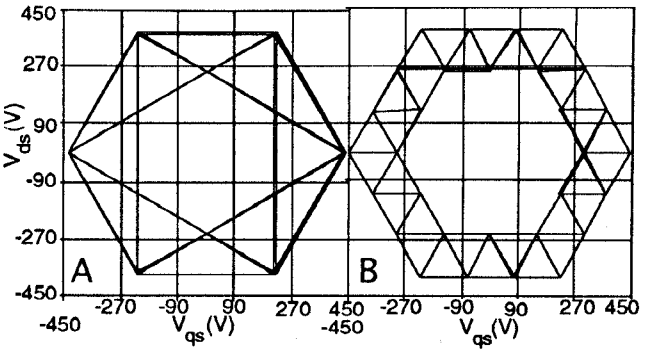

Fig. 13 Voltage vectors at same operating point (A) : Space vector scheme, (B) : Four level PWM

the modified space vector scheme is invoked whenever the voltage unbalance exceeds a pre-defined limit (typically 5%). This limit should be greater than the maximum unbalance that the PWM scheme can correct by redundant state selection. By ensuring that the changeover from the PWM to the space vector scheme occurs at the end of a carrier period the resulting transients can be minimized. Fig. 14 illustrates the balancing of the link voltages under such a condition.

At very high modulation depths (field weakening region of induction motor), the four level space vector modulation makes a seamless transition to two level space vector modulation. This is a very attractive benefit of the proposed scheme. Fig. 15 shows the load phase voltage and current under near two level modulation case at f_o=120Hz. The transition from space vector to a four level PWM scheme occurs when the capacitor voltage unbalances are within limits and $m_a \leq 0.67$ (for heavy loads) and $m_a \leq 0.77$ (light loads). This difference accounts for the variation in balancing capabilities of the inverter with load power factor. Reverting to four level PWM once the DC voltages are rebalanced by space vector modulation, though possible is not desirable at heavy loads since the link voltages are promptly driven back into unbalance.

The spectral performance of the proposed scheme is intermediate between the conventional two level inverter and the four level inverter PWM. Fig. 16 illustrates the motor phase current spectrum under 4 level PWM, space vector modulation and with conventional two level PWM. In every

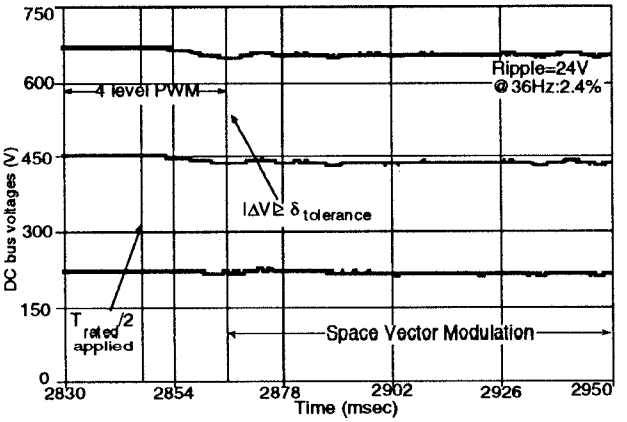

Fig. 14 Link voltage balancing at transition from PWM to space vector modulation scheme.

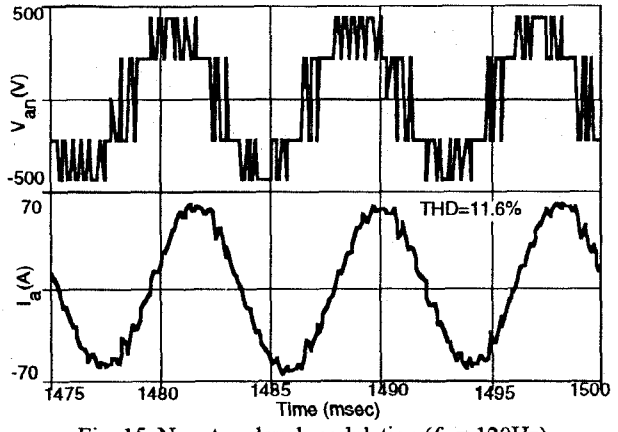

Fig. 15 Near two-level modulation (f_o = 120Hz)

case, the modulation depth was adjusted to yield a constant fundamental voltage of 230V at 90Hz. The computation step size was selected to yield the approximately same average switching frequency as in the two level inverter case.

Analogous to the conventional space vector modulation schemes, further optimizations in the proposed space vector method are possible. However, the absence of any switching state common to all regions differentiates space vector modulation from the conventional space vector scheme. A property of the multilevel space vector is that the device switching frequency is a sub-multiple of the computation frequency. This offers yet other avenue for optimization in multilevel control.

V. CONCLUSIONS

In this paper, limitations of conventional multilevel modulation schemes have been demonstrated. A new space vector based modulation strategy is proposed which improves the DC bus utilization and reduces the harmonic distortion. Though demonstrated for the four level inverter is completely general and easily extended to *n*-levels. The proposed scheme can be implemented on both hard switched and PWM type of soft switched multilevel topologies. Space vector control method adds to the complexity to multilevel inverter control. However, the transition from one control regime to another is smooth. For practical applications inverter design as well as hardware implementation issues become important and will be the subject of a future publication. This modulation scheme has overcome a serious drawback of conventional multilevel inverter implementation which should improve the viability of multilevel inverter based drives. This approach also lends itself to low frequency modulation schemes - an attractive feature for static var compensation applications.

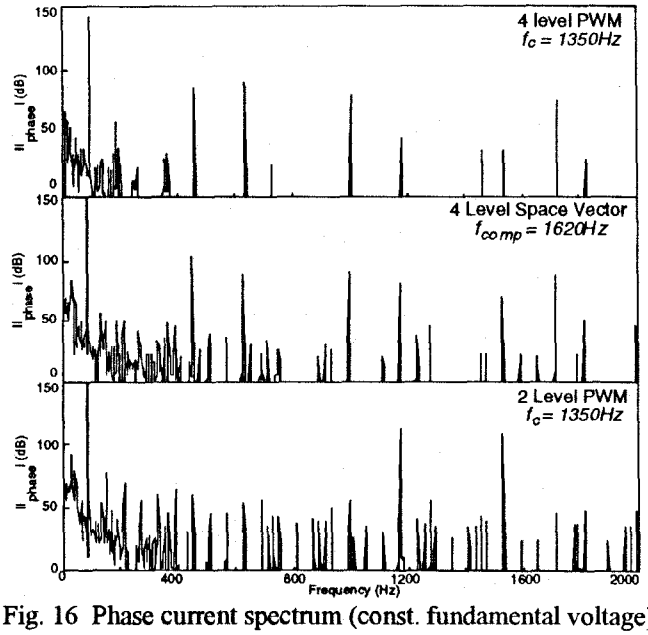

Fig. 16 Phase current spectrum (const. fundamental voltage)

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