DC Link Voltage Control of Reduced Switch VSI-PWM Rectifier/Inverter System

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Abstract **- Three-phase to three-phase VSI-PWM rectifier and inverter system with eight switches has many advantages, capability of unity or even leading power factor, sinusoidal input current waveforms, bidirectional power flow. This paper derives a mathematical model of the dc link voltage control for the system. The transient model for overall and difference voltages of split capacitor dc link is developed, and typical simulated and experimental results for dynamic responses are presented to illustrate important performance characteristics to verifiy the developed model.**

I. INTRODUCTION

Improvements in power semiconductor switching technology have significantly reduced the cost and size of ac drives and improved waveform quality. Recently there has been growing interest in low cost ac drives to meet the needs for reducing cost. A number of low cost topologies have been suggested for single-phase to three-phase[1]-[6] or three-phase to three-phase voltage source inverter[7]-[9]. There are a variety of names for these inverters, i.e. inverter system with a reduced switch count, component minimized or B4 inverter, split capacitor dc link inverter, and four switch three-phase inverter.

Van der Broeck et. al. suggested a method of generating the three-phase waveforms with two dc link voltages and discussed the harmonic effects and [1], [2]. The modulation strategy suggested can produce three phase balanced sinusoidal waveforms at a reduced output voltage of 0.866 compared with the conventional six switch inverter. In another topology proposed by Enjeti et. al., the diode bridge rectifier is replaced by a single-phase current controlled rectifier employing two switches and two capacitors[4], [5]. Covic et. al. proposed the new voltage control scheme, which enables unity power factor and an improved dc link voltage control independent of input voltage fluctuations[6]. However, the sinlge-phase rectifier has a limitation for high power applications because power flow is not constant, therefore, requires a much larger capacitance in the dc link, which makes system performance sluggish.

G. T. Kim et. al. proposed a three-phase to three-phase VSI-PWM rectifier and inverter structure with eight switches, and discussed feasibility and operational limitations of the proposed structure[7]. The proposed converter uses two identical inverters with four power switches both for a rectifier and for a inverter, and a two split capacitor dc high voltage link as shown in Fig. 1. F. Blaabjerg et. al. suggested adaptive space vector modulation(SVM) to compensate dc link voltage ripple[8], and D. T. W. Liang suggested flux vector modulation strategy[9].

The main advantages of this structure are: 1) capability of unity or even leading power factor, 2) sinusoidal input current waveforms reducing harmonic pollution, 3) bidirectional power flow. Despite of these advantages, the main shortcomings are: 1) increased voltage stress both on the power devices and on induction machine, 2) voltage fluctuation of split capacitor dc link due to the incomplete decoupling of inverter and rectifier.

This paper derives a mathematical model of the dc link voltage control for the three-phase to three-phase VSI-PWM rectifier and inverter structure with eight switches. The transient model for overall and difference voltages of split capacitor dc link is developed, and typical simulated and experimental results for dynamic responses are presented to illustrate important performance characteristics to verifiy the developed model.

II. PRINCIPLES AND OPERATION OF SYSTEM

Fig. 1 shows the circuit diagram of three-phase to three-phase rectifier/inverter system with a reduced switch count. The leakage inductances of the induction motor are shown to emphasize the symmetric structure of the converter. The important features of this structure are the placement of the inductances on the input side for the boost operation of the rectifier and the placement of the capacitance in the dc link. Some ac line inductances are needed because Ldi/dt voltage form an essential element in forcing the currents track current references and dc link capacitors act as dc voltage sources and provide filtering operation. For proper operation, the dc link capacitor voltage must be sufficiently higher than the peak line-to-line voltage of ac main source and counter emf of ac motor for the

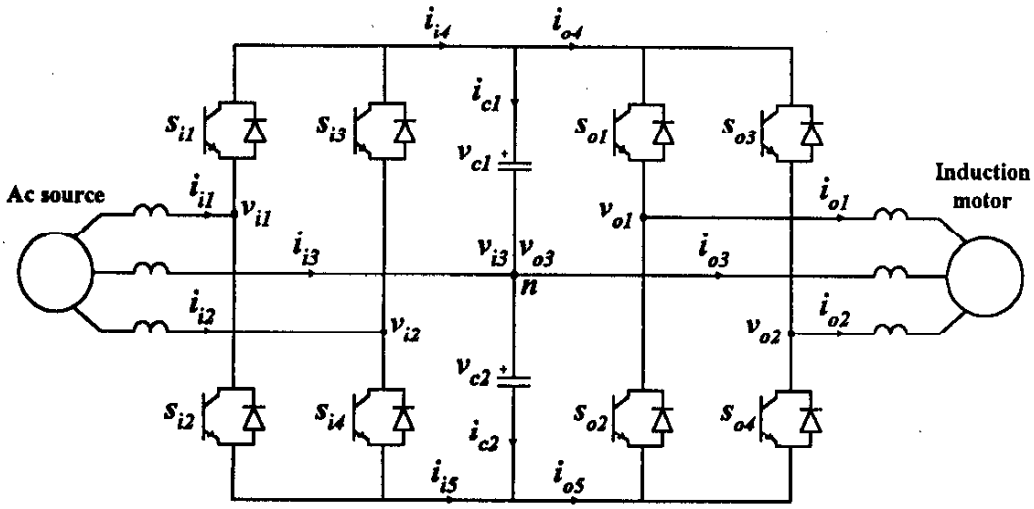

Fig. 1 Rectifier/inverter system with a reduced switch count

back-bias of the anti-parallel diode and for the current controllability without current distortion.

The configuration incorporates an active rectifier structure that provides an active input current wave shaping feature and allows bidirectional power flow with four switches. A four switch inverter with the split capacitors in the dc link provides balanced three phase output to ac motor at adjustable voltage and frequency. An ac input is then connected to the two PWM voltages of rectifier and the center point of two split capacitors. A three phase ac motor is also connected to the ouput inverter and the same center point.

The split capacitor bank is charged initially to the peak value of input line-to-line voltage through the diodes in S_{i1}-S_{i4}. The switches operate on a PWM pattern to shape the input currents to follow the current references. The filter inductors provide current filtering and voltage boost operation. The center point of the split capacitor link forms the third phase both for the rectifier and inverter. The output inverter can be operated either by voltage control or by current control. Fig. 2 shows the sinusoidal PWM voltage control for the inverter, and Fig. 3 shows the hysteresis current control for the rectifier.

The input current references are taken from the ac mains through voltage transformers. The phase voltages of ac mains are introduced for unity power factor input current reference and multiplied by the output of the outer loop dc link voltage controller (magnitude of input current is determined to maintain constant the dc link voltage) to form the current reference template waveforms as shown in Fig. 4. The current of uncontrolled leg is also automatically sinusoidal, because there is no connection of the neutral point. One sees that the ac source and induction motor are not completely decoupled because one input leg and one output leg are connected directly with two dc link capacitors.

The inverter or rectifier operates in one of four nonzero voltage vectors. If balanced three phase sinusoidal waveforms are required, the maximum circular locus results in 0.866 compared with the conventional six switch inverter. The third harmonic injection technique cannot be applied because no zero sequene voltage vector is available.

A dc bus center point is assumed to be the ground reference. The line to ground voltages are uniquely determined by the PWM inverter switching according to the voltage or current controller. There is no zero voltage vector, therefore, the switching frequency of the four-switch inverter is somewhat higher than that of the conventional six-switch one, in which six nonzero voltage vector and two zero vectors are available. Both of the dc link capacitor voltages must be higher than the peak value of input and output line-to-line voltages for current controllability, respectively. Thus, the overall dc link voltage of the four-switch inverter must be twice as high as that of the six-switch one.

III. DYNAMIC MODEL OF VOLTAGE CONTROL

For the four-switch inverter or rectifier, the switching functions can be stated as follows. Given a desired set of three phase voltages for the output inverter:

$$v_{o1} = V_o \sin(w_0 t)$$
$$v_{o2} = V_o \sin(w_0 t - \frac{2\pi}{3}) \quad (1)$$
$$v_{o3} = V_o \sin(w_0 t + \frac{2\pi}{3})$$

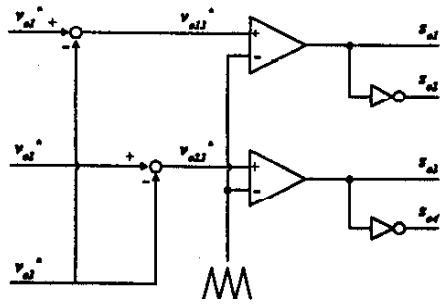

Fig. 2 Sine PWM for inverter voltage control

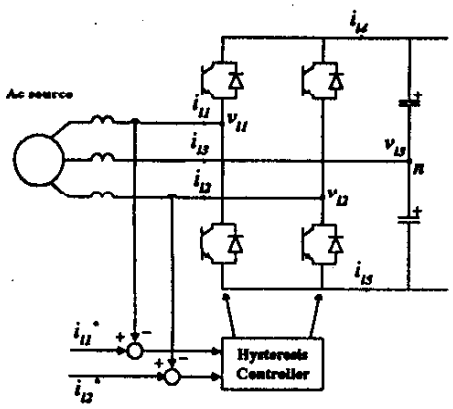

Fig. 3 Hysteresis current control for PWM rectifier

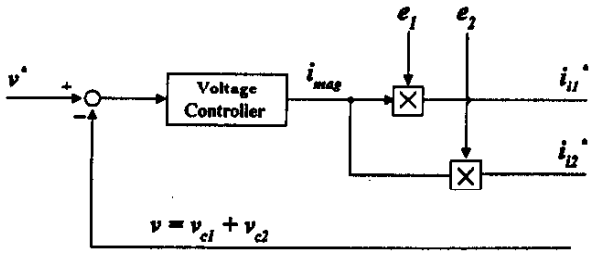

Fig. 4 Current reference generation for PWM rectifier

where, V_o is the magnitudes of the output phase voltages. Determine the switching matrix [S] that will produce a desired set of line-to-ground voltages

$$v_{o1n} = v_{o1} - v_{o3} = \sqrt{3}\, V_o \sin\left(w_0 t - \frac{\pi}{6}\right)$$
$$v_{o2n} = v_{o2} - v_{o3} = \sqrt{3}\, V_o \sin\left(w_0 t - \frac{\pi}{2}\right) \quad (2)$$

$$\begin{bmatrix} v_{o1} \\ v_{o2} \end{bmatrix} = \begin{bmatrix} S \end{bmatrix} \begin{bmatrix} v_{c1} \\ -v_{c2} \end{bmatrix} \quad (3)$$

where, n is the dc bus center point assumed to be ground. One can see that the phase difference between two line-to-ground voltages is 60°. The above equation can be solved as follows

$$\begin{bmatrix} S \end{bmatrix} = \begin{bmatrix} S_1 & S_2 \\ S_3 & S_4 \end{bmatrix} \quad (4)$$

$$S_1 = 0.5[1 + a_0 \sin(w_0 t - \frac{\pi}{6})]$$
$$S_2 = 0.5[1 - a_0 \sin(w_0 t - \frac{\pi}{6})]$$
$$S_3 = 0.5[1 + a_0 \sin(w_0 t - \frac{\pi}{2})] \quad (5)$$
$$S_4 = 0.5[1 - a_0 \sin(w_0 t - \frac{\pi}{2})]$$

The switching function is based on the assumtion of $v_{c1} = v_{c2} = V$. The overall control block diagram describing the split capacitor dc link, inverter, and load is shown in Fig. 5. Each element in Fig. 5 is as follows.

To describe the overall dc link voltage $v = v_{c1} + v_{c2}$, and the voltage difference $v_d = v_{c1} - v_{c2}$, the following transformation matrices are introduced.

$$\begin{bmatrix} v \\ v_d \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} v_{c1} \\ v_{c2} \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} v_{c1} \\ -v_{c2} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v \\ v_d \end{bmatrix} \quad (7)$$

Therefore, the relation $[T_1]$ between v_{c1}, v_{c2} and v_{o1}, v_{o2} will be

$$\begin{bmatrix} T_1 \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (8)$$

The load model is three phase ballanced RL with counter emf as shown in Fig. 5, and dq coordinate transformation is introduced.

$$\begin{bmatrix} T_2 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} T_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (10)$$

The inverter input currents i_{o4}, i_{o5} are related with the output currents i_{o1}, i_{o2} by the transpose of the switching matrix.

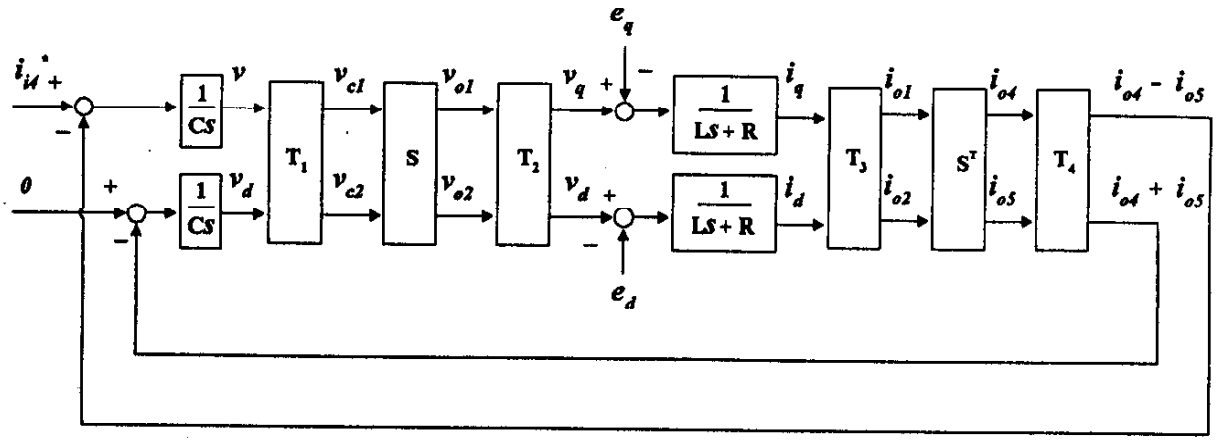

Fig. 5 Block diagram of split dc link and inverter

$$\begin{bmatrix} i_{o4} \\ i_{o5} \end{bmatrix} = \begin{bmatrix} S \end{bmatrix}^T \begin{bmatrix} i_{o1} \\ i_{o2} \end{bmatrix} \tag{11}$$

From Fig. 1 the overall dc link voltage v, and the voltage difference v_d can be expressed by

$$\begin{aligned} v &= v_{c1} + v_{c2} \\ &= \frac{1}{C}\int(-i_{o4})dt + \frac{1}{C}\int(-i_{o5})dt \\ &= -\frac{1}{C}\int(i_{o4} - i_{o5})dt \end{aligned} \tag{12}$$

$$\begin{aligned} v_d &= v_{c1} - v_{c2} \\ &= -\frac{1}{C}\int(i_{o4} + i_{o5})dt \end{aligned} \tag{13}$$

Thus, the relation $[T_4]$ between i_{o1}, i_{o2} and i_{o4}, i_{o5} will be

$$\begin{bmatrix} i_{o4} - i_{o5} \\ i_{o4} + i_{o5} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} i_{o4} \\ i_{o5} \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} T_4 \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \tag{15}$$

The equations (8)-(15) are combined to be eq. (16). The overall control block diagram can be expressed as shown in Fig. 6.

$$\begin{bmatrix} T_1 \end{bmatrix}\begin{bmatrix} S_1 \end{bmatrix}\begin{bmatrix} T_2 \end{bmatrix}\begin{bmatrix} T_3 \end{bmatrix}\begin{bmatrix} S_2 \end{bmatrix}\begin{bmatrix} T_4 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}$$

$$a_{11} = a_0^2, \quad a_{22} = \frac{4}{3} \tag{16}$$

$$a_{12} = a_{21} = \frac{2}{\sqrt{3}} a_0 \sin(w_0 t - \frac{\pi}{3})$$

IV. VOLTAGE CONTROLLER

Fig. 6 shows that the control system is a coupled system., and v and v_d affect each order. A set value for v, the sum of two capacitor voltages, should be greater than double the peak line-to-line voltages in order to control voltages and currents without distortion, whereas that of v_d is zero.

Fig. 7 shows the control blockdiagram of v, where the controller output is i_{mag} in Fig. 4. In order to control v various controllers such as a PI controller can be applied, and feedforward compensation by measuring the output power can be added to the controller output to improve the control performance. The controller output is, in effect, the magnitude of the input currents in phase with the input phase voltages, which is the required power by the capacitors to maintain the dc link voltage constant. There is a disturbance of double the output frequency due to a_{21} and v_d, because a_{21} and v_d have output frequency components.

Fig. 8 shows the control blockdiagram of v_d and one can see that the system is asymtotically stable, so v_d will go zero and no control for v_d is needed. There exists a disturbance of the output frequency due to a_{12} of eq. (16) and the transfer function of output freequency is as follows

$$\frac{V_d(s)}{D_2(s)} = \frac{3}{3LCs^2 + 3RCs + 4} \tag{17}$$

the voltage fluctuation of v_d should be suppressed for current controllability by designing RLC within the output operating frequency range. It can be observed that in case of zero or very low output frequency operation the voltage fluctuations of capacitance are too high to satisfy the requirement that each capacitor

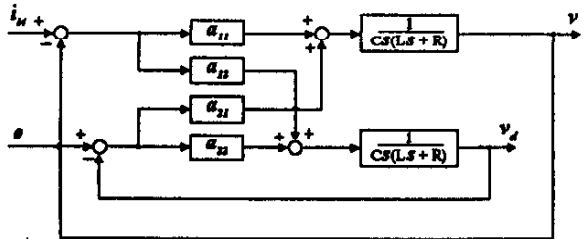

Fig. 6 Simplified blockdiagram of Fig. 5

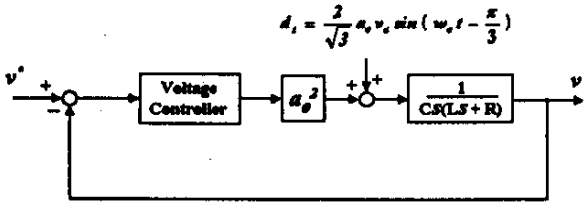

Fig. 7 Dc link voltage control blockdiagram

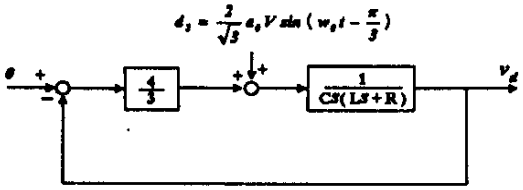

Fig. 8 Dc link voltage difference control blockdiagram

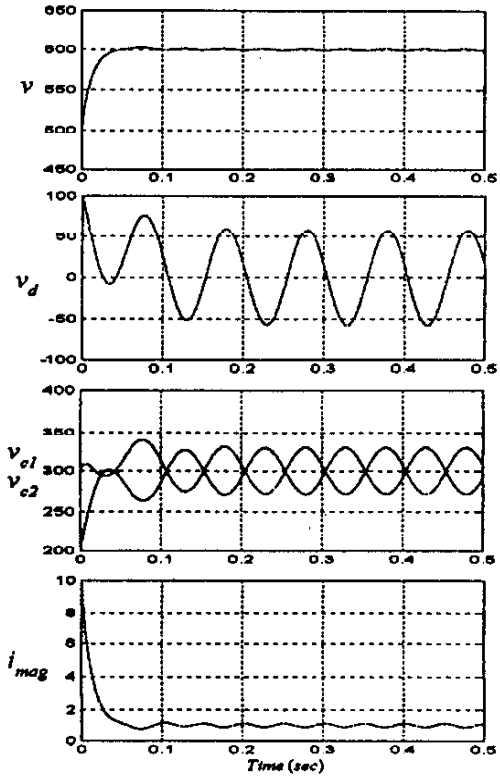

Fig. 9 Simulated waveforms of voltage control

voltage must be greater than the peak line-to-line voltage even if the overall dc link voltage can be maintained constant. Thus the lower limit of output frequency must be bounded

Fig. 9 shows the simulated waveforms from initial condition v=500V, v_d=100V. v reaches a set value 600V, and v_d goes to zero and shows the flucuation. v_d flucuates with the output frequency, whereas v and imag with double the output frequency.

V. EXPERIMENTAL RESULTS

A 1kVA prototype was contructed using 600V, 15A IGBT IPM module, two 2000F capacitors, and three 3mH inductors. A set of reduced input voltages was used by a input transformer. A 1kW induction motor was used as a load of the inverter. The output inverter was operated by the sine triangle PWM and the rectifier was operated by the current hysteresis control. TI TMS320C31 DSP processor was used for the control of the overall system. The sampling time for the voltage control and the current hysteresis control was 40μsec. The dc link capacitance voltages are charged initially to the voltage of a three phase full bridge diode rectifier.

Figs. 10-13 show the experimental waveforms of voltages and currents of the rectifier/inverter system to illustrate the transient responses. Time division is 0.5 sec/div., voltages 200V/div., currents 10A/div.

Fig. 10 illustrates the transient waveforms of the dc link voltages and input currents for the initial voltage build up. One sees that the magnitude of input current, which is the output of the voltage PI controller, changes according to the reference voltage, and that the dc link voltage follows the voltage command. In Fig. 10 i_{in} is a waveform through a low pass filter, and has a almost same waveform of controller output i_{mag}. It is seen that the dc link voltage is self supporting through the charge of the filter capacitance.

Fig. 11 shows the same waveforms according to inverter starting and Fig. 12 the change of the reference voltage with motor running, and Fig. 13 the change of the load. One sees that the controller works well and the rectifier/inverter system with eight switches shows excellant performance and can challenge the conventional twelve switch system.

VI. CONCLUSION

In this paper, This paper derives a mathematical model of the dc link voltage control for the three-phase to three-phase VSI-PWM rectifier and inverter system with eight switches. The transient model for overall and difference voltages of split capacitor dc link is developed. The control system is a coupled system and

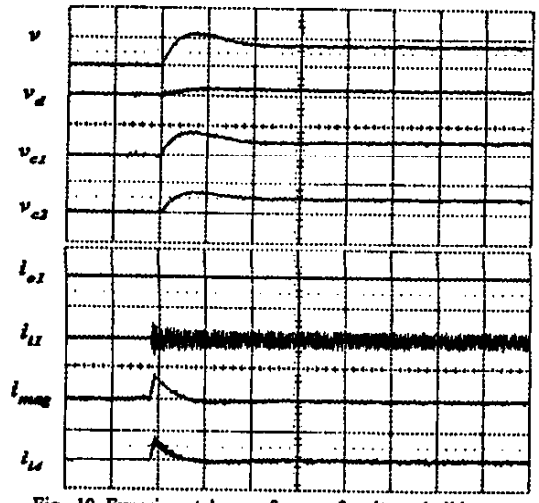

Fig. 10 Experimental waveforms of voltage build up

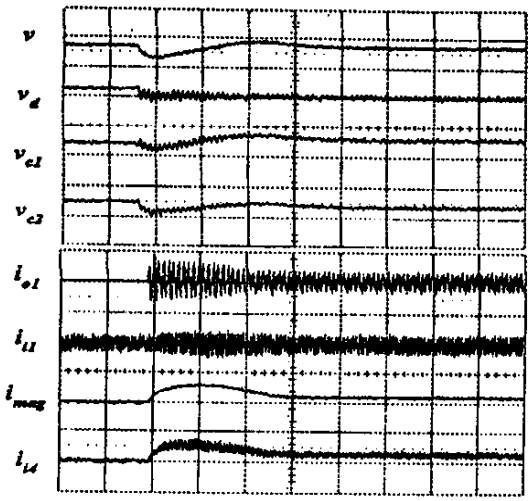

Fig. 11 Experimental waveforms of inverter starting

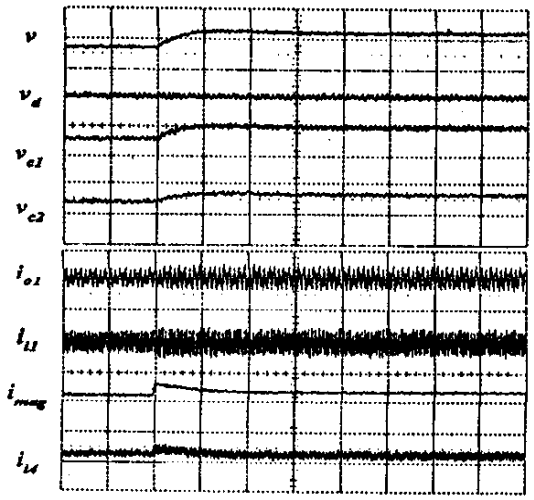

Fig. 12 Experimental waveforms of voltage reference step change

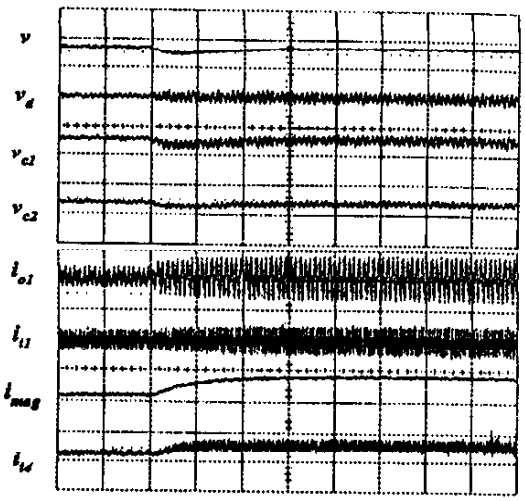

Fig. 13 Experimental waveforms of load disturbance

the system for v_d is asymtotically stable, so v_d will go zero and no control for v_d is needed. Typical simulated and experimental results for dynamic responses are presented to illustrate important performance characteristics to verifiy the developed model.

VII. REFERENCES

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