Rectifier Current Regulation in Four Level Drives

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***Abstract*—A four level drive system utilizing an active four level rectifier has been recently proposed. This paper outlines the strategy for the rectifier control of such a system. A new switching scheme for concurrently balancing the link voltages and drawing unity power factor input currents is introduced. The proposed control scheme is dynamic and does not use lookup tables. Simulation results are used to verify the performance for a variety of load conditions.**

I. INTRODUCTION

Multilevel inverter drives are based on the neutral point clamped (NPC) inverter topology first proposed by Nabae, Takahashi and Akagi [1]. Bhagwat and Stefanovic [2] demonstrated the possible advantages of a multilevel converter topology. The NPC topology has some attractive features such as reduced voltage THDs, higher voltages using devices of lower ratings and reduced dv/dt stresses. Attention so far has been largely restricted to high voltage applications such as static var compensation though three level drives have been increasingly investigated [3-6] for high power drives and in [7], a four level drive was proposed. The reduced dv/dt stresses are significant when EMI is considered. Also, with a reduced voltage step size, the multilevel waveform leads to a reduced motor terminal overvoltage stresses thereby increasing motor reliability

Three distinct multilevel inverter topologies have been proposed viz. the diode clamped inverter topology, the *'flying capacitor'* topology and the topology utilizing modular H-bridges with separate DC capacitors [8]. The merits of the main topologies has been adequately discussed in [9]. For drive applications, the diode clamped inverter topology (DCMLI) is the most suitable. Consequently, only the DCMLI topology is discussed further. It is clear that four level inverters can attain higher voltages than three level inverters. The only added converter kVA penalty arises from the greater number of clamp diodes. Four level converter based drives might prove suitable for traction applications where higher voltages are a distinct advantage.

In high power drives, the harmonic current injection problem rapidly becomes a dominating concern and with the advent of the IEEE-519 harmonic standard, a desirable property of a drive is to keep the input harmonic current content low. Several options exist for a multilevel inverter drive to be interconnected with the AC system viz. (i) a conventional two level diode bridge rectifier with tuned input filters. (ii) an active two level active rectifiers. (iii) a partially active four level rectifier based on [10] (iv) a fully active four level rectifier.

In this paper, we concern ourselves only with the fourth solution. A practical motivation for this is that the fully active four level rectifier provides the most degrees of freedom in balancing the link voltages. In addition, with a fully active four level rectifier, it will be shown that the voltage boost required can be minimized so that device ratings can be reduced improving the cost advantage.

MLIs have a serious drawback in that that the DC link capacitor voltages tend to drift from the nominal values. In static var applications where the power flow is predominantly reactive, the link voltages tend to stay balanced. However, in a drive application where the power flow is both real and reactive, in the absence of an explicit control strategy, the link voltages vary considerably, typically resulting in voltage inversion causing large device stresses and degradation in waveform quality finally leading to system shutdown.

The DC capacitor voltages can be balanced under certain conditions by using the redundant states. This approach has been incorporated in a 3 level drive control largely by the use of lookup tables. As compared to a two level inverter, the MLI control thus is more complex. Reducing control complexity would make the MLI based drives more feasible.

This paper demonstrates a viable control strategy whereby the active rectifier can be used not only to balance the link voltages but also to draw unity power factor utility currents. The rectifier switching scheme is then able to handle bi-directional real power flow. So far, DC voltage balancing has not been satisfactorily discussed for the case when real power is drawn from the inverter.

II. A FOUR LEVEL INVERTER BASED MOTOR DRIVE

A. Four level drive configuration

The four level drive studied (fig.1) consists two fully controllable, IGBT based four level diode clamped converters. The inverter drives a three phase, 460 V, wye connected, 100 HP induction motor with a fan load. The inverter is modulated using a four level sine triangle PWM scheme based on [11]. Occasional redundant state selection

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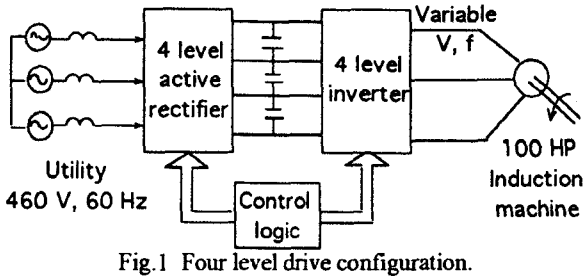

Fig.1 Four level drive configuration.

from the inverter is effected to aid the voltage balancing. The system is similar to the one proposed in [12] except that the front end is an active four level rectifier. The objectives of the four level drive is threefold - (i) To balance the link voltages. (ii) To supply the induction motor with optimal voltage waveforms. (iii) To draw unity power factor currents. The inverter control is left unconstrained so that there is ample scope to optimize the inverter modulation. The rectifier then has to balance the link voltages and concurrently regulate the input current. Rectifier control is thus the focus of this work.

B. Terminology

A terminology for four level converters is developed in this section. Referring to fig.2, it is seen that the converter is modeled as a set of three single pole four throw switches. The pole voltages then are defined as:

$$v_{uo} = \delta(h_u - 1)V_{C1} + \delta(h_u - 2)(V_{C1} + V_{C2}) + \delta(h_u - 3)(V_{C1} + V_{C2} + V_{C3}) \quad (1)$$

Here h_u is the phase U switching function and $\delta(.)$ is the Dirac delta function. Phase V and W pole voltages are expressed similarly. The use of switching functions enables compact algebraic evaluation for rectifier control algorithm. and also permits writing the converter DC currents as:

$$i_{rj} = k\left(\delta(h_u - j)i_u + \delta(h_v - j)i_v + \delta(h_w - j)i_w\right);\ j = 1,2,3 \quad (2)$$

where $k = 1$ for the rectifier and $k = -1$ for the inverter DC currents. The capacitor currents are then expressed as:

$$i_{C3} = i_{r3} - i_{i3};\ i_{C2} = i_{r2} - i_{i2} + i_{r3} - i_{r3};\ i_{C1} = i_{i2} - i_{r1} \quad (3)$$

C. The four level converter switching states

In general, the n level converter has n^3 switching states and $1 + 3n(n-1)$ voltage vectors. The four level inverter is

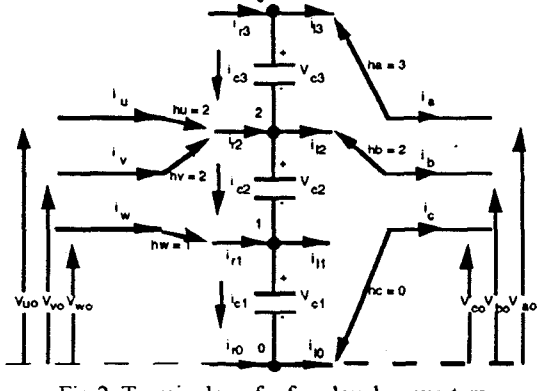

Fig.2 Terminology for four level converters.

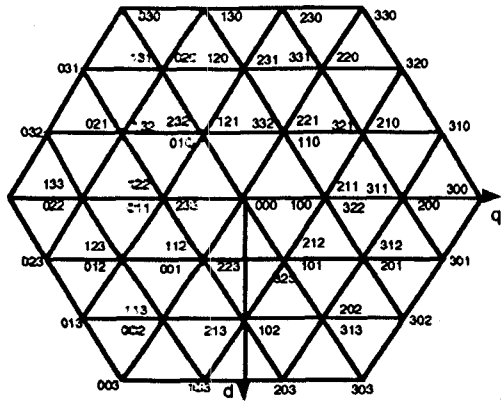

Fig.3 Switching states of 4 level converter.

characterized by 37 nominally distinct voltage vectors and 64 switching states. These vectors and switching states are located in the $dq0$ plane (fig.3) by using the dqn transformations given by:

$$q(h_u, h_v, h_w) = \frac{2}{3}\left(h_w - \left(\frac{h_u + h_v}{2}\right)\right);\ d(h_u, h_v, h_w) = \left(\frac{h_v - h_u}{\sqrt{3}}\right)$$

$$n(h_u, h_v, h_w) = \frac{h_u + h_v + h_w}{3} \quad (4)$$

Note that the redundant states differ in the zero sequence component. For example, $d(1,2,3) = d(0,1,2)$ and $q(1,2,3) = q(0,1,2)$ but $n(1,2,3) = 2$ while $n(0,1,2) = 1$. The relative locations of the voltage vectors and the switching states plays a significant role in the control scheme employed.

Figs.4(a,b) show the classification of the switching states. S_{10}, S_{20}, S_{30} states (fig.4.a) form the three concentric hexagons. S_{10} states produce only one non-zero capacitor current S_{20} states produce equal capacitor currents through two out of the three DC capacitors. S_{30} states correspond to the vertices of the outermost hexagon and produce the largest line voltages. Selection of S_{30} states always produces identical charging currents through all three link capacitors. S_{21} states (fig. 4.b) produce line voltages larger than the S_{10} states but smaller than S_{20} states. However, the S_{21} states (fig.4.b) which are the intermediate points of the intermediate

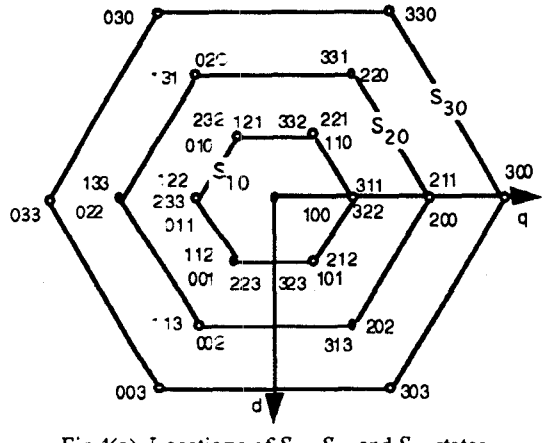

Fig.4(a) Locations of S_{10}, S_{20} and S_{30} states.

vector and the current error vector should be greater than 90°. Mathematically, this condition is written as:

$$Q(k) = Re\left\{\Delta\bar{I}^*_{qds}(\bar{V}(k) - \hat{E}_{qds})\right\} \le 0 \qquad (10)$$

If $\Delta\bar{I}_{qds} = \Delta I e^{j\beta}$; $\hat{E}_{qds} = Ee^{j\theta}$ and $\bar{V}(k) = V(k)e^{j\alpha_k}$, (10) can be re-expressed as:

$$Q(k) = E\left(\frac{V(k)}{E}\cos(\alpha_k - \beta) - \cos(\theta - \beta)\right) \le 0 \qquad (11)$$

Depending on the state selected, $V(k)$ has magnitudes given as: $V(k) = 0.222V_{DC}$ for S_{10} states, $= 0.444V_{DC}$ for S_{20} states, $= 0.385V_{DC}$ for S_{21} states, $= 0.667V_{DC}$ for S_{30} states and $= 0.588\ V_{DC}$ for S_{31}, S_{32} states. In fig.6, the maximum angle γ between the E and ΔI vectors for current regulation is plotted as a function of the voltage boost ($V(k)/E$). It is evident that the angle γ is small for S_{10}, S_{21} and S_{20} states for low boost values Hence, it can be inferred that in order that selection of any S_{10}, S_{21} and S_{20} states results in a reduction of current error vector only occasionally. Selection of S_{30} states results in current regulation for a minimum voltage boost of about 1.4 which is the known ratio for a conventional rectifier. For the four level drive, a DC bus voltage of 660 V was selected with a 460 V line ($V(k)/E = 1.43$) guaranteeing that the selection of a particular S_{30} state will always reduce the current error. The motivation for a low DC bus voltage is to minimize the voltage ratings of the devices used which improves the cost benefit.

C. *Reference current magnitude generation*

The reference current magnitude I_m^* (8) is derived in a manner similar to the conventional two level rectifier. The magnitude is derived from two sources:

(i) Each capacitor voltage is regulated using a PI controller. This approach is a sufficient condition for stable generation of voltage references. The output of all PI regulators is summed to form one part of the reference.

$$I^*_{m1}(t) = \sum_{j=1}^{3}\alpha_j\left(k_p(V^*_{dc}/3 - V_{cj}) + k_i\int_0^t (V^*_{dc}/3 - V_{cj})d\tau\right) \qquad (12)$$

Since $\Delta V_{C3} \approx \Delta V_{C2} - (I_{2R} - I_{2l})\Delta T/C_3$ and $\Delta V_{C1} \approx \Delta V_{C2} + (I_{1R} - I_{1l})\Delta T/C_1$, by regulating each capacitor voltage, in effect the reference is made proportional to the net unbalance between the rectifier and the inverter DC node currents. Also, the integral constant k_i is chosen to be greater than the proportional constant k_p so as to minimize oscillations due to large dynamic range of the DC currents ($k_p = 1$, $k_i = 10$). The value of α_2 was set at 1.2 while α_1, $\alpha_2 = 1$ sufficed for almost all operating points. Increasing the controller constant α_2 improves the dynamic response since i_{C2} has faster dynamics as compared to i_{C1}, i_{C3}.

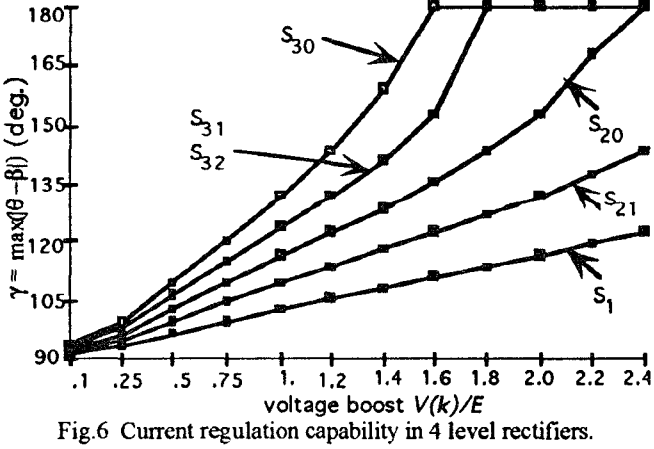

Fig.6 Current regulation capability in 4 level rectifiers.

(ii) An inverter instantaneous output power decoupling term provides the other part of the reference current. Thus:

$$I^*_m(t) = I^*_{m1}(t) + k_{iff}P_{out}(t) \qquad (13)$$

The inverter output power is filtered so that only those variations in load power that lie within the rectifier bandwidth appear in the rectifier magnitude reference. Hence

$$\tilde{P}_{out}(s) = G\frac{P_{out}(s)}{1+s\tau} \text{ where } \tilde{P}_{out}(s) = L^{-1}[P_{out}(t)] \qquad (14)$$

Typically $0.001 \le \tau \le .0167$ with an improved transient response for low values of τ. τ_{iff} was set at 0.002 for all operating points. The rectifier performance however is sluggish since the regulation of each individual capacitor voltages (12) results in a small net term. In the steady state, the capacitor voltages are regulated to their nominal values. Inverter output power is decoupled to prevent inverter overcurrents and resulting bus voltage sags. The phase current reference magnitudes being defined by (12) leads to the phase current references being given by:

$$i^*_u = I^*_m\cos(\omega t) \quad i^*_v = I^*_m\cos(\omega t - 2\pi/3) \quad i^*_w = I^*_m\cos(\omega t + 2\pi/3)$$

III. RECTIFIER SWITCHING SCHEME

The link voltages will stay balanced if the overall bus voltage and the innermost capacitor voltage V_{C2} are regulated. In order to concurrently regulate utility phase currents, a modified hysteresis control method, closely based on the conventional two level case, was devised to schedule the rectifier switching events. Alternate approaches to rectifier switching have been proposed in [11], [14]. In the latter a modified version of space vector based modulation scheme is verified with an R-L load.

Fig.7 shows the disposition of the hysteresis bands on a phase basis and in the dq plane. Two non intersecting tolerance bands are defined around the phase current reference. An intersection of a phase current with the inner tolerance band schedules a '*voltage balancing priority*' event whereas an intersection of any phase current with the outer tolerance band schedules a '*current regulation priority*' event. The principle of this scheme is that when the current errors are small, the rectifier can select states which redistribute the

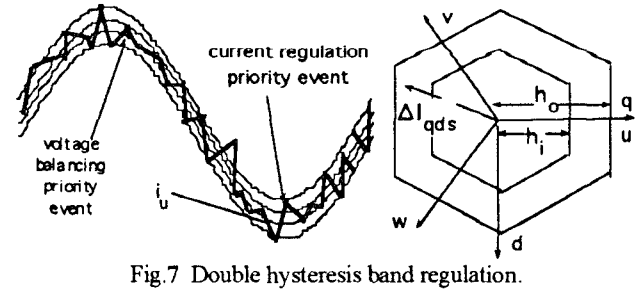

Fig.7 Double hysteresis band regulation.

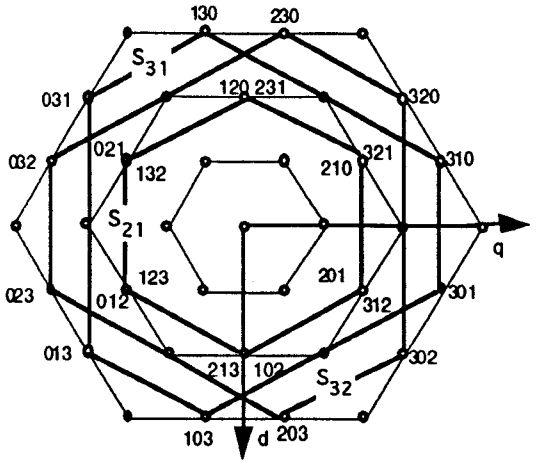

Fig.4 (b) Locations of S_{21}, S_{31} and S_{32} states.

hexagon are the most important for voltage balancing since they lead to currents of opposite polarity in the innermost capacitor and one of the outer capacitors. S_{21}, S_{31} and S_{32} states are shown in fig.4.b. S_{31} and S_{32} states lead to two capacitors currents having the same polarity and magnitude whereas the third capacitor current has the opposite polarity.

II. RECTIFIER CONTROL

A. Time averaged voltage balancing

Whether any switching scheme can be devised to simultaneously balance the link voltages and regulate the utility currents simultaneously can be addressed by referring to fig.2, where the capacitor currents are given as:

$$i_{C3} = i_{C2} - (i_{2R} - i_{2I});\ i_{C1} = i_{C3} - (i_{1R} - i_{1I}) \qquad (5)$$

where i_R and i_I are the rectifier and the inverter DC currents.

The instantaneous rectifier DC current references are given as $i_{2R}^*(t) = i_{2I}(t)$ and $i_{1R}^*(t) = i_{1I}(t)$. $i_{2I}(t)$ and $i_{1I}(t)$ are load and inverter modulation dependent. There are three degrees of freedom (switching functions h_u, h_v, h_w) and 4 constraints i.e. two rectifier DC currents and two utility phase currents. The system is over constrained and hence voltage balancing and current regulation cannot be simultaneously effected.

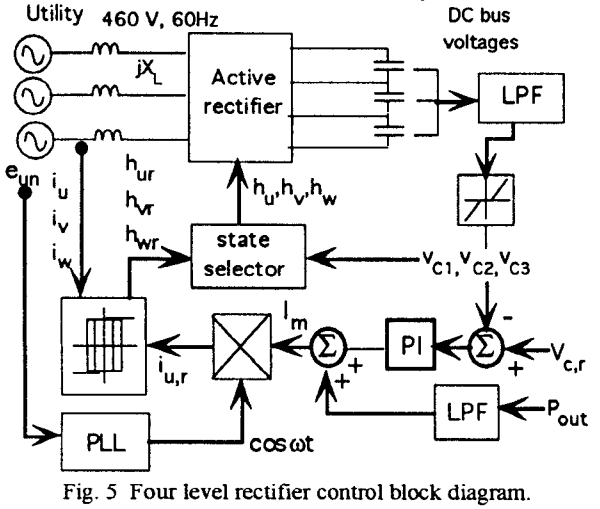

Fig. 5 Four level rectifier control block diagram.

However on an average basis, voltage balancing implies that $I_{C3} = I_{C2} = I_{C1}$. Also, by symmetry of the load and inverter operation, $I_{2I} = -I_{1I}$. Hence, voltage balancing results in only one additional constraint i.e. $I_{2R}^* = I_{2I}$ because symmetric inverter and rectifier operation leads to $I_{1R}^* = -I_{2R}^* = -I_{1I}$. Hence, the constraints can be satisfied on an average basis.

Based on the preceding discussion, a control structure for the rectifier was devised and is shown schematically in fig.5. There are two basic issues - i.e. generation of the current references and more importantly scheduling rectifier switching events. Both these topics are addressed in the following sections.

B. Four level rectifier current regulation capability

The current regulation capability of the four level rectifier depends very strongly on the location of the switching state used to effect current regulation. Simple extensions of the two level current regulation schemes [13] have to be modified by the magnitudes of the *'back-emf'* for developing a consistent switching scheme.

In the stationary *dq0* reference frame, the utility currents are governed by:

$$L_s \frac{d\bar{I}_{qds}}{dt} + R_s \bar{I}_{qds} = \bar{E}_{qds} - \bar{V}_{qds}(k) \qquad (6)$$

where L_s, R_s are utility line inductance and resistance respectively, $\bar{I}_{qds} = I_{qs} - jI_{ds}$ is the line current vector,. Similarly, $\bar{E}_{qds} = E_{qs} - jE_{ds}$ is the utility phase voltage vector and $\bar{V}_{qds}(k) = V_{qs}(k) - jV_{ds}(k)$ is the rectifier phase voltage with respect to the utility neutral. k is the index of the voltage vector that the rectifier can produce and corresponds to each node in the hexagon of fig.3. $(1 \le k \le 37)$. Thus:

$$V_{qs}(k) = \frac{2}{3}\left(v_{uo}(k) - \left(\frac{v_{vo}(k) + v_{wo}(k)}{2}\right)\right) \qquad (7.1)$$

$$V_{qs}(k) = \left(\frac{v_{wo}(k) + v_{vo}(k)}{\sqrt{3}}\right) \qquad (7.2)$$

With the pole voltages defined as in (1), (7.1)-(7.2) hold for continuous utility current case only. The utility phase voltages are assumed to form a balanced set and are given as:

$E_{un} = E\cos(\omega t)\ E_{vn} = E\cos(\omega t - 2\pi/3)\ E_{wn} = E\cos(\omega t + 2\pi/3)$

Thus, $E_{qs} = E\cos(\omega t)$ and $E_{ds} = -E\sin(\omega t)$. Further, it can be observed that each vector with index k, may have more than one constitutive switching states. Substituting $\Delta\bar{I}_{qds} = \bar{I}_{qds}^* - \bar{I}_{qds}$, the current error equation is given by

$$L_s \frac{d\Delta\bar{I}_{qds}}{dt} + R_s \Delta\bar{I}_{qds} = \bar{V}(k) - \hat{E}_{qds} \qquad (8)$$

where $\hat{E}_{qds} = \bar{E}_{qds} - R_s \bar{I}_{qds}^* - L_s \frac{d\bar{I}_{qds}^*}{dt}$; and

$$\bar{I}_{qds}^* = I_m^* \cos(\omega t) + jI_m^* \sin(\omega t) \qquad (9)$$

where I_m^* is the reference current magnitude. The procedure for generating I_m^* is dealt with in the next section. The right hand side of (8) is the rectifier regulating voltage. For effective regulation, the angle between the regulating voltage

charges amongst the DC capacitors. The selected states are not guaranteed to reduce current errors thereby necessitating the outer hysteresis band switching event dedicated to reducing the current errors. Voltage balancing priority event is disabled when phase current returns within the inner tolerance band so as to minimize the switching frequency.

A. Voltage balancing priority event

The inner band schedules a switching event where the rectifier control has to select a vector, $V(k)$, such that the resulting capacitor currents drive the voltage deviations to zero. The capacitor voltage deviations are given by:

$$\Delta V_{c_j} = V_{c_j} - V_{dc}^*/3 \quad j = 1,2,3 \;\&\; if \;\; |V_{c_j} - V_{dc}^*/3| > \delta \quad (15)$$
$$= 0 \qquad \text{otherwise}$$

A dead band of magnitude 2δ is introduced around the nominal capacitor voltages disabling the voltage balancing if all deviations are within tolerances. A large value of the tolerance reduces the required switching events but makes unbalance recovery harder to accomplish. The suitability of a state k, in a voltage balancing priority event is determined by evaluating the incremental real power that would flow through each capacitor p_{cj} for state k.

$$p_{c_j}(k) = i_{c_j}(k) \times \Delta V_{c_j} \; ; \; j = 1,2,3 \quad (16)$$

A state is ideal for balancing the voltages if it results in negative values in (16). Ordinarily, (16) needs to be evaluated for all 64 states. Considerable simplification results from the observation that for lagging power factor operation of the inverter, capacitor C_2 discharges more rapidly than C_1 or C_3. For example, if the previous state was an S_{30} state, $I_{1R} = I_{2R} = 0$, thus $\Delta V_{C3} = \Delta V_{C2} - kI_{2I}$ and $\Delta V_{C1} = \Delta V_{C2} + kI_{1I}$. So, ΔV_{C1}, $\Delta V_{C3} \leq \Delta V_{C2}$ since $I_{2I} \geq 0$ and $I_{1I} \leq 0$. ($k = \Delta T/C_1$ and I_{1I} and I_{2I} are the average inverter DC currents in the interval between the previous switching event and the current event). Thus, power usually needs to be transferred from the outer to the inner capacitor. This rules out the selection of S_{30}, S_{31}, S_{32} and S_{20} states since they produce currents of the same polarity through the inner and at least one outer capacitor. Thus, only S_{21} and S_{10} states need be considered in (10). If $\Delta V_{c2} < -\delta$, $\Delta V_{c3} > \delta$, $|\Delta V_{c1}| < \delta$, unbalance is reduced if a state can be found such that it produces $i_{c3} < 0$, $i_{c2} > 0$. In general, the existence of two S_{21} states that will transfer power from an outer capacitor to the inner capacitor is guaranteed. These states are in quadrature with input current vector. Referring to fig.8 where $i_u > 0$, $i_v < 0$, $i_w < 0$, states (213) and (231) will produce desirable capacitor currents but neither of these states can regulate input currents. State (231) should then be chosen since it causes the current error to grow more slowly. In case $|\Delta V_{C2}| >> |\Delta V_{C1}|, |\Delta V_{C3}|$, S_{10} states (211), (212) and (221) should be chosen, since these states cause $i_{C2} > 0$. For any S_{21} or S_{10} state chosen at $V_{dc} = 660\ V$, the current error grows necessitating the current regulation event.

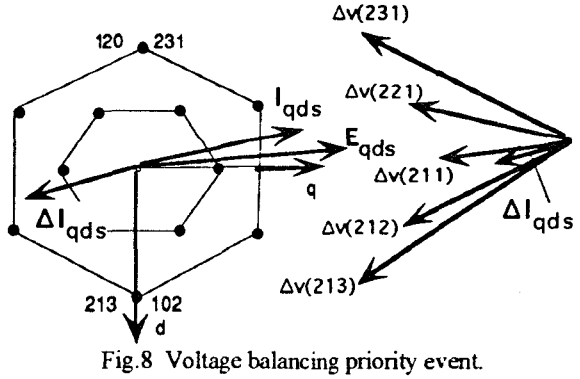

Fig.8 Voltage balancing priority event.

B. Current regulation event

When the current error grows exceeds an outer current threshold, the rectifier control initiates a current regulation event. For example, suppose that $\Delta V_{C1} > \delta$, $\Delta V_{C2} < -\delta$, $\Delta V_{C3} > \delta$ and the E, I, ΔI vectors are oriented as shown in fig.9. In this case, initially all S_{30}, S_{31} and S_{32} states as well as two S_{21} states i.e. (321) and (123) are to be considered. Of these using (10), the states remaining to be considered are (030), (130), (230), (330), (320), (310), (300), (301), (302) and (321). Of these, states (300), (301) and (302) can be omitted, because they lead to $i_{C2} < 0$. Of the remaining states, state (321) would be selected. However, state (030) should be chosen to minimize the switching frequency. In fact, if an S_{21} state cannot regulate the current, the controller is biased to select only an S_{30} state since it always produces capacitor currents of the same polarity and would thus never exacerbate the link voltage imbalance.

IV. RECTIFIER PERFORMANCE

The proposed drive system was simulated using ACSL. The control scheme was found to work under a wide variety of load conditions. Unity power factor operation can be clearly seen from Fig.10 which shows the utility phase voltage and current as well as the pole voltage at the rated operating point of the motor. Fig.11(a,b) show the rectifier and motor phase currents as well as regulated DC bus voltages at a high speed (3560 RPM) operation of the induction motor. Fig.12 shows the input current in the low speed case while in Fig.13 the currents are traced for the generating mode of the induction motor. Thus, the rectifier scheme imparts a true bi-directional capability to the drive.

The main parameters affecting the rectifier operation are the hysteresis bands and the bandwidth of the DC voltage filters. Reducing the bands increases the average switching

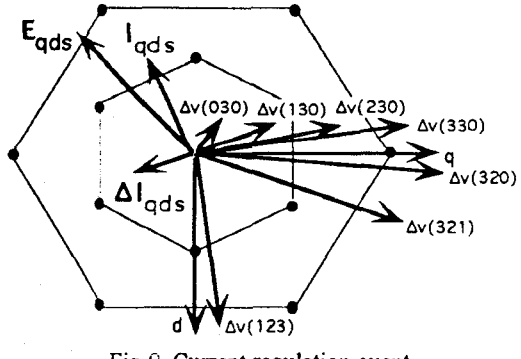

Fig.9 Current regulation event.

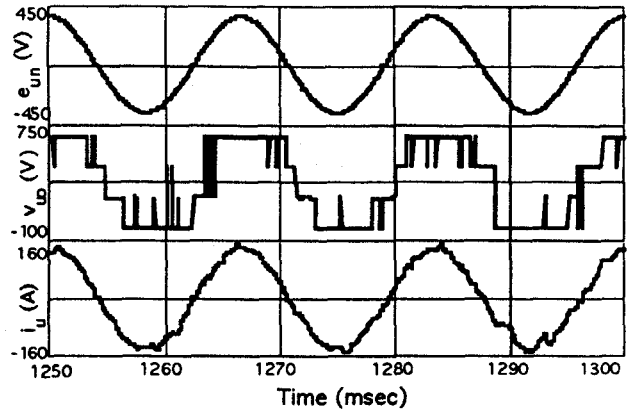

Fig.10 Utility phase voltage, currents, link voltages (rated point).

frequency and the losses. For light loads at low speeds, current regulation capability is severely degraded as seen in fig.13. However, due to the small magnitudes of the harmonics injected, this is not a serious drawback. By reducing the tolerance bands, the harmonics can be reduced.

The bandwidth of the link voltage filters has a significant impact on the rectifier operation. When the bandwidth was increased from about 100 Hz to 1 kHz, at the rated point, the current THD was found to increase from 6.5% to 9.5%. More significantly, the average switching frequency increased from 1.3 kHz to 1.7 kHz. The main cause for this effect is that the reference current now is distorted as compared to the low bandwidth case (fig.14). This result is generally valid over the entire operating region. Hence the filter bandwidth is kept low to minimize THD and switching

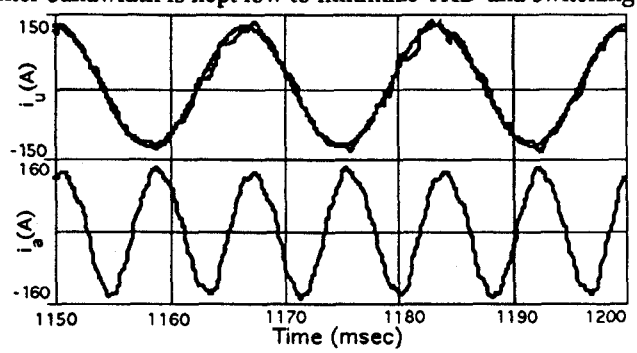

Fig.11(a) Input phase and motor phase current (3560 RPM).

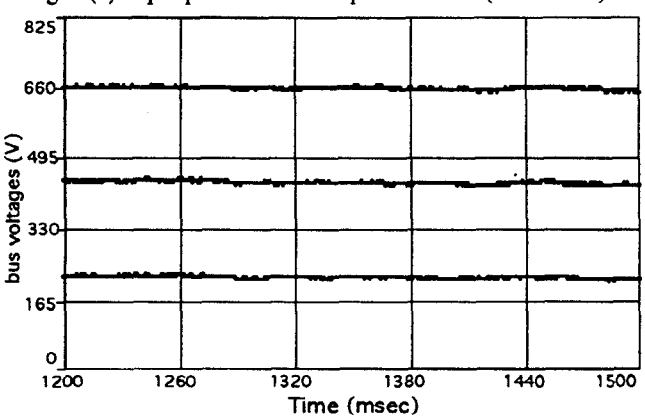

Fig.11(b) DC voltages at high speed operation.

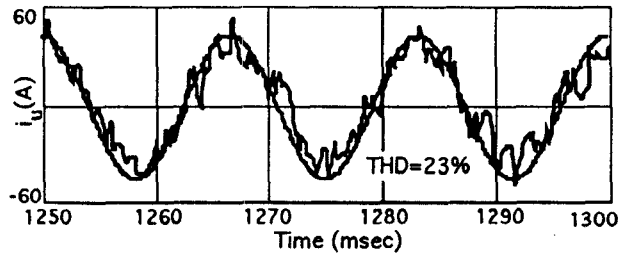

Fig.12 Input current, link voltage at 450 RPM.

frequency at the expense of speed of response. The tolerance bands around the capacitor voltages have marginal effect on the performance. A large value of the voltage tolerance band leads to an increase in the load current THD and must be avoided for that reason.

Fig.15 shows a phase leg of the four level active rectifier and the current distribution amongst important devices in the leg. The bulk of the phase current is seen to be carried by the antiparallel diodes and the inner clamp diodes The current distribution is consistent with charging the innermost capacitor and regulating the total DC bus. However, the devices are stressed unequally.

Table 1 summarizes the performance of the rectifier at the nominal operating point of the motor. In any multilevel topology, the number of state transitions per second (Column 6) is not directly related to the actual device switching frequency. With a dynamic current control scheme power dissipation is hard to predict. The devices actually switch at very different frequencies depending on their location on a phase leg. By counting the number of commutations per

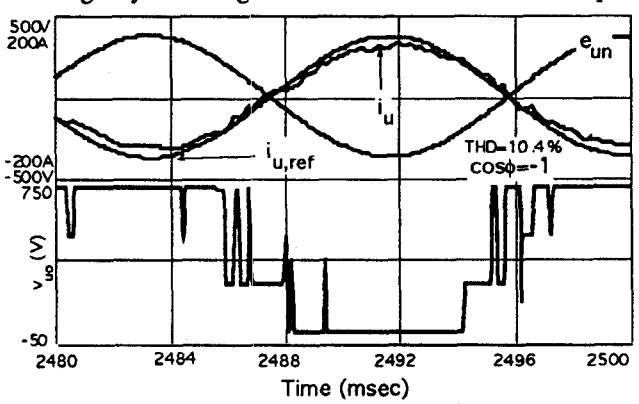

Fig.13 Input phase voltage, current, pole voltage (gen. mode).

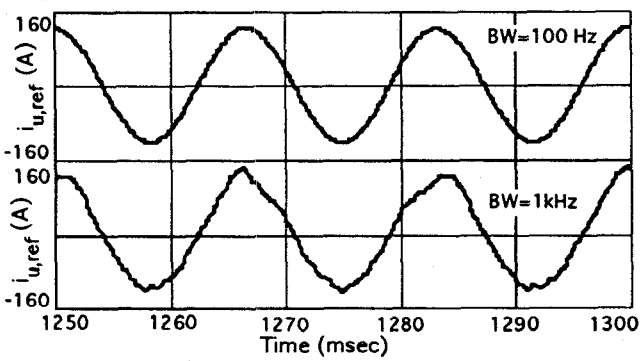

Fig.14 Input current references (BW = 100 Hz & 1 kHz)

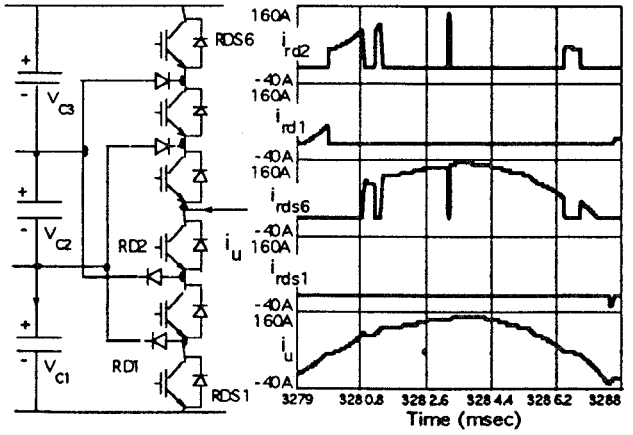

Fig.15 Phase leg, current distribution in four level active rectifier.

cycle, an estimate of average device frequency is reported in Column 9. This value of average switching frequency is quite low (about half the number in Column 6) and consistent with simulation indicated efficiency of about 94% at the rated operating point. Rectifier operation at any other operating point can be similarly evaluated. The almost constant value of the load current THD indicates that so long as the link voltages are regulated, the load performance is not affected by the rectifier parameters. The table clearly illustrates that the reactor and capacitor sizes can be traded off with the switching frequency. Capacitance values can be safely reduced to values comparable to the two level converter case. The line reactances have to be sized to minimize switching at light load conditions. Alternately, by increasing the tolerance bands switching frequency is reduced at the expense of increased current THDs. With the advent of faster IGBTs, this tradeoff is not significant. However, this scheme may not be well suited to GTO thyristor based drives due to the high switching frequencies and increased losses.

C_{dc} *mF*	L_s *mH*	h_i *A*	h_o *A*	δ *V*	f_{sw} *Hz*	I_u *%THD*	I_a *%THD*	F_{sw} *Hz*
6	2	10	20	1	1260	6.5	10.4	640
6	2	10	30	1	1020	10.8	12.1	480
6	2	10	20	3	1500	8.4	10.3	760
3	2	10	30	1	1200	9.4	10.7	680
3	1	10	35	1	2640	12.9	9.0	1360
3	1	15	30	1	1680	17.4	10.7	720
3	1	10	45	1	1200	15.9	8.5	440
3	1	5	45	1	1740	15.7	8.9	800

Table 1. Rectifier performance at rated operating point.

IV. CONCLUSIONS

In this paper, a new robust control strategy for an active four level rectifier was discussed. The proposed scheme is verified by simulation studies to work satisfactorily for almost all operating conditions of the induction motor including the generating mode. The control scheme is completely dynamic and the need for lookup tables has been eliminated. The rectifier control scheme is an attractive drive solution since the link voltages are balanced almost entirely from the rectifier so that the inverter modulation can be optimized since it is now unconstrained.

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