A Four Level Inverter Based Drive With a Passive Front End.

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Abstract—Multilevel inverters are suited for high power drive applications due to their increased voltage capability. A four level inverter is able to synthesize better waveforms and attain higher voltages while reducing the device ratings. While converter device count and kVA are high, a conventional diode bridge rectifier is a low cost multilevel drive solution for the input rectifier if suitable inverter side dc voltage balancing schemes can be devised. This paper investigates the operation of four level rectifier/inverter based drives under commonly used modulations schemes. Link voltage balancing and output voltage capability are analyzed for a four level inverter. Simulation results are presented to verify the link voltage balancing strategy in the absence of any balancing action from the rectifier.

I. INTRODUCTION.

Multilevel inverters are based on the neutral point clamped inverter topology first proposed by Nabae et al [1]. For high power drive applications, three level inverter based drives and control scheme have been extensively studied [2-6]. The trend towards a greater number of levels is necessitated by advantages of higher voltage ratings. For example, 1200V devices are normally required in a conventional VSI with a DC bus voltage of 600V whereas using the same devices and a three level inverter, the DC bus can be rated at 1200V. With a four level inverter, the DC bus voltage can be raised to 1800V. Thus, there are clear advantages to using multilevel inverters especially when the voltages can be raised sufficiently high enough to eliminate transformers.

Associated with multilevel inverter based drives is the problem of DC link voltage balancing. However, redundant states offer a method of redistributing the charge amongst the DC capacitors. The severity of the problem varies with the application. In case of static var compensation, voltage balancing is much easier since the power flow is essentially reactive. It is possible to regulate the link voltages using a low frequency switching scheme and properly selecting the redundant states. In drive applications, the availability of redundant states will determine whether the link voltages can be balanced. Also, it is not always possible to balance the link voltages at every switching event.

In drive applications, real power flow leads to the drift of the link 'neutral' voltages in a multilevel DC bus. Capacitor voltages can be balanced with the help of an active rectifier as discussed in [7,8,9]. Additionally, with an active rectifier, the DC voltage is reduced and the inverter modulation is relatively unconstrained by link voltage balancing requirements. The drawback of this approach is that there are now two active converters which increases the cost of the drive system. Partially active rectifier topologies as in [7] are compromise solutions which have a lower kVA rating than a fully active rectifier and a lower power transfer capability.

The simplest method of connecting a multilevel DC bus to the utility is by the diode bridge rectifier due to its greatly reduced cost. In this paper, the passive solution i.e. a diode bridge rectifier front end is considered since it represents the simplest configuration of the multilevel drive. For example, a fully active 4 level rectifier/inverter system has a nominal total device kVA rating of $24V_{dc}I_{max}$: a partially active four level rectifier and a four level inverter has a device kVA rating of $22V_{dc}I_{max}$ whereas a diode rectifier-four level inverter system has a total device kVA rating of $18V_{dc}I_{max}$. For larger drives, the cost benefits of reduced device kVA may prove advantageous especially when utility harmonic currents may be reduced by active filters.

II. THE FOUR LEVEL INVERTER.

Of the three prominent multilevel topologies, the diode clamped inverter topology has been found to be suitable for drive applications primarily because of reduced component device ratings and count [10] though the cascadced H bridges topology [11] is extremely modular and robust for practical applications. The four level diode clamped inverter is the only topology discussed further. (Fig. 1).
Fig. 1 Four level inverter (diode clamped topology).

Fig. 2 Four level inverter switching states in dq0 plane.

The DC inverter voltages are given by:
\[
\frac{d}{dt}v_C = \bar{F}I_{DC}(t)
\]
where \(v_C = [v_{C1}(t) \ v_{C2}(t) \ v_{C3}(t)]^T\), \(C = 3C_{DC}\) and
\[
\bar{F} = \begin{bmatrix} 1 & 0 & 0; 1 & 1 & 0; 1 & 1 & 1 \end{bmatrix}^T
\]
Therefore, from (5) and (6), we get
\[
\frac{d}{dt}v_C = \bar{F}M(t)\dot{I}(t)
\]
Eq. (8) represents a physical system with a variable structure since the matrix \(M(t)\) is modulation dependent (\(0 \leq \text{rank}(M(t)) \leq 2\)). The differential mode component of each capacitor voltage is then given as:
\[
\Delta V_C = \bar{V}_C - \begin{bmatrix} 1 & 1 & 1 \end{bmatrix}^T V_{CM}
\]
where
\[
V_{CM} = \begin{bmatrix} \frac{V_{C1} + V_{C2} + V_{C3}}{3} \end{bmatrix}
\]
Since \(\text{rank}(T) = 2\), only two of the three capacitor voltage deviations are independent. \(V_{CM}\) is the common mode capacitor voltage which can be considered as resulting from a common charging current. By differentiating (9) and substituting (8), one obtains:
\[
\frac{d}{dt}\Delta V_C = \frac{1}{C} \overline{\bar{F}M(t)\dot{I}(t)}
\]
Capacitor voltage unbalance in an interval \(t_0 < t < t_1\) is minimized when:
\[
\|
\Delta V_C \| = \left\| \frac{1}{\overline{C}} \overline{\bar{F}M(x)\dot{I}(x)} \right\| dx = \text{minimum}
\]
A necessary condition for this to occur is:
\[ \Delta V_C = \mathbf{T} \mathbf{F} M(t) \mathbf{f}(t) \leq 0 \quad (13) \]

When (13) is satisfied, the capacitor voltage unbalance is guaranteed to not grow. The interval \( t_1 - t_0 \) is usually the switching interval over which the load current dynamics do not change appreciably. Hence, at the start of a switching interval, computations can be made about the switching state to be selected based on the currently available values of the load currents.

Link voltage balancing then can be formulated as a problem in finding a suitable switching state \((h_a,h_b,h_c)\) which will satisfy (13). There are 64 switching states and finding a switching state to satisfy (13) is, in general extremely computationally intensive. Simplification of (13) leads to a more insightful version of the voltage balancing condition i.e.
\[
\Delta V_{C1} i_{C1} + \Delta V_{C2} i_{C2} + \Delta V_{C3} i_{C3} \leq 0 \quad \text{or} \\
\Delta V_{C1} (I_2 + I_1) + \Delta V_{C2} I_2 \geq 0 \\
(14)
\]

Eq.(14) can be combined with (4) to determine the effect of selecting a switching state on the link voltage unbalance. Therefore, if an \( S_{30} \) state is selected, (14) is always satisfied with the equality - hence link unbalance, if any, does not worsen. However, this corresponds to the largest voltage vectors being used (two level operation) and consistent selection of such states makes poor utilization of the low THD waveform generation capability of the inverter. To gain a further insight into the nature of link voltage balancing, (14) can be recast into the following form:
\[
\Delta V_2, I_2 + \Delta V_1, I_1 \geq 0 \\
\text{where} \quad \Delta V_2 = \Delta V_{C1} + \Delta V_{C2} \quad \text{and} \quad \Delta V_1 = \Delta V_{C1} \\
(15)
\]

From (15) it is evident that two neutral voltages need to be regulated. Eq. (15) also suggests a strategy as follows: select a switching state which produces a DC node current of the polarity opposite that of voltage of the node into which it flows. For example, if \( \Delta V_2 > 0 \) and \( \Delta V_1 < 0 \), link unbalance is reduced if we select only those states which produce \( I_2 > 0 \) and \( I_1 < 0 \). It is not however guaranteed that such states can be freely selected expressly for link voltage balancing.

In a typical application, the inverter modulation scheme such as sine triangle PWM, current regulation etc. determine the voltage vector that the inverter must produce. Also, as shown earlier multiple switching states \((n^3)\) produce the same voltage vectors \((1 + 3n(n - 1))\) - thereby illustrating the phenomenon of redundant states. Assuming that the inverter is required to produce a voltage vector \((v_q, v_d)\) - the switching states that will produce the required voltage vector can be determined by inverting (1). The solutions have to be integers satisfying \( 0 \leq h_a, h_b, h_c \leq 3 \). The exact number of redundant states will depend on the magnitude of \( v_q \) and \( v_d \).

When the inverter is required to produce a vector \((v_q, v_d)\), inverter DC currents are evaluated for each constituent switching states using (4). Eq. (15) is then tested for suitability for link voltage balancing. That switching state is selected which produces desirable DC currents.

III. CAPACITOR VOLTAGE BALANCING WITH SINE TRIANGLE PWM.

In the previous section, a mathematical condition for link voltage balancing was derived. Given the freedom to select any switching state from the four level inverter, the link voltages can be driven towards balance at each switching state selection event. However, the inverter operation is constrained by a modulation scheme typical of which is the sine triangle PWM scheme. The four level sine triangle algorithm is based on the multilevel sine triangle PWM scheme first proposed in [13]. Fig. 4 shows the disposition of the triangle carrier waves and the reference sinusoid. This scheme produces at its output the three phase switching functions according to:

\[
\begin{align*}
    h_a &= 3 & \text{if} & & v_a^* & \geq v_{rc3} \\
    h_a &= 2 & \text{if} & & v_{rc3} & \geq v_a^* & \geq v_{rc2} \\
    h_a &= 1 & \text{if} & & v_{rc2} & \geq v_a^* & \geq v_{rc1} \\
    h_a &= 0 & \text{otherwise}
\end{align*}
\]

The phase switching functions of the other two phases are similarly defined. Supposing that the state \((h_a,h_b,h_c)\) is the PWM pattern, the number of redundant states, if any, can be determined from:
\[
N_{red} = 3 - \max(h_a, h_b, h_c) + \min(h_a, h_b, h_c) \\
(16)
\]

The resulting DC node currents for each constitutive switching state is evaluated from (4). Eq. (15) is evaluated for each switching state and that switching state is selected which produces the most positive left hand side in (15).

In multilevel inverters, visualizing the voltage deviations is not tractable especially for \( n \geq 3 \). In order to obtain a clearer understanding of voltage deviation pattern of the four level DC bus we rewrite (15) as:
\[
E = \Delta V_1 \left( X_{q1} i_q + X_{d1} i_d \right) + \Delta V_2 \left( X_{q2} i_q + X_{d2} i_d \right) \\
(17)
\]
\[
X_{qj} = \left( \delta(h_a - j) - \frac{\delta(h_a - j) + \delta(h_a - j)}{2} \right) \\
(18.i)
\]
\[ X_{dj} = \frac{\sqrt{3}}{2} \left( \delta(h_d - j) - \delta(h_c - j) \right); \ j = 1, 2 \quad (18.ii) \]

By integrating (17) over one fundamental period, a necessary condition for the link voltages to remain balanced can be established as:
\[ \int_0^T \Delta V_2(x)dx = \int_0^T \Delta V_1(x)dx = 0 \quad (19) \]

This in turn implies that:
\[ \Delta V_1(\bar{x}_{qd1} - \bar{I}_{qd1}) < 0 \quad \text{and} \quad \Delta V_2(\bar{x}_{qd2} - \bar{I}_{qd2}) < 0 \quad (20) \]

The dimensionless 'vectors' \( X_1 \) and \( X_2 \) for a 4 level inverter depend on the voltage vector itself. This representation is useful in determining the effect of selecting a voltage vector on link voltage balancing. Figs. 5-7 illustrate the orientation of \( X_1 \) and \( X_2 \) relative to the voltage vectors for each class of switching states. Considering fig. 2, it can be seen that the magnitude of the inverter voltages varies with the modulation depth \( m_a \). Fig. 8 shows the graphical equivalent of (20) applied to \( S_{10} \) states. According to the balancing scheme, for \( \Delta V_1 > 0 \) and \( \Delta V_2 > 0 \), if \( X_p(h_a, h_b, h_c) \) belongs to region II (or \( = 0 \)) then \( \Delta V_1 \) can be regulated and if \( X_q(h_a^*, h_b^*, h_c^*) \) belongs to region II (or \( = 0 \)) then \( \Delta V_2 \) can be regulated. In fig. 7, for the load current vector as shown, state \( (322) \) will regulate the DC voltages most effectively. For \( S_{10} \) states, it is always possible to select a switching state which produces current of an appropriate polarity through any DC capacitor. A similar graphical equivalence can be derived for each of the switching state classes.

**Fig. 8**: \( S_{10} \) Switching state selection for voltage balancing.

When a voltage vector corresponding to an \( S_{21} \) state is selected, it can be shown that for at least one switching state both DC voltages can be regulated. Thus, from fig. 9 it is evident that state \( (321) \) will regulate \( \Delta V_1 \) and \( \Delta V_2 \). A similar argument holds for \( S_{20} \) states. For \( S_{30} \) states, \( X_1 = X_2 = 0 \) identically and so link unbalance never worsens as a result of selecting \( S_{30} \) states. When an \( S_{11} \) or \( S_{12} \) state is selected, two cases arise as illustrated in fig. 10. In fig. 10(a), the selection of state \( (310) \) results in an appropriate polarity of current to regulate \( \Delta V_1 \) but selection of \( (301) \) with the load current at the same power factor will cause a charging current of the opposite polarity thereby worsening the unbalance. A similar result can be shown to hold for \( S_{22} \) states. When \( S_{30} \) states are selected, as stated earlier, the capacitors are charged symmetrically. Thus, when outer hexagon states are used, it follows that unbalance will result.

This is the fundamental limitation in the link voltage balancing capability of the four level inverter. Note that the limitation arises from the fact that there are now no redundant states available which will regulate the DC voltages. Assuming ideal and balanced three phase load currents, in the limiting case when only the \( S_{31}, S_{32} \) and \( S_{30} \) states are used the average values of the DC currents are given by:
\[ \langle I_1 \rangle = -\langle I_2 \rangle = 6 I \cos \phi \sin \left( \frac{\tilde{\lambda}}{2} \right) \cos(2\pi/3 - \lambda); \quad (21) \]

where \( \lambda = 19.11^\circ \) and \( I \) is the peak value of the load phase currents. Also,
\begin{align}
\langle i_{C2} \rangle &= \langle i_{C3} \rangle - \langle i_2 \rangle = \langle i_{C3} \rangle - 0.188 I \cos \phi \\
\langle i_{C1} \rangle &= \langle i_{C3} \rangle - \langle i_2 \rangle + \langle i_1 \rangle = \langle i_{C3} \rangle
\end{align}

(22)  (23)

Thus, the innermost capacitor tends to discharge for any real load because \( \cos \phi \neq 0 \). Also, there is symmetry in the charging of \( V_{C1} \) and \( V_{C3} \). Typically, in the absence of any balancing action, \( V_{C2} \) undergoes inversion leading to a catastrophic shutdown.

\[ V_{C1} + V_{C2} = V_{C3} \]

(301)

\[ V_{C1} + V_{C2} + V_{C3} = 0 \]

(310)

\[ I_m \quad \frac{\text{Freq. ratio}}{m} \quad \text{Ref.} \quad \text{Freq. ratio} \quad \text{Enable} \quad \Delta V_{C1} \quad \Delta V_{C2} \quad \Delta V_{C3} \quad \text{To Gate Drives} \]

Fig. 12 Inverter control scheme.

\[ V_{qs}(V) \quad V_{ds}(V) \quad V_{qs}(V) \quad V_{ds}(V) \quad 273 \quad \text{RPM} \]

(14)

\[ V_{qs} \text{ and } V_{ds} \text{ at } 20 \& 40 \text{ Hz} \]

IV. SIMULATION RESULTS.

Fig. 11 shows the drive system that has been simulated to verify the theory developed in the previous sections. This system is currently being constructed at the University of Wisconsin. The load for a high 8 pole 460/230V induction motor. 600V/100A IGBTs are used as the active switches. The control scheme implemented is based on the scheme outlined in the previous section. A four level PWM scheme provides the pulse pattern to a redundant state selector. In [14], a control scheme for such a topology with R-L loads only is discussed.

Fig. 12 shows the block diagram of the control scheme. The redundant state selector performs the link voltage balancing. It should be noted that the input to this block can be voltage vectors resulting from any control scheme such as current regulation or field orientation. In this particular case, a simple V/Hz control scheme was implemented. Fig. 13 shows the motor phase voltage and current for a low speed operation case. For a low carrier frequency of 420 Hz, the current THD is reasonably low at about 11%. The actual

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device switching frequency varies with the location of the device in the inverter pole. Depending on the load currents and link voltages, the actual device switching frequency can be as high as three times the carrier frequency if at every reference-triangle intersection a transition occurs in all phase switching functions. At low modulation depths states with higher redundancies are selected. At low modulation depths, as explained earlier, only \( S_{10} \) states are being used, hence the link voltages are balanced as is shown in fig. 14.

Fig. 15 shows the motor \( q \) and \( d \) axis voltages in the stationary reference frame when the synchronous frequency is 20 Hz and 40 Hz. As the modulation depth is increased, \( S_{10} \) and \( S_{21} \) states are selected as shown in fig. 15(b). In this case, link voltages can be still balanced because modulation in this range can be considered as a superposition of two modulations - one using only \( S_{10} \) states and the other using only \( S_{21} \) states.

For a fixed 'gear ratio', as the synchronous frequency increases at constant V/Hz the current THD improves significantly because the motor leakage reactance is better able to filter the currents. This results in reduced phase current THD (4.4%) at the rated point of the motor as shown in fig. 16. Motor torque at this operating point is traced in fig. 17 which suggests a peak to peak torque of about 20%.

The inverter operates at the limits of its voltage capability while retaining four level inverter operation when \( m_u \geq 0.75 \) (approx.). Scant use is made of \( S_{31}, S_{32}, S_{30} \) states as seen in fig. 18(a) where the synchronous frequency is 90 Hz and the motor produces 80N-m torque (field weakening). Link voltages are still balanced as shown in fig. 19. The induction motor leakage reactance now filters the current further so that the current THD stays low (5.2%) even when the carrier frequency is dropped (fig. 20). Finally, fig. 21 shows the motor phase and current under no load conditions when the inverter synchronous frequency is 120 Hz. As seen in fig. 18(b), the inverter modulation makes use of the outermost states \( (S_{31}, S_{32}, S_{30}) \) since the modulation depth is high (≈...
Also at no load, the motor impedance is predominantly inductive so that \( \cos \phi \approx 0 \). Hence, in accordance with (21)-(23), \( <I_{C1}> = <I_{C2}> = <I_{C3}> \approx 0 \) and so the link voltages stay balanced. This is reflected in fig. 22 showing the well regulated DC link voltages.

Although the four level inverter cannot satisfactorily balance capacitor voltages for \( m_a \geq 0.75 \) and deliver real power to the load, in applications wherein higher voltages are required, the inverter can be made to operate in the two level mode i.e. selecting only \( S_{30} \) states - thereby trading off voltage THD for fundamental voltage magnitude.

Fig. 22  DC link capacitor voltages at no load and 120 Hz.

IV. CONCLUSIONS

Four level inverters based drives with a diode rectifier front end offer the prospect of reduced total kVA ratings. A new methodology for viewing concurrent link voltage balancing and inverter modulation was discussed. It is possible to obtain low THD voltage waveforms from the four level inverter while retaining adequate link voltage balancing capability. This makes such drives suitable for applications wherein low speed operation is the dominant mode of operation. The voltage THD can be lowered at lower average device switching frequencies. Time domain simulations indicate that the control scheme for link voltage balancing outlined earlier are viable over the entire motoring region. If necessary, the voltage capability of the four level inverter can be improved by reverting the modulation to a conventional two level scheme.

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