Research Report

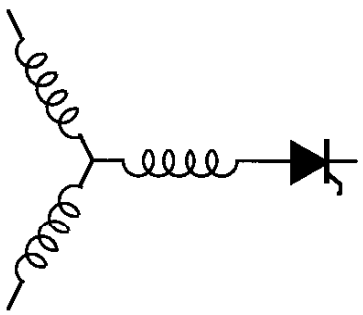
98-03

Active Filtering for Common Mode Conducted EMI Reduction in VoltageSource Inverters

A.L.Julian*, R. Cuzner*, G. Oriti, T.A. Lipo

Wisconsin Power Electronic
Research Center
University of Wisconsin-Madison
Madison WI 53706-1691

* Eaton Corporation / NCD
4265 North 30th St.
Milwaukee, WI 53216



Wisconsin
Electric
Machines &
Power
Electronics
Consortium

University of Wisconsin-Madison
College of Engineering
Wisconsin Power Electronics Research Center
2559D Engineering Hall
1415 Engineering Drive
Madison WI 53706-1691

Active Filtering for Common Mode Conducted EMI Reduction in Voltage Source Inverters

A. L. Julian, R. Cuzner
Eaton Corporation / NCD
4265 North 30th St.
Milwaukee, WI 53216
e-mail: {aljulian,rcuzner}@vines.etn.com

G. Oriti, T. A. Lipo
University of Wisconsin
1415 Engineering Drive
Madison, WI 53706
e-mail: oriti@cae.wisc.edu, lipo@engr.wisc.edu

Abstract **- As solid state power converters become more numerous the unwanted EMI effects created by these converters increase. To address this issue more attention has recently been given to the reduction of electromagnetic emissions created by power electronics. The proliferation of solid state inverters brings the cost of semiconductors down making active filtering an attractive alternative to passive filter topologies. Active filtering may also realize higher efficiency than passive filtering. This paper focuses on an active filter topology that significantly reduces the common mode voltage created by voltage source inverters. The reduction of common mode voltage is achieved by introducing a novel inverter topology and a new hysteresis modulation strategy to control this inverter topology.**

I. INTRODUCTION

Voltage source inverters are becoming more prevalent as an interface between DC energy sources such as fuel cells, batteries, photovoltaic arrays or simply diode rectifiers and three phase AC utility lines in areas such as factories, hospitals, ships and aircraft to name a few. Three phase voltage source inverters followed by second order filters are a popular method of creating a 'clean power' interface. While much attention has been given to conditioning the differential output voltage of such systems little attention has been placed on the common mode voltage created by the voltage source inverter.

Traditionally, isolation transformers and/or common mode inductors have been used to impede the common mode conducted current caused by common mode voltage. This paper investigates an active filter topology as an alternative to passive filtering to mitigate common mode conducted EMI. The active filter greatly reduces the size of the common mode inductor needed to limit the common mode conducted current. Magnetic materials used for common mode inductors are bulky and expensive; active filtering is a more compact alternative. As semiconductor prices diminish, active filtering becomes more cost effective than using expensive magnetic materials to mitigate common mode conducted EMI. Additionally, active filtering reduces the losses associated with the common mode filter.

In this paper six pole VSIs driving three phase loads are examined. As the power rating of the converter exceeds that of available power switches, the need to parallel inverter poles arises. In a six pole-three phase VSI the rating of the power switches is half the rated output current.

II. CIRCUIT OPERATION

Active reduction of the common mode voltage inherent in voltage source inverters (VSIs) can be achieved in two steps. First, the active and passive elements that balance the circuit are added to the VSI. Second, a new modulation strategy can be introduced to maintain the differential voltage performance and cancel the common mode voltage. If the DC source driving the VSI does not contain common mode distortion then the common mode voltage produced by the VSI can be significantly reduced [2,3,4].

Fig. 1 shows the inverter topology being studied. The six inverter poles used for power conversion are modulated depending on the current flowing in their respective inductors, labelled L_f in Fig. 1. The seventh inverter pole is present only to balance the inverter/filter network thus realizing active filtering of the common mode voltage.

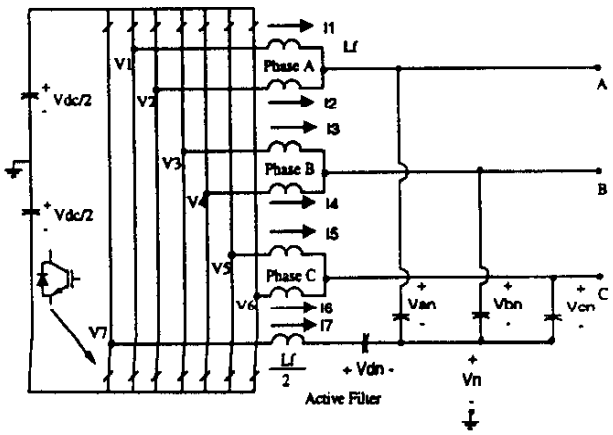


Fig.1 Schematic of the inverter with active filter

When the three phase load is balanced, the active filter pole carries only the ripple current due to the modulation, thus the active devices and the active filter inductor in this pole can be significantly derated with respect to the power phase pole devices and inductors. This approach increases the cost effectiveness of the active filter with respect to traditional passive filters.

For the circuit in Fig. 1 the equations that describe the voltage loop through the filter neutral are:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ 2V_7 \end{bmatrix} = L_f \frac{d}{dt} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \end{bmatrix} + \begin{bmatrix} V_{an} \\ V_{an} \\ V_{bn} \\ V_{bn} \\ V_{cn} \\ V_{cn} \\ 2V_{dn} \end{bmatrix} + \begin{bmatrix} V_n \\ V_n \\ V_n \\ V_n \\ V_n \\ V_n \\ 2V_n \end{bmatrix} \quad (1)$$

The last row of Eq. 1 represents the voltage loop equation of the active filter pole multiplied by two. Summing the seven rows of Eq. 1 yields:

$$V_n = \frac{V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + 2V_7}{8} \quad (2)$$

because $I_1..I_7$ sum to zero (when no leakage currents to ground exist) and $V_{an}..V_{dn}$ sum to zero if the initial charge of the filter capacitors, C_f, is zero.

The expression in Eq. (2) is defined as the common mode voltage produced by the inverter. When the leakage current due to capacitive coupling from the load to ground is present the common mode voltage is still defined by Eq. 2; but the deviation of the filter neutral voltage, V_n, from Eq. 2 increases as the leakage current increases.

The common mode voltage can be controlled to zero by properly modulating the inverter switches. This is accomplished by always setting half of the voltages in Eq. 2 to $+V_{dc}/2$ and the other half to $-V_{dc}/2$. Since V_7 acts as a double inverter pole, because it is multiplied by 2, four of the other pole voltages are always $+V_{dc}/2$ or four are always $-V_{dc}/2$. This constraint guarantees that the common mode voltage created by the inverter, defined in Eq. 2, will always equal zero. It can be shown that thirty switching states exist that make the common mode voltage equal zero (out of the possible 64 switching states) for the topology shown in Fig.1. Given this modulation constraint, nearly any conventional modulation strategy can be used to control the inverter. In this paper a novel hysteresis modulation strategy has been devised to control the active topology shown in Fig.1. A set of three phase currents is generated as references for the currents in phases A,B and C. In addition the currents on each of the six phases are controlled to be half of the reference current amplitude. Every time the error output of any of the six comparators exceeds the hysteresis band, the six errors are ranked from highest to lowest by the controller. Next, the controller determines whether four of the inverter legs will be tied to the positive DC bus or whether four of the inverter legs will be tied to the negative DC bus. Once the switch states of phase 1..6 are determined, then the switching state of the active filter is set such that Eq. 2 is zero. In particular, if four of the six pole voltages are equal to $+V_{dc}/2$ ($-V_{dc}/2$), then the lower (upper) switch in phase 7 is turned on. The modulation strategy is simple to implement using two generic PROMs and a PLD.

III. SIMULATION RESULTS

In order to prove that the common mode voltage is reduced by the active filter, computer simulations of the system have been performed by using ACSL (Advanced Continuous Simulation Language). The inverter in Fig. 1 was simulated together with input and output EMI π filters in order to meet EMI standards on conducted EMI. Simulations of the system with and without the seventh pole were performed for comparison.

For the six pole - three phase inverter and for the active filtering topology two different sets of values for the π filter have been selected, as shown in Table I.

TABLE I
COMMON MODE π FILTER COMPONENT VALUES

	3-phase inverter	New inverter
Inductance	20 mH	0.5 mH
Capacitance	2000 nF	50 nF

In addition to the EMI filters, a line impedance stabilization network (LISN) model was connected to the DC input as described in MIL-STD-461D to measure conducted emissions on DC power leads.

Figs 2 and 3 show the simulated LISN voltage depicting the electromagnetic emissions produced by a the six pole and seven pole inverter, both driving a three phase RL load.

In contrast to the six pole inverter (Fig. 2), Fig. 3 shows that the active filter can achieve the same conducted EMI levels. The active filtering realizes an enormous reduction in the size of the π filters needed to meet the EMI goal. This result predicts a significant reduction in filter volume, cost, and losses.

Fig. 4 shows the output line to line voltage and phase current for the seven pole topology. Fig. 5 contrasts the current in one of the active power poles with the current in the seventh pole. For a balanced load the seventh pole current is derated with respect to the active power poles.

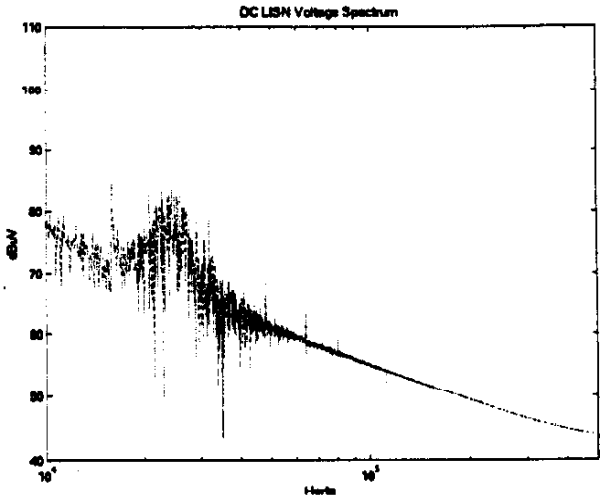


Fig. 2 – Spectrum of DC LISN voltage with 6 phase inverter

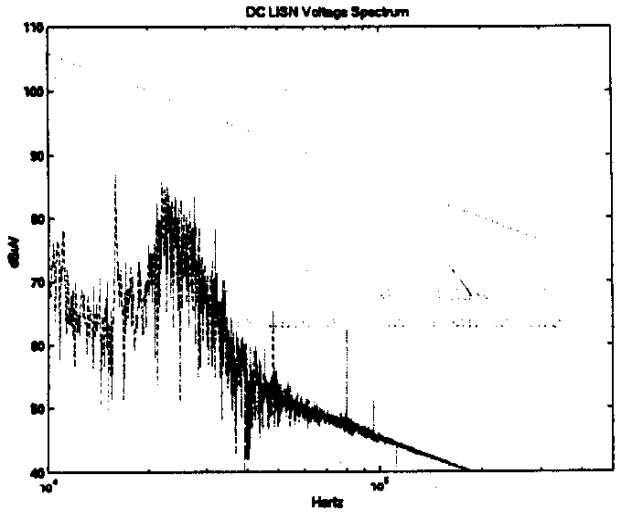


Fig. 3 – Spectrum of the DC LISN voltage for the new active topology

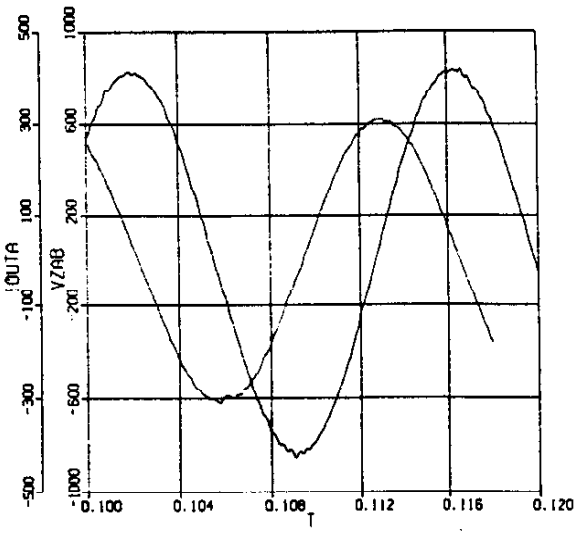


Fig. 4 – Output line to line voltage (smaller) and output phase current (larger)

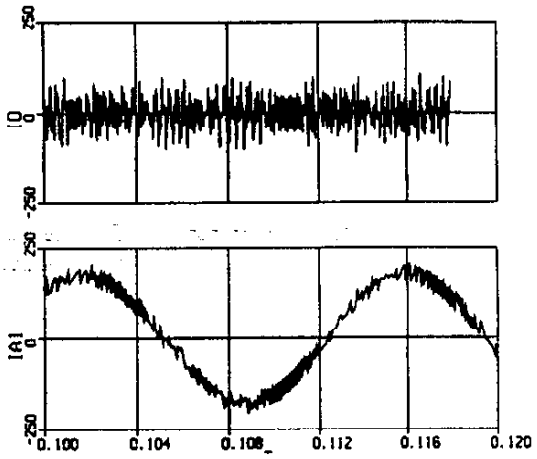


Fig. 5 – Simulated currents in phase 1 (I_1) (bottom) and phase 7 (I_7) (top)

IV. EXPERIMENTAL RESULTS

The DC to AC converter shown in Fig. 6 was built and partially tested. For the lab configuration a π filter was used between the DC input and the inverter. This filter is necessary to meet MIL-STD-461D CE102 EMI limits at the DC input port of the system. On the output of the inverter a second order filter is used to achieve sinusoidal output voltage and current. The output common mode choke limits circulating currents if the load is capacitively coupled to ground.

Hysteresis modulation is used to control the inverter in this case. The first step toward full operation of the circuit in Fig. 6 was to verify the hysteresis regulation of three phases alone and then all six phases together. Figs. 7 and 8 show the output current and the inverter line to line voltage (V1-V3) for three phase and six phase operation, respectively. Three phase operation was realized using phases 1, 3 and 5. A three phase resistor (17Ω/phase) was used as the load for these measurements. It can be noted that when six phase operation is implemented some additional distortion in the load current occurs. This distortion will be eliminated when an outer voltage control loop is added to the system.

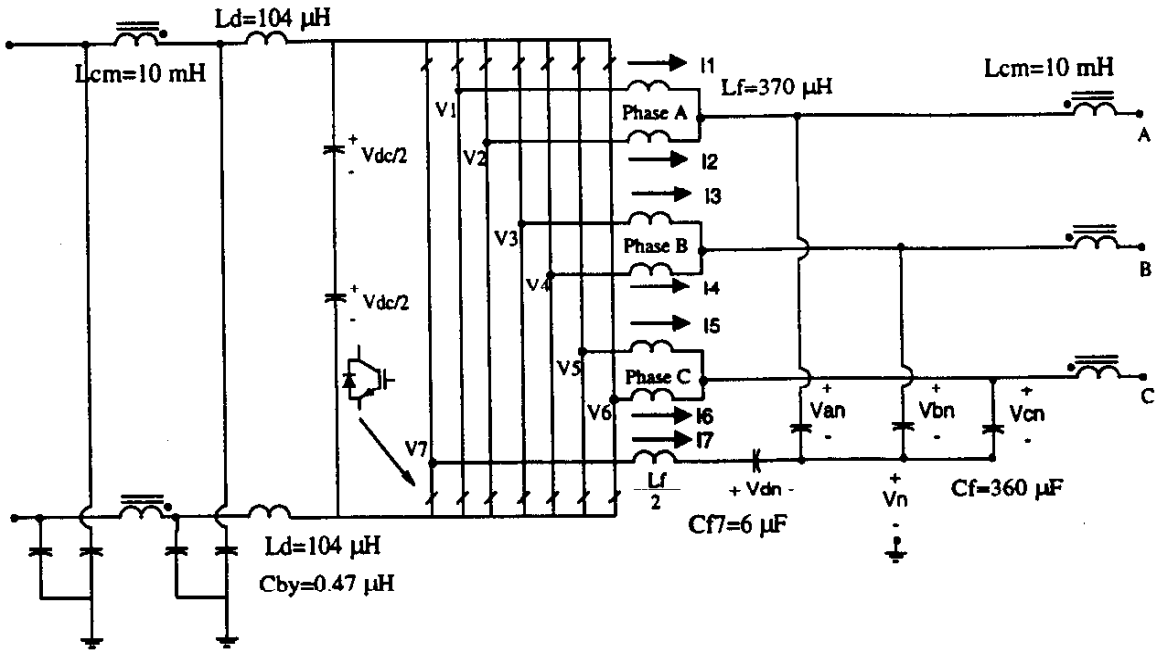


Fig. 6 – Inverter built in the lab for experimental measurements

In order to establish the conducted emission levels, a line impedance stabilization network (LISN) was connected to each DC input terminal. In Figs. 9 and 10 the common mode conducted EMI at the LISN terminals are presented for three phase and six phase operation, respectively. The measurements are a single sweep of the spectrum with a sweep rate of 30 ms. The spectrum analyzer used for these tests was a HP ESA-L1500A 9 kHz to 1.5 GHz.

In Figs. 9 and 10 the emission levels are contrasted with the EMI limits defined by MIL-STD-461D, CE102. Since the DC bus voltage was 300V a 10 dB relaxation is used to determine the EMI limit. This is offset by a 10 dB attenuation introduced by the 'transient limiter' used to protect the spectrum analyzer. These preliminary measurements indicate that the filter design is adequate to meet MIL-STD-461D conducted EMI limits for operation at 300 VDC input. In fact the EMI shown in Figs. 9 and 10 are approximately 20 dBµV below the EMI limits; it is expected that this inverter will meet the EMI limits when operated at 750 VDC input, for which it was designed

It should be noted that the emission peak at 500 kHz (and the harmonics of 500 kHz) is due to the universal power supplies used for gate drives, LEMs, fans and control power. Fig. 11 shows the conducted EMI emissions when the universal power supplies are energized but the converter is *not modulating*.

At present the active filtering of the inverter has not yet been completed. It is expected that the size to the common mode chokes in the topology of Fig. 6 will be reduced when the seventh inverter pole, the active filter pole, is implemented. Challenges such as filter resonance, and controller bandwidth, both of which effect the active filter performance, are presently being addressed and will be reported in a future paper.

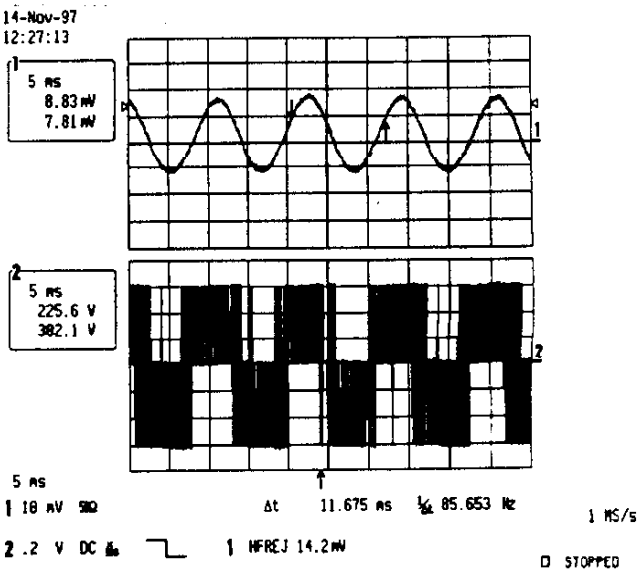


Fig. 7 – Time domain measurements for three pole operation. Top: I_A 5A/div. Bottom: V_{13} 100V/div.

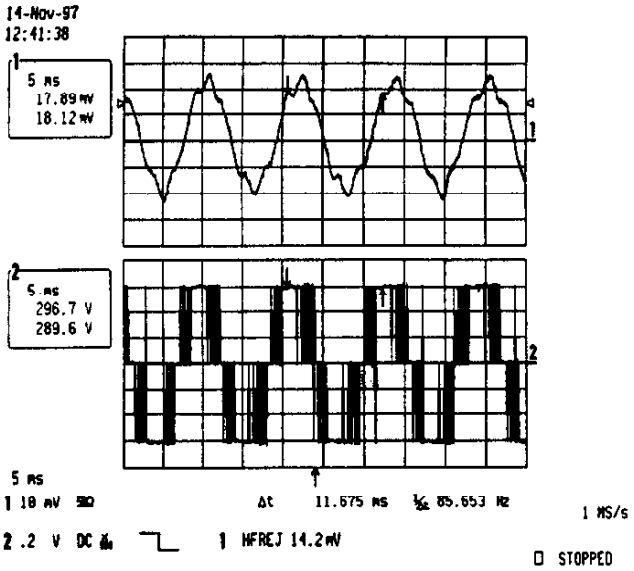


Fig. 8 – Time domain measurements for six pole operation. Top: I_A 5A/div. Bottom: V_{13} 100V/div

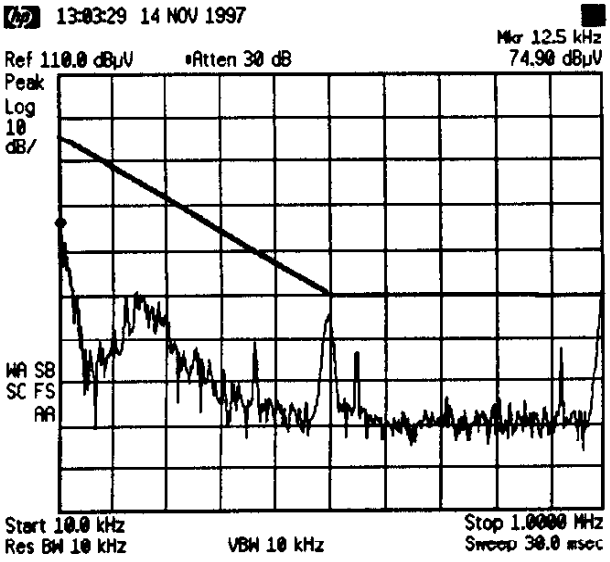


Fig. 9 – EMI conducted emission for three pole operation

V. CONCLUSION

The active filter topology presented in this paper represents one possible combination of hardware and control to effectively eliminate the common mode voltage produced by a three phase VSI. The analysis presented suggests that the common mode filter size can be substantially reduced by active filtering.

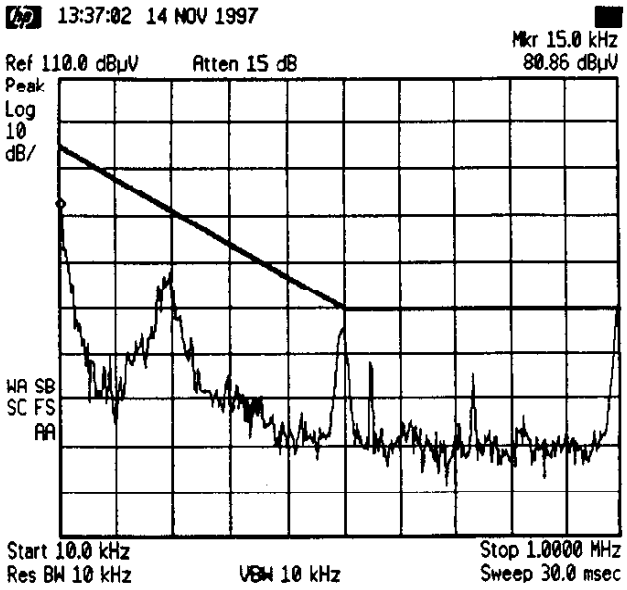


Fig. 10 – EMI conducted emission for six pole operation

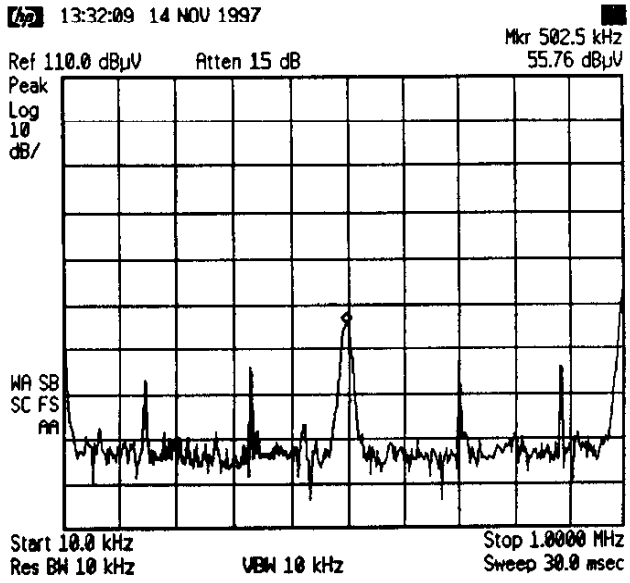


Fig. 11 – EMI conducted emission due to universal power supplies and background noise

A seven pole inverter has been built and partially tested. The three pole and six pole operating modes have been demonstrated to meet conducted EMI limits. Simulation results indicate that the active filter can achieve the same EMI limits while reducing the filter component sizes. This operating mode is currently being assembled and tested. EMI tests on the hardware confirm the low predicted EMI conducted emission.

ACKNOWLEDGMENTS

Many engineers are contributing to the fabrication of the power converter. The authors would like to thank Andy Rockhill, Raymond Marion, Eric Benedict, Mike Shannon at the University of Wisconsin-Madison, and Rebecca Mathiasen at Eaton Corporation.

REFERENCES:

[1] H. Ott., "Noise Reduction Techniques in Electronic Systems", J. Wiley & Sons, 2nd edition, 1988

[2] A.L. Julian, T.A. Lipo, G. Oriti, "Elimination of Common Mode Voltage in Three Phase Sinusoidal Power Converters", PESC'96, Baveno, Italy, 24-27 June 1996, pp. 1968-1972, vol. II.

[3] G. Oriti, A.L .Julian, T.A. Lipo, "A New Space Vector Modulation Strategy for Common Mode Voltage Reduction", Proc. of PESC'97, St. Louis, MO, USA, June 22-27, 1997.

[4] G. Oriti, A.L .Julian, T.A. Lipo, "An Inverter/Motor Drive wthout Common Mode Voltage", Proc. of IEEE-IAS'97, New Orleans, LA, Oct 5-9, pp.

[5] MIL-STD-461, Requirements for the Control of Electromagnetic Interference Emissions and Susceptibility.

[6] MIL-STD-462D Measurement of Electromagnetic Interference Characteristics, Jan 1993.