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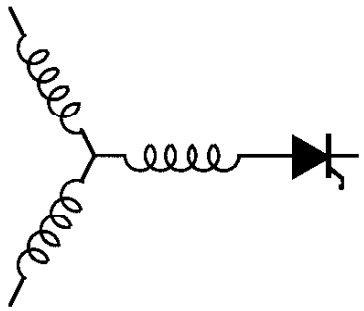
W.E. Brumsickle, D.M. Divan*, T.A. Lipo

Wisconsin Power Electronic
Research Center
University of Wisconsin-Madison
Madison WI 53706-1691

* Soft Switching Technologies Corp.
2224 Evergreen Rd., #6
Middleton, WI 53562



Wisconsin
Electric
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University of Wisconsin-Madison
College of Engineering
Wisconsin Power Electronics Research Center
2559D Engineering Hall
1415 Engineering Drive
Madison WI 53706-1691

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William E. Brumsickle*, Deepak M. Divan**, and T.A. Lipo*

*Dept. Electrical and Computer Engineering
University of Wisconsin—Madison
1415 Engineering Dr.
Madison, WI 53706 U.S.A.
http://www.engr.wisc.edu/consortia/wempec

**Soft Switching Technologies Corp.
2224 Evergreen Rd., #6
Middleton, WI 53562 U.S.A.
http://www.softswitch.com

Abstract— **High Voltage (3.3–4.5 kV) Insulated Gate Bipolar Transistors (HVIGBTs) are limited in SOA and ability to be effectively used in hard switched 2-level PWM inverters. The proposed operation sequence for the well known 3-level inverter allows use of HVIGBTs at near-rated voltage while cutting switching loss in half and allowing 3-level PWM for improved harmonics spectrum. Simulation and laboratory results prove the concept.**

I. INTRODUCTION

High voltage (3.3–4.5 kV) insulated gate bipolar transistor (HVIGBT) modules are now commercially available from several sources, with current ratings up to 1.2 kA. These isolated-base Integrated Power Modules (IPMs) include a freewheeling diode part, and would seem to be capable of controlling megawatts in voltage-source inverter (VSI) applications. Nearly-snubberless operation of such IPMs in medium voltage industrial and traction motor drives is eagerly anticipated by drives manufacturers to replace bulky and expensive GTO inverters. But the switching safe operating area (SOA) of these HVIGBTs is limited at present, as demonstrated in Fig. 1 [1]. Hence, the IPMs must be significantly derated for hard-switched inverter use, especially with minimal snubber networks. In addition, switching frequency must be limited because the relatively slow switching times of these HVIGBTs (compared with 1200 V IGBTs) results in high switching losses.

In this paper the authors propose that a three-level inverter structure [2], distinct from the familiar neutral-point-clamped (NPC) inverter [3], be revived for the purpose of reducing SOA requirements and switching losses for high voltage IGBTs in a medium-voltage VSI. A control sequence is proposed in which a mid-level voltage is applied only during switching events, so that the main HVIGBTs hard switch at 50% voltage—and 50% switching loss—and the auxiliary switches operate with low rms current. Midpoint capacitor charge tends to be conserved with such operation in three phase inverters under two-level pulse width modulation (PWM).

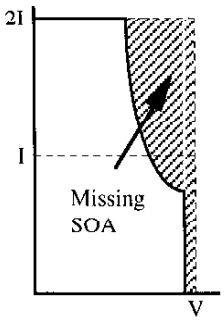

Fig. 1. HVIGBT SOA

The resulting inverter can operate at higher voltage and current levels than a conventional two-level VSI using the same main bridge HVIGBTs. Because these HVIGBT modules are relatively large and expensive, the proposed inverter offers a cost-effective means of incrementally increasing inverter power throughput without parallel connection of modules. Alternatively, the savings in switching loss may be applied to doubling the switching frequency, and three-level PWM algorithms may be applied to further reduce the output voltage harmonics content by a factor equivalent to a 2.7 times increase in switching frequency [2, 3], for an overall effective switching frequency improvement of 5.4 times.

II. THE 3-LEVEL CONVERTER STRUCTURE

The proposed inverter topology is shown in Fig. 2. It is an example of the multilevel PWM inverter structure proposed by Bhagwat and Stefanovic [2], and independently by Nabae, et al., as the "second type of NPC-PWM inverter" [3], in 1980. The designations v_{in}, v_a, etc. refer to the node voltage with respect to the negative terminal of the DC source. The IPMs S_1/D_1, S_2/D_2, etc. comprise the main two-level VSI. The auxiliary IGBTs S_{a1} and S_{a2} provide the means of

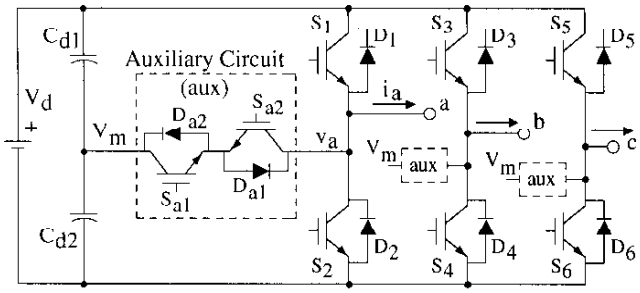

Fig. 2. The 3-Level Inverter Structure.

clamping the output voltages v_a, v_b, v_c to the midpoint level v_m. These IGBTs can be rated at 0.5 p.u. voltage. The diodes D_{a1} and D_{a2} are required because IGBTs typically do not block reverse voltage. Identical auxiliary circuits are required for each phase leg; the midpoint voltage node is common to all three auxiliary circuits. This structure is the limiting case of the Auxiliary Resonant Commutated Pole Inverter (ARCPI) [5] when the resonant components are replaced by parasitic inductances and device capacitances.

III. QUASI 3-LEVEL INVERTER (Q3I) OPERATION.

The inverter of Fig. 2 can be operated with conventional two-level PWM algorithms, while using the third (midpoint) voltage level only during switching transitions. This is termed "quasi 3-level inverter" (Q3I) operation. The Q3I operation limits main HVIGBT voltage and current stress to 1.0 p.u. during conduction, and somewhat more than 1.0 p.u. current and 0.5 p.u. voltage during switching events—a 50 percent reduction in switching stress compared to two-level hard switching. Proper control sequencing requires only a current polarity sensor for each phase current and insertion of *fixed* time delays. The operating modes of the inverter are described next for the case of positive load current i_a, with the aid of the timing diagram, Fig. 3. Switching waveforms from a Saber [4] simulation with realistic device models, but no stray inductances, are shown in Fig. 4.

A. Commutation from an HVIGBT (S_1) to a diode (D_2).

Consider first the case where an IGBT (S_1) is initially conducting, and a modulator command to turn off the IGBT (S_1) is received (at t = 100 μs in Fig. 4). Gate drive logic signals are issued in the sequence illustrated in the left half of Fig. 3:

1. Immediately turn on the appropriate auxiliary IGBT:
   - If phase current i_a is positive, turn on device S_{a1}.
   - If phase current i_a is negative, turn on device S_{a2}.

   Then wait a time t_1 (2.1 μs) for the auxiliary IGBT (S_{a1}) to increase conductivity. The series auxiliary diode (D_{a1}) remains reverse biased throughout this interval. Note that device turn-on delays are modeled.

2. Turn off the main device (S_1).
   The load inductance causes the output voltage v_a to drop until the series auxiliary diode (D_{a1}) becomes forward biased. If stray inductances are not too high, the auxiliary branch will supply the load current and clamp the output voltage at the midpoint level V_m.
   Then wait a time t_2 (5 μs) for the IGBT (S_1) to substantially decrease its conductivity.

3. Turn off the auxiliary IGBT (S_{a1}).
   The load inductance causes the output voltage v_a to drop until the opposite diode (D_2) becomes forward biased to clamp the output voltage at the negative DC bus rail.
   Then wait a further time t_{2a} (5 μs) for the auxiliary IGBT (S_{a1}) to substantially decrease its conductivity *and* for the main IGBT (S_1) to have reached the forward blocking state.

4. Turn on the opposite main IGBT (S_2).
   The anti-parallel diode (D_2) is already conducting, so the turn-on is at zero current and zero voltage.
   Then wait a further time t_{off} (7 μs), at least long enough for the incoming IGBT (S_2) to reach full conductivity, before allowing another switching cycle to begin. Modulator commands are locked out during the commutation cycle

B. Commutating from a diode (D_2) to an HVIGBT (S_1).

Consider next the case where a diode (D_2) is initially conducting when a modulator command to turn on the IGBT (S_1) is received (at t = 130 μs in Fig. 4). Gate drive logic signals are then issued as shown in the right half of Fig. 3, and explained below

1. Immediately turn off the opposite main IGBT (S_2). This IGBT turn-off occurs at zero voltage and zero current.
   Then wait a time t_{3a} (3 μs) for the IGBT (S_2) conductivity to decrease.

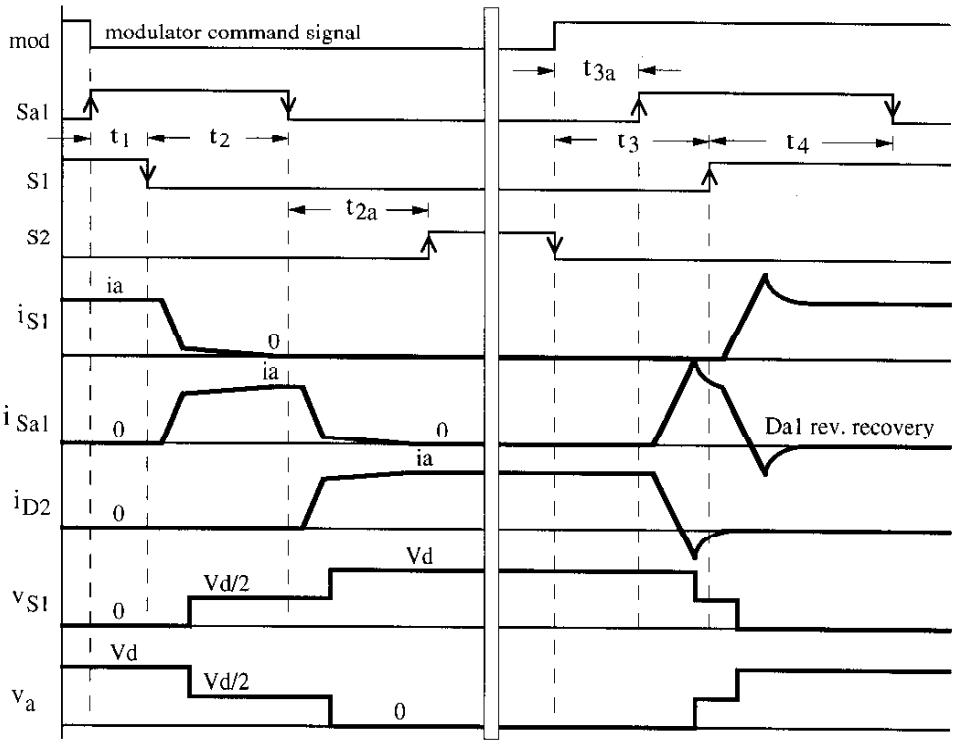

Fig. 3. Simplified Q3I switching sequence timing when $i_a > 0$.

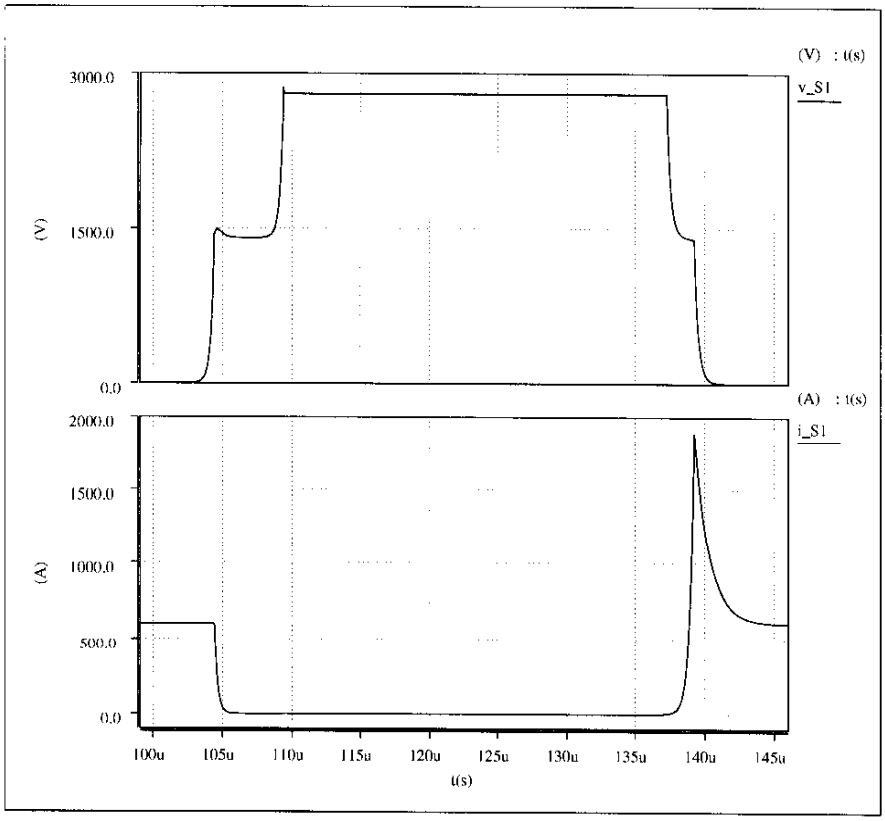

Fig. 4. Switching Waveforms Without Stray Inductance: S_1 voltage (top), S_1 current (bottom).

2. Turn on the appropriate auxiliary device:
   • If phase current i_a is positive, turn on device S_{a1}.
   • If phase current i_a is negative, turn on device S_{a2}.
   Then wait a further time, $t_3 - t_{3a}$ (2 μs) for the auxiliary IGBT (S_{a1}) to increase conductivity *and* for the opposite IGBT (S_2) to reach a forward blocking state *and* for the opposite diode (D_2) to complete its reverse recovery. Hence t_3 (5 μs) is at least as long as the total turn-off time for a main IGBT carrying zero current, and may be longer. Once conductivity is established in the auxiliary devices (S_{a1} and D_{a1}), the voltage $V_d/2$ across the stray circuit inductances increases the auxiliary branch current until it reaches the level of the load current. The main diode (D_2) then begins reverse recovery. If the turn-on di/dt of the auxiliary device is controlled then the main diode recovery current will be controlled.
3. Turn on the main device (S_1).
   Then wait a time t_4 (7 μs) for the incoming IGBT (S_1) to take over current from the auxiliary devices (S_{a1} and D_{a1}). The reverse recovery current of the auxiliary series diode (D_{a1}) will increase the turn-on current in the main device (S_1); the magnitude of this recovery current can be reduced by slowing the turn-on of the main IGBT (S_1)
4. Turn off the auxiliary device (S_{a1}).
   Then wait a time t_{off} (7 μs).
5. Allow another commutation cycle to begin.

The large i_{S1} current spike observed in Fig. 4 is caused by reverse recovery current in diode D_{a1}.

Each of the time delays t_1-t_4 is fixed and predetermined. The total length of the commutation process is approximately 14 μs in this example, on the same order as two level hard switching when required dead time is included.

IV. Q3I DESIGN ISSUES

If stray inductance L_p between the auxiliary devices and the main bridge devices is large, the HVIGBTs will tend to switch at full voltage. With smaller parasitic inductance, commutation will be delayed and L_p will form a resonant circuit with device capacitances possibly causing actual device voltages to oscillate to greater than 0.5 p.u. during switching. Voltage transients due to reverse recovery current of the auxiliary diodes into the stray inductance, can be severe. These reverse recovery effects can be controlled by slowing the main HVIGBT turn-on by gate control to reduce di/dt and stored charge in the diode. As a last resort, an auxiliary diode snubber network could be added.

Figure 5 shows the Saber simulation result for the same conditions as in the earlier Fig. 4, but now with realistic device models, stray inductances and device capacitances. Only the second transition, turning on HVIGBT S_1, is shown here. The control timing is identical to the earlier case. Reverse recovery current of the main diode D_2 flows into the auxiliary devices, and a parasitic oscillation of device voltages v_{S1} and v_{D2} occurs when D_2 finally snaps off with high di/dt. But this oscillation does not affect switching loss because S_1 is not yet carrying current. Now when S_1 conducts the reverse recovery current of D_{a1} (at t = 139 μs), and D_{a1} snaps off, the resulting parasitic oscillation does not involve the capacitance of S_1 and so voltage v_{S1} does not show any oscillation.

The effect of holding the output voltage at $V_d/2$ for a period of time is to apply more volt-seconds to the load than were commanded by the modulator (for a high-to-low voltage transition) or less volt-seconds than desired (for a low-to-high transition). It is advantageous to designate the controller times t_1–t_4 such that the dwell time at the midpoint voltage is approximately the same for either switching transition. In this way the volt-seconds applied to the load will match the desired level when averaged over several cycles.

Load current polarity information is required before beginning the commutation sequence. Sophisticated gate drives may provide this information at little additional cost by observing device voltages; otherwise, current transformers will suffice. The consequence of incorrect polarity information is a full-voltage hard switching event. Since incorrect polarity feedback is likely to occur only around zero load current, the SOA limit of the HVIGBTs will not be exceeded, and switching loss will remain low.

Because the auxiliary devices are conducting only during PWM switching events, and switching frequencies are typically low at these power levels (on the order of 1 kHz), the rms current in the auxiliary devices is low. Hence, the four auxiliary devices in each leg could be packaged into a single module without excessive heat-sinking requirements. The total added silicon area is approximately 50 percent of that in the main inverter bridge.

To first order, the IPM switching losses are proportional to voltage. Hence, the Q3I reduces switching losses by approximately one half. The following case study demonstrates the

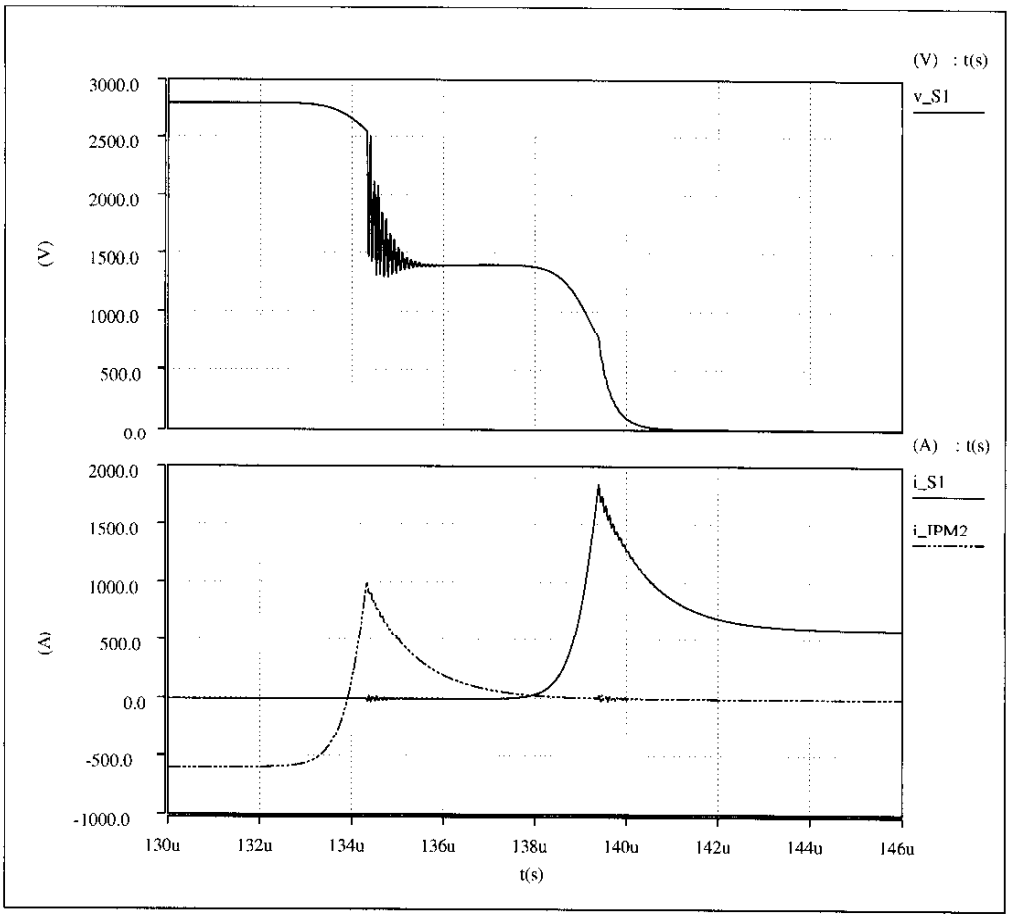

Fig. 5. IPM voltage (top) and currents (bottom), with parasitic elements included.

possible improvement in inverter power throughput using the Q3I approach.

The reduction in main HVIGBT switching loss is mostly transferred to the auxiliary IGBTs, but since these devices have very little conduction loss they can be smaller than the main HVIGBTs.

V. CASE STUDY

To demonstrate the advantage of the Q3I in concrete terms, consider the case of a three phase VSI built with commercially available HVIGBT modules: the POWEREX model CM1200HA-66H, rated for 3300 V and 1200 A [1]. A 600 Hz switching frequency is assumed. The switching and conduction losses are estimated, based on PWM at 1.0 modulation factor and sinusoidal reference. The losses and inverter output kVA are given in Table I. Also included in the table are results for the Q3I, first at the same current as for the baseline inverter, and then with increased current to provide the same total losses as in the baseline case. The VSI output kVA capability is increased by 27%.

VI. EXPERIMENTAL RESULTS

A single phase scale-model inverter was built using 1200 V, 600 A IGBT modules for the main devices and 600 V, 400 A IGBT modules for the auxiliary devices. The Q3I switching waveforms are shown in Figs. 6 and 7 for the case of positive 60 A load current and 300 V DC bus.

TABLE I.
CASE STUDY RESULTS WITH 1500 VDC BUS

	I_{OUT} (A)	Conduct. Loss (W)	Switching Loss (W)	Total Loss (W)	VSI Output (kVA)
2-level VSI	600 (rms)	714	516	1230	956
Q3I	600	714	258	972	956
Q3I	760	904	327	1231	1210

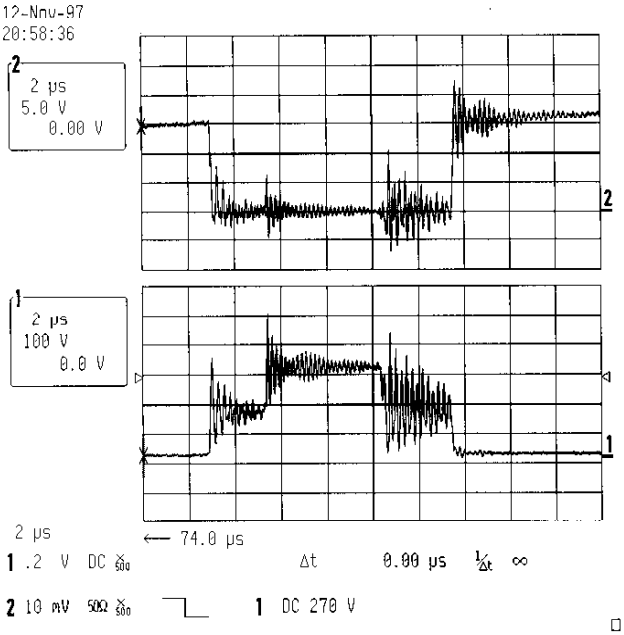

Fig. 6. Q3I lab results, turning IGBT off and on: S_1 voltage (bottom) & S_1 current (top).

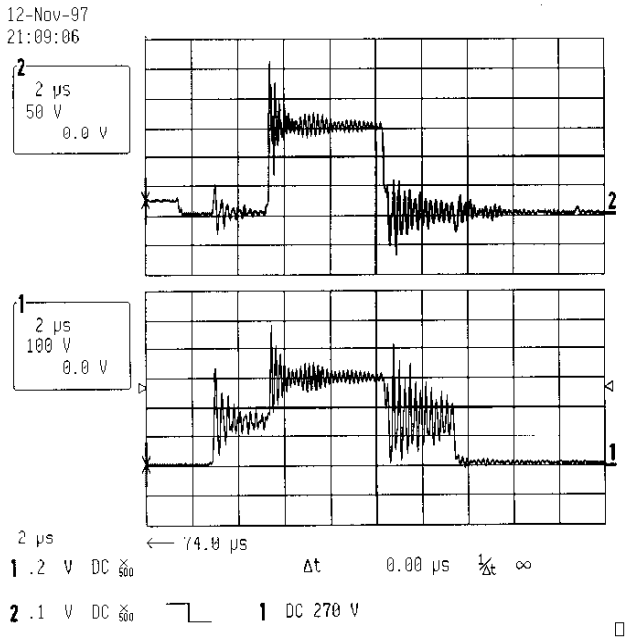

Fig. 7. Q3I lab results, turning IGBT off and on: S_1 voltage (bottom) & S_{a1} voltage (top).

The high frequency oscillations seen in the figures are the result of the module and bus parasitic inductances and the capacitor bank ESL (equivalent series inductance) ringing with the module capacitances. The oscillations would be reduced by using a laminated bus structure and adding low–ESL capacitors across the main capacitor bank. The simulation plot in Fig. 5 shows some of the same characteristics, but at a much lower level.

VII. CONCLUSIONS.

The proposed Q3I operating sequence for the three-level inverter structure:

- Increases the useful power throughput of HVIGBTs with limited SOA.
- Reduces switching loss of the main HVIGBTs by approximately one half.
- Allows 3-level PWM (for harmonics reduction: equivalent to increasing switching frequency 2.7 times).

Realistic modeling, including estimated device and packaging parasitics shows that the approach is viable. A laboratory prototype using 600 A, 1200 V IGBTs proves the concept. More detailed experimental work is under way.

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