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Fast Clamped Short Circuit Protection of IGBTs

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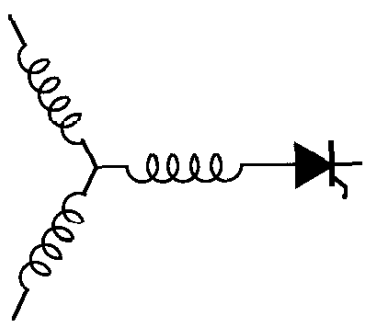

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Abstract **- Identification of fault current during the operation of a power semiconductor switch and activation of suitable remedial actions are important for reliable operation of the power converter including the power semiconductor device. A short circuit is a basic and severe fault situation in a circuit structure such as voltage source converter. This paper presents a new active protection circuit for fast and precise clamping of fault currents and safe shutdown of the IGBTs. This circuit allows operation of the IGBTs with a higher on-state gate voltage, which can thereby reduce the conduction loss in the device without compromising the short circuit protection characteristics. The operation of the circuit is studied under various conditions, considering variation of temperature, the rising rate of fault current, gate voltage value, and circuit parameters. A study of the operation of the circuit is made using IGBTs from different manufacturers to confirm the effectiveness of the protection circuit.**

Index Terms **– Fault current, Fault inductance, FUL, HSF, Protection.**

I. INTRODUCTION

Short circuit and over-current are severe fault conditions that can result in failure of the IGBT if appropriate remedial action is not taken within short time of the order of a few microseconds. It has been shown in [1] that the failure mechanism caused by short circuit is different from inductive turn-off failure case. Short circuit results in local heating closer to the gate oxide in the IGBT and can severely degrade the device. Several methods of protection are available by the use of intelligent power modules and advanced gate driver chips [2]-[4]. However, there are no benchmarks for the performance these circuits.

Various approaches have been proposed and studied to protect IGBTs in [5]-[12]. Different topologies have been investigated for fault current limiting circuits (FCLCs) in [5], [6]. The technique used in [5], which utilizes a capacitor to limit fault currents, has the limitation that the device may be shut off and turned back on again depending on the initial condition of the capacitor and its value. Also, a large value of capacitance is necessary to prevent the capacitor voltage from drifting back to the normal on-state gate voltage. Multiple stages of clamping were proposed in [5] to increase the endurance time and reduce the turn-off current level. A pure zener based clamp has the drawback that the clamping voltage can be much larger under the transient conditions of the fault. Reference [6] discusses a topology where the zener and capacitive method is used to limit fault currents. This circuit is effective in eventually clamping the fault current level but does not limit the large peak current that flows immediately after the fault due to delay in its operation. References [7]-[12] discuss methods to softly turn off the IGBT after the fault and to reduce the over-voltage due to the turn-off di/dt. This feature is to control the over-voltage caused by the parasitic inductance of the power circuit while turning off a large current.

This paper focuses on the following study issues for active protection of fault current for IGBT modules:

- Use of a large on-state gate voltage to reduce conduction losses makes the fault situation more problematic and dangerous, because it leads to very high fault current. This results in very large instantaneous power dissipation [13] and the possibility of latching in the device. Therefore, there is a trade-off between the short circuit current magnitude and conduction loss;
- Precise detection of fault current levels is a challenging issue if current sensors are not used in series with the IGBTs. In particular, in case of soft fault (large fault inductance), it is very difficult to precisely recognize the over-current condition using the de-saturation technique which is the general method used to detect fault current. This is due to the reduced voltage drop in the IGBT under low di/dt conditions as well as the slow dynamics in the electronic components in the detection circuit;
- Fast detection and reliable handling of fault currents are important study issues. The initial value of short current is the highest due to the increased gate voltage caused by the Miller capacitance. It is not easy to mitigate the initial peak current, because activation of protection circuit should be prevented under transient conditions such as IGBTs' turn-on and turn-off, and switching noise;

- At shutdown, the falling rate of the current should be controlled to reduce the over-voltage stress. The over-voltage level across the device can become much larger than the rated voltage, if the large collector current is turned off without any treatment. While using a FCLC, soft turn-off is also required to take into account possible changes in the operating modes of the protection circuit.

For the study mentioned above, experimental investigation on the fault situation is performed in detail based on the variation of temperature, the rising rate of fault current, positive gate voltage level, and circuit parameters. A new active protection method is proposed, which can limit fault currents to a reasonable level while suppressing the initial peak current value and safely shut down the IGBTs. Test results are given by using IGBTs from different manufacturers to study operation of the protection circuit under varying device parameters.

II. OPERATION CHARACTERISTICS OF THE PROPOSED ACTIVE PROTECTION CIRCUIT

Fast detection of the occurrence of the fault, limiting of the initial peak current, clamping of the over-current, and safe shutdown are essential features of the protection circuit. Fig. 1 shows the schematic of the proposed circuit, which is composed of the basic drive circuit, three feedback lines, and the additional protective control circuit. Major operational functions of the circuit are explained.

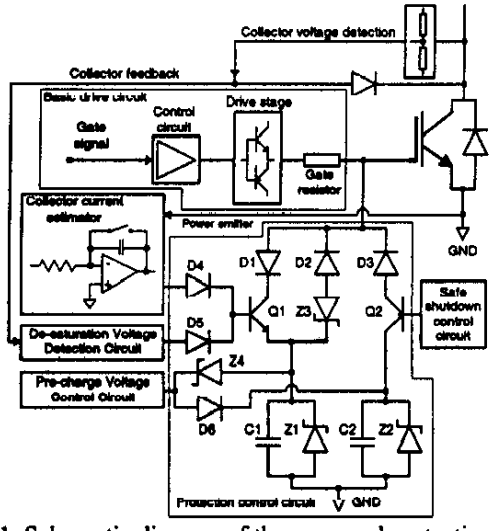

Fig. 1. Schematic diagram of the proposed protection circuit.

A. Detection

The detection of fault current is based on two inputs into the control circuit. One is the de-saturation voltage of the device. The other is the voltage drop between the power and the Kelvin emitter terminals of the device. The connection between these two terminals is modelled as an inductor. This allows an estimate of the device current level that is obtained using a resettable integrator circuit as shown in Fig. 1. The parameters of the integrator are mainly based on circuit loading and parasitic capacitance of the reset switch. The de-saturation voltage detection has a rapid response to low impedance (hard fault) fault under load (FUL) condition. The device current estimator is more effective to detect soft fault (high inductance) situations. Direct measurement circuit, which is added to collector feedback line in Fig. 1, of the collector voltage is used to rapidly recognize hard switched fault (HSF) condition and to distinguish it from normal switching transients of the IGBT [12].

B. Limiting

Limiting of the current is obtained using the capacitor, C_1, and the zener diode, Z_1, for fast and stable protection. On detection of fault the transistor, Q_1, is turned on, which causes C_1 to charge up to the voltage level of Z_1, thus discharging the gate. The transistor is activated by the combination of collector current estimate and de-saturation voltage, which is obtained by the diodes D_4 and D_5. A large C_1 results in initial oscillation in the device current and a slow ramp up to the clamp current level. A small value of C_1 results in increased peak fault currents due to insufficient gate discharge. The zener diodes, Z_3 and Z_4, make the voltage of C_1 to be at the desired voltage level before turning on the IGBT. This pre-charge voltage compensates for the delay in operation of the protection circuit. A lower pre-charge voltage will result in the activation of the protection circuit at an earlier instant. The on-state voltage of the IGBT and the voltage drop along the de-saturation circuit path limit the minimum value of the pre-charge voltage.

C. Clamping

The final gate voltage level is clamped by the zener Z_1. The value of the zener voltage is selected to be above the threshold voltage and depends on the transconductance gain of the driven IGBT. The voltage drops across the transistor, Q_1, and the diode, D_1, have to be considered while selecting the zener diode, Z_1. The clamped gate voltage decides the IGBT clamp current level.

D. Shutdown

The capacitor C_2 is placed in parallel with the gate capacitance to turn off the IGBT at a reduced dV_{ge}/dt. The pre-charge level of C_2 is higher than the gate voltage level used for clamping due to the voltage drop corresponding to the conducting paths of the shutdown circuit. The current path during shutdown changes from D_1-Q_1-Z_1 to C_2-Q_2-D_3. This eliminates small notch in the gate voltage caused by the reversal of current from the clamping mode to the safe

shutdown mode. The purpose of the diode, D_6, is to obtain decoupling between the pre-charge voltage levels for C_1 and C_2. The zener diode, Z_2, determines the pre-charge level of C_2.

E. Fault Monitoring

Nuisance faults signals can be rejected strongly because the main fault signal sent to the system controller occurs based on the measured V_{ce} information. Also, a delay time of a few microseconds is used to report the fault information allowing for momentary transient in the current that could occur without damaging the device. These momentary transients are also held to the clamping current level.

III. EXPERIMENTAL EVALUATION

A simple test circuit is set up to verify the validity of the

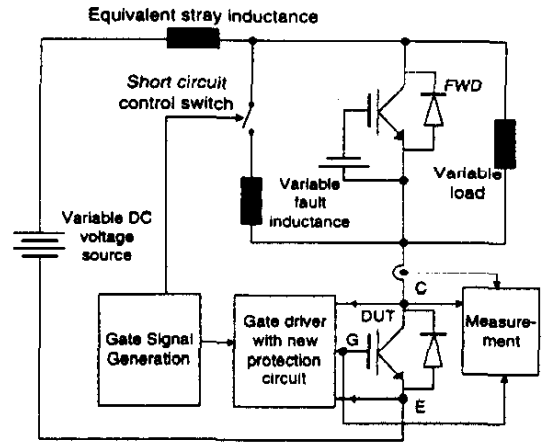

Fig. 2. Test setup.

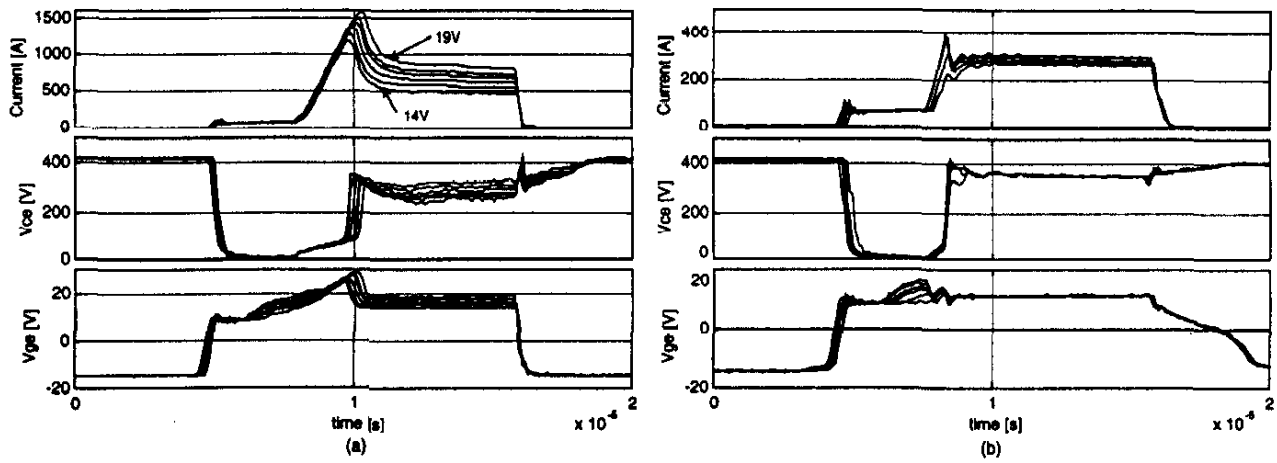

Fig. 3. FUL test results for Toshiba MG100Q2YS40 under Vge variation. (a) Without protection. (b) With protection. Selected positive gate voltages are as follows: 14, 15, 16, 17, 18, 19V. Other conditions are as follows: C_1 = 30nF, Pre-charge voltage = 4.5V, Vdc = 405V, T = 24°C, L = 200nH.

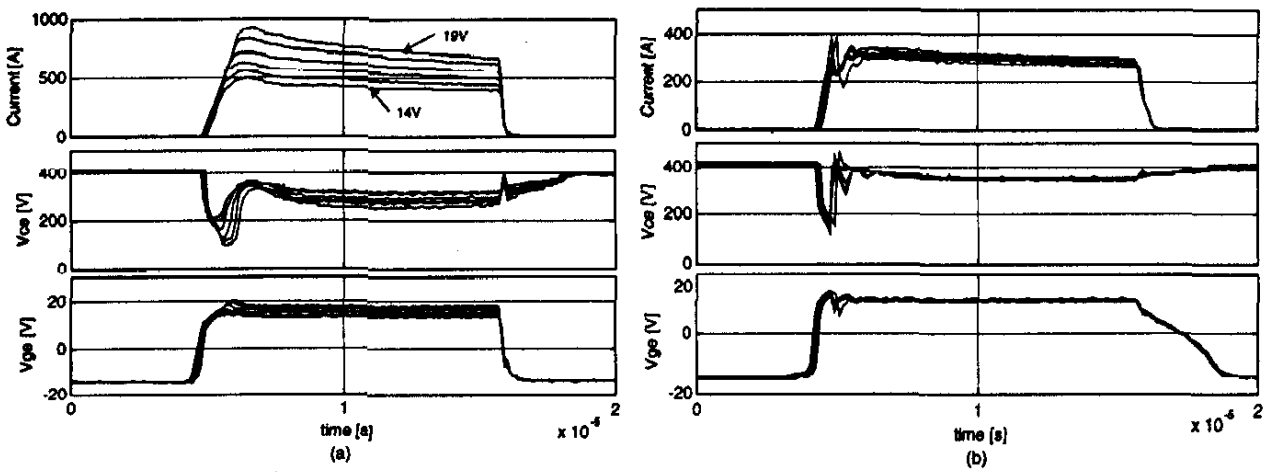

Fig. 4. HSF test results for Toshiba MG100Q2YS40 under Vge variation. (a) Without protection. (b) With protection. Selected positive gate voltages are as follows: 14, 15, 16, 17, 18, 19V. Other conditions are as follows: C_1 = 60nF, Pre-charge voltage = 5V, Vdc = 405V, T = 24°C, L = 200nH.

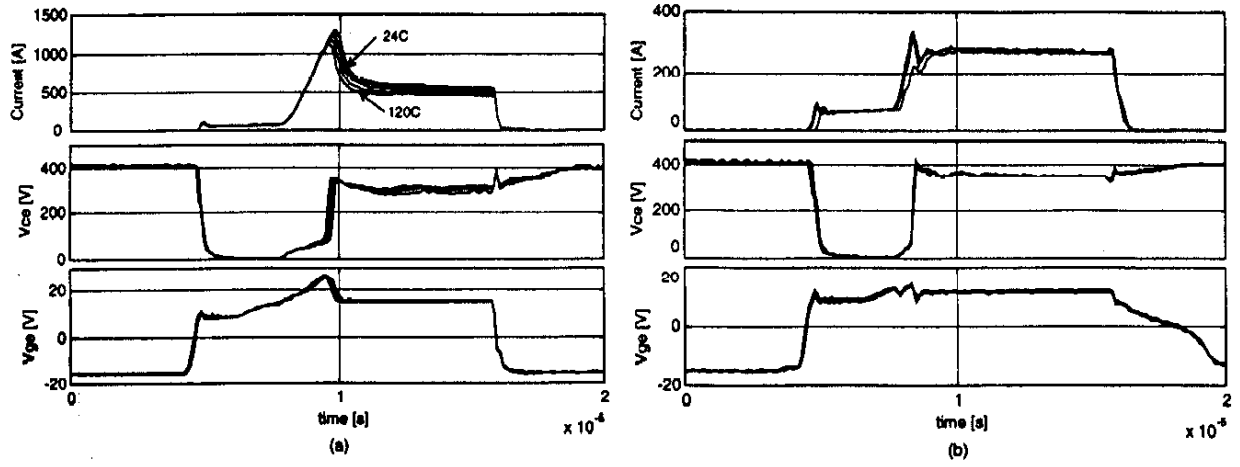

Fig. 5. FUL test results for Toshiba MG100Q2YS40 under variation of temperature. (a) Without protection. (b) With protection. Selected temperatures are as follows: 24, 40, 60, 90, 120°C. Other conditions are as follows: C_1 = 60nF, Pre-charge voltage = 5V, Vdc = 405V, Vge = 15V, L = 200nH.

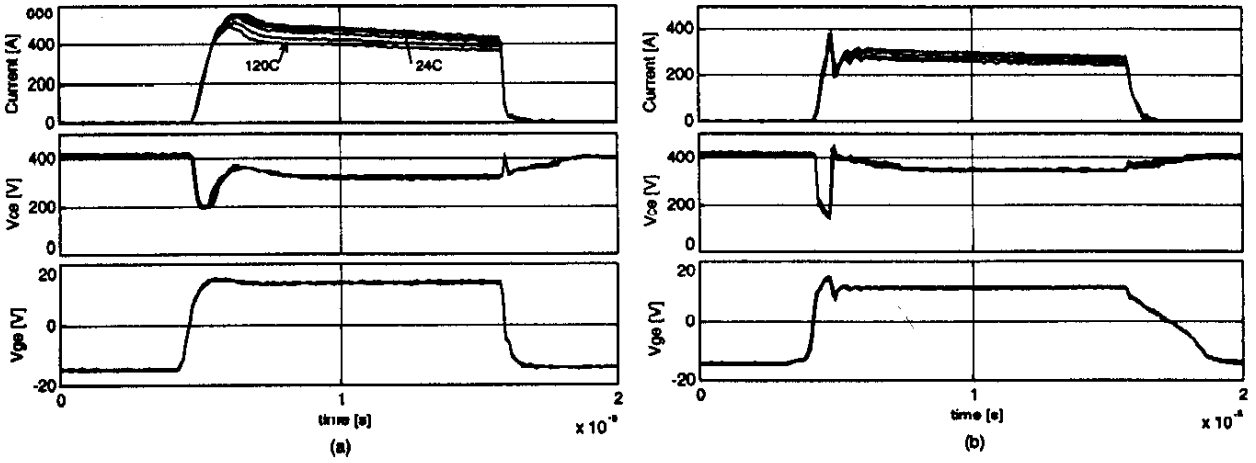

Fig. 6. HSF test results for Toshiba MG100Q2YS40 under variation of temperature. (a) Without protection. (b) With protection. Selected temperatures are as follows: 24, 40, 60, 90, 120°C. Other conditions are as follows: C_1 = 30nF, Pre-charge voltage = 4.5V, Vdc = 405V, Vge = 15V, L = 200nH.

proposed protection circuit, which is shown in Fig. 2. The test has been conducted with three different IGBTs modules - Toshiba MG100Q2YS40 (1200V, 100A), Powerex CM75DY-12H (600V, 75A), and Fuji 2MBI75-060 (600V, 75A). The measured collector current, collector voltage, and gate voltage waveforms using the Toshiba IGBT are shown in Figs. 3 to 10.

A. On-State Voltage Variation

Fig. 3(a) and (b) show the test results of fault under load (FUL) varying the on-state gate voltage, which is the parameter studied during this test. In case of no protection, which is shown in Fig. 3(a), the peak and final current levels are strongly dependent on the gate voltages. When the on-state gate voltage is 19V, the peak current is more than fifteen times of the rated current. There is not much difference in the Vce waveform. From Fig. 3(b) we can see that the fault current can be at controlled levels irrespective of the on-state gate voltage with the active protection circuit. Fig. 4(a) and (b) are for the case of HSF. Fig. 4(b) shows that the protection circuit keeps the fault current within a small envelope for a wide range of on-state gate voltage levels as in the case of FUL. On the other hand, from Fig. 4(a), it is shown that the peak and final current levels increased by a factor of two when the gate voltage was increased from 14V to 19V.

B. Temperature Variation

Figs. 5 and 6 show the effect of operating temperature for FUL and HSF respectively. The peak and final fault current decreases as the temperature is increased due to the negative temperature coefficient at high current levels. This result

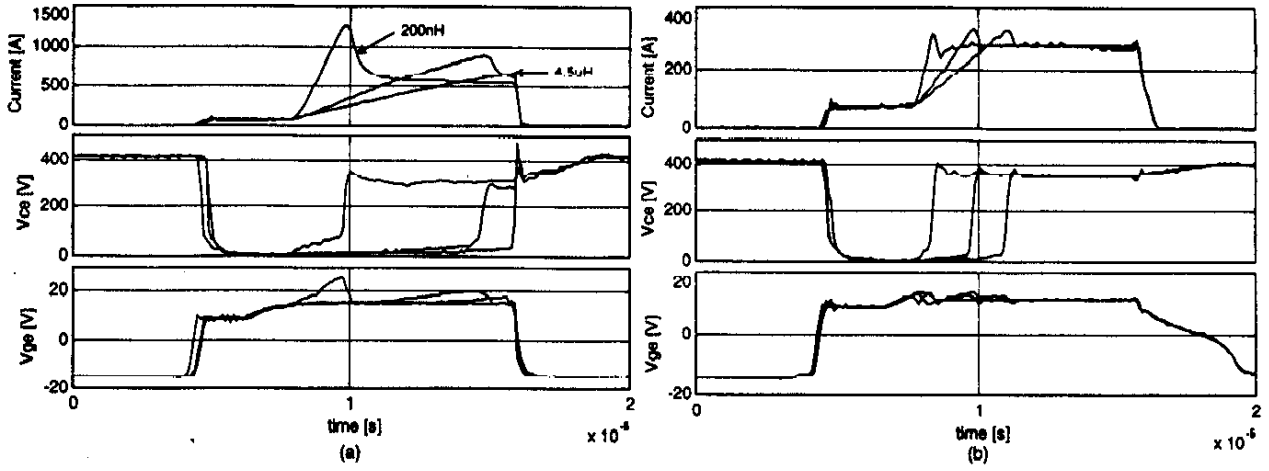

Fig. 7. FUL test results for Toshiba MG100Q2YS40 under variation of inductance. (a) Without protection. (b) With protection. Selected inductances are as follows: 0.2, 2.5, 4.5μH. Other conditions are as follows: C_1 = 60nF, T = 24°C, Pre-charge voltage = 5V, V_{dc} = 405V, V_{ge} = 15V.

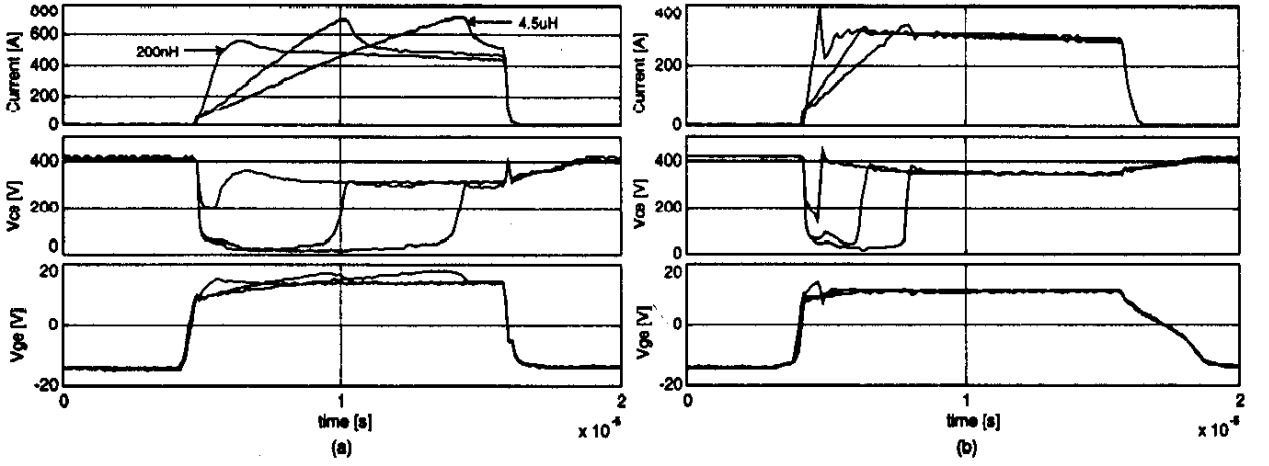

Fig. 8. HSF test results for Toshiba MG100Q2YS40 under variation of inductance. (a) Without protection. (b) With protection. Selected inductances are as follows: 0.2, 2.5, 4.5μH. Other conditions are given as follows: C_1 = 30nF, T = 24°C, Pre-charge voltage = 4.5V, V_{dc} = 405V, V_{ge} = 15V.

indicates that within the normal operating temperature range, the fault current waveform does not vary significantly if the device is turned off before breakdown. When the active protection circuit is applied, this effect becomes much smaller.

C. Fault Inductance Variation

For this test, the variable fault inductance, which is shown in Fig. 2, is varied to obtain the desired inductances of 0.2, 2,5 and 4.5μH. Fig. 7(a) shows that the peak fault current is largest for small fault inductance in case of FUL. As fault inductance increases pure de-saturation based fault detection would have a large delay in operation. As fault inductance decreases it is necessary for the protection circuit to have a quick reaction to prevent the high peak current. Therefore, it would not be possible to limit the peak fault current and to estimate the exact fault current level without using a current sensor. In the case of HSF, which is shown in Fig. 8(a), the peak fault current increases as the fault inductance is increased. At larger fault inductance, the difference between HSF and FUL becomes smaller. The active protection circuit detects and limits the fault current at the same level for a wide range of fault inductance for both FUL and HSF.

D. Circuit Parameter. C_1. Variation

Fig. 9 shows the effect of variation of the capacitor, C_1 in Fig. 1, on the response of the protection circuit for FUL and HSF. A large C_1 results in the device current reaching almost zero and then slowly building up to the clamp current level. A small C_1 is not effective in discharging the gate capacitance rapidly and results in a higher initial peak in the fault current.

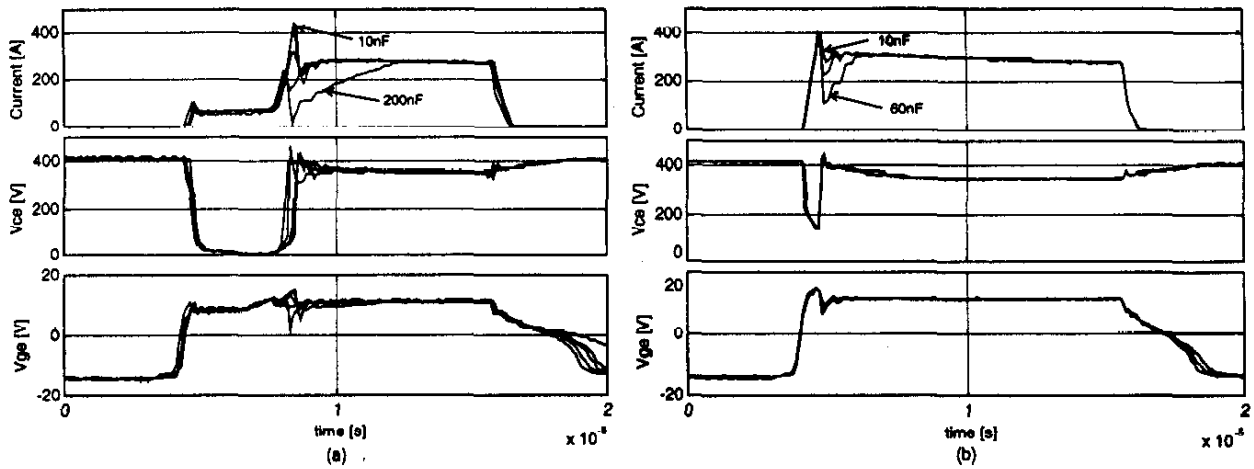

Fig. 9. Test results for Toshiba MG100Q2YS40 under variation of capacitance, C_1. (a) FUL with selected capacitance as follows: 10, 30, 60, 100, 200nF. Pre-charge is at 4.8V. (b) HSF with selected capacitance as follows: 10, 30, 60nF. Pre-charge is at 5.0V. Other conditions are given as follows: Fault inductance = 200nH, T = 24°C, Vdc = 405V, Vge = 15V.

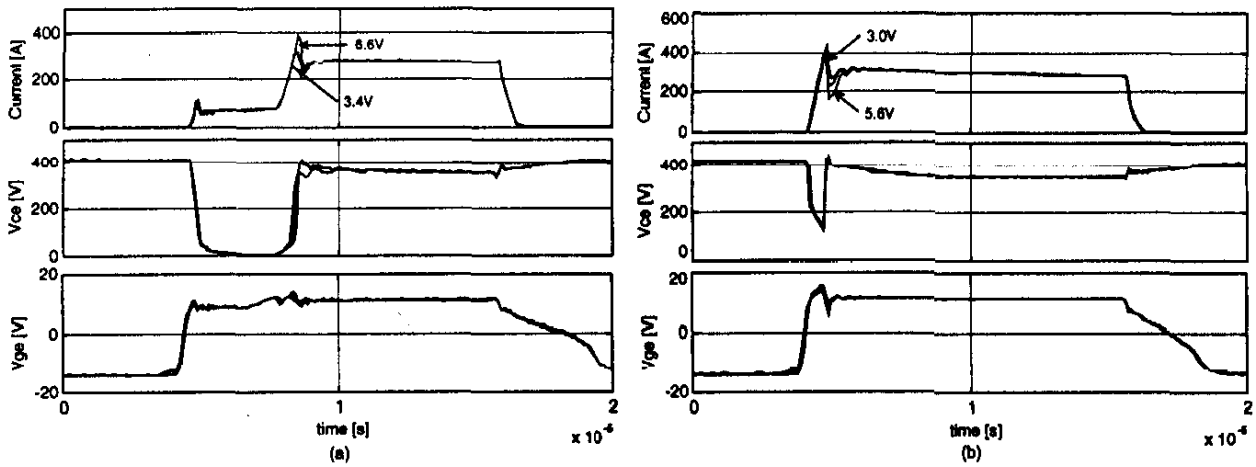

Fig. 9. Test results for Toshiba MG100Q2YS40 under variation of C_1 pre-charge voltage. (a) FUL with selected pre-charge voltage values as follows: 3.4, 4.8, 6.6V. C1 is 60nF. (b) HSF with selected pre-charge voltage values as follows: 3.0, 4.0, 5.6V. C_1 is 30nF. Other conditions are given as follows: Fault inductance = 200nH, T = 24°C, Vdc = 405V, Vge = 15V.

E. Pre-charge Voltage Variation

Fig. 10(a) and (b) show the effect of the pre-charge voltage level of the response on the protection circuit for FUL and HSF, respectively. It can be seen that lowering the pre-charge voltage is effective in lowering the initial peak in the fault current. The pre-charge voltage variation has a greater effect on FUL than HSF. This is because of the need to have a minimum delay before activation of the de-saturation detection path. This effect can be minimized by using the measured Vce voltage.

F. Analysis

Table I lists a comparison of the peak power and the energy dissipation with and without the active protection

TABLE I

PEAK POWER [kW] AND ENERGY DISSIPATION IN THE IGBT WITH AND WITHOUT PROTECTION

(Energy dissipation is normalized to 1.0 for operation without protection. Other conditions are Vge_on = 15V, Vdc = 405V, T = 24°C, L* = 200nH.)

Device	FUL		HSF	
	w/o [kW]	w [kW]	w/o [kW]	w [kW]
Toshiba MG100Q2YS40	423 (1.0)	110 (0.59)	201 (1.0)	125 (0.73)
Powerex CM75DY-12H	178 (1.0)	44.3 (0.46)	135 (1.0)	62.0 (0.48)
Fuji 2MBI75-060	156 (1.0)	55.9 (0.45)	145 (1.0)	82.5 (0.58)

* L is the fault inductance shown in Fig. 2.

circuit, for the cases of FUL and HSF for three different IGBTs. Under the given operating conditions, the peak power dissipation is reduced by a factor of 3 for FUL and by a factor of 1.8 for HSF on an average. The energy dissipation is reduced by a factor of 0.5 on an average. The reduction of power dissipation improves the ability of the device to endure the fault.

IV. CONCLUSION

This paper has shown a new active protection circuit for IGBTs. The experimental results obtained under various conditions indicate that the proposed circuit has the following features:

- Precise detection of over-current can be done without an additional current sensor;
- Fast detection and quick reaction of the protection circuit are enough to effectively limit the initial peak current;
- Precise clamping of the fault current and measurement of Vce can improve the error signal noise immunity;
- The clamping of the fault current reduces the peak power and energy dissipation;
- Safe shutdown of fault currents can control the over-voltage level at turn-off.

The circuit is able to control not only the steady state but also the transient fault currents. In particular, the circuit has the ability to activate the protection circuit and limit the fault current at similar current level irrespective of fault impedance and on-state gate voltage.

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