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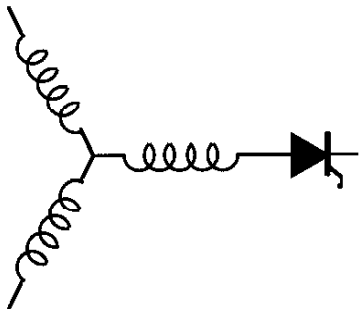

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A Reduced Parts Count Realization of the Resonant Snubbers for High Power Current Stiff Converters

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Abstract - Resonant snubbers have been shown to present significant advantages over classical RCD snubbers in Current Stiff Converters (CSC). In this paper, a new realization of resonant snubbers in CSC topologies is introduced requiring only two extra thyristor-type devices. The rating of these snubber switches is shown to be significantly lower than the ratings of the main converter. A complete discussion of the control issues related to this topology is presented. The compatibility of the resultant CSC topology with PWM methods is investigated and compared with a previously presented resonant realization employing six snubber switches. Simulation results are included to illustrate the CSC performance and support the topology analysis presented in this paper.

1. INTRODUCTION

Current Stiff Converters (CSC) are usually employed in high power levels (hundreds of kW and MW range). Among their features, it can be pointed out the CSCs sustained regeneration capability and improved overall reliability due to their inherent overcurrent and short circuit protection, unidirectional nature of the switches and the absence of electrolytic capacitors. CSCs also present inherent low input/output voltage dV/dt, an important characteristic considering the present EMI restrictions and EM compatibility with the load. The main drawbacks of classical PWM CSCs are associated to their low switching frequency, limited to the range of a few hundreds of Hz in conventional GTO based topologies, mainly due to the switching losses [1]. Also, large AC side filter capacitors are required increasing converter cost and leading to low input power factor. Another drawback of low switching frequency operation is the large dc bus inductor required to smooth the DC bus current.

Advances in high power GTO-type devices such as the MTO [2,3] and the IGCT [4,5] are expected to have a significant impact in high power applications, due to their fast switching characteristics and simplified gate drive requirements when compared to GTOs. The GTOs and MTOs require snubber circuits to shape their switching locus (non-square SOA) and switching losses can be significantly reduced in IGCTs with turn-off snubbers [6].

The present technology in snubber circuits employed in CSC topologies is the RCD snubber [7-9]. The bi-directional voltage blocking characteristic of the CSCs switches require non-polarized snubber circuits, preventing the use of most of the snubbers developed for VSCs. Among the drawbacks of the RCD snubber, it can be pointed out that: switching losses are transferred to the snubber resistor (heat still has to be managed) and no enhancement of converter efficiency is possible; size of the snubber capacitor is limited; voltage spikes and reapplied dV/dt (when the snubber diode snaps off) at turn-off exist due to series stray inductance, limiting devices and converter utilization.

A regenerative snubber for CSCs has recently been introduced [10]. This snubber circuit is rather complex and requires a large electrolytic capacitor and a transformer-coupled line commutated inverter for energy recovery for each individual switch. Also, since the circuit preserves the RCD snubber structure, several of the drawbacks listed above are still present.

The application of resonant snubbers [11,12] to CSC topologies is very promising from the perspective of overcoming these limitations [13,14]. The stray inductance in series with the snubber capacitor can be greatly removed since they be placed very close to the power device. Significantly higher current turn-off and consequently power control capability follows from that. A lossless snubber reset mechanism is provided, allowing larger snubber capacitors and leading to lower SOA requirements and lower turn-off losses (increase in the overall converter efficiency). The reduction in the switching losses can be also seen as extra room for conduction losses with the same cooling requirements, leading to an increase in the converter power control capability.

A new realization of the resonant snubber in CSC topologies allowing a significant reduction in the total parts count was recently proposed [15] and it is discussed in detail in this paper. This realization of the resonant snubber requires two extra thyristor-type devices with significant lower current and voltage ratings than the main converter devices. A converter control strategy is introduce, leading to true zero voltage switching (ZVS) of the main converter devices over the entire operating range. The modulation capabilities of the CSC with this reduced parts count resonant snubbers is also investigated. The topology is shown to be compatible with discontinuous PWM schemes.

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2. ANALYSIS OF THE NVD REALIZATION OF THE RESONANT SNUBBERS

Two commutation sequences are identified in converter topologies employing resonant snubbers [15,16]. The *passive commutation sequence* (incoming device is reverse biased) happens at the level of the snubber capacitors. The *active commutation sequence* (incoming device is forward biased), on the other hand, involves the active insertion of the snubber inductance in the circuit to create a resonant mode in the snubber. During this mode, the voltage across the incoming device is driven to zero, so that the incoming device can be turned-on under ZVS conditions. Notice that the active commutation sequence provides the snubber reset mechanism with minimum losses.

Fig. 1 shows a generalized form of the three-phase realizations of the resonant snubber that can be used to represent the current commutations processes involving any pair of devices in the same group [15]. The common-cathode group is represented here, but minor changes would lead the conditions encountered in the common-anode group (the dc link current and all the devices should be reversed).

For optimal commutation conditions [15] (minimum current and voltage stress on the main devices and snubber components) the snubber state and control variables at the beginning of the resonant mode of the active commutation sequence are such that :

$$\text{i) } v_{Sb,optimal} = \frac{v_f^{in} + v_f^{out}}{2}$$

$$\text{ii) } i_{Ls}(t_1) = i_{dc} \qquad (1)$$

where v_f^{in} and v_f^{out} are the line to neutral voltages associated with the incoming and outgoing devices, respectively.

Condition (i) in (1) can be shown to be closely approximated at any instant by the realization of the resonant snubbers in CSCs proposed by McMurray [11]. Condition (ii) implies a certain dwell time during which the current i_{Ls} through the snubber inductor ramps up (start of the active commutation sequence) and down (reset of the snubber inductor). It can be demonstrated that this dwell time is minimized if the line to line voltage associated with the incoming and outgoing devices, $v_f^{in} - v_f^{out}$, is maximized.

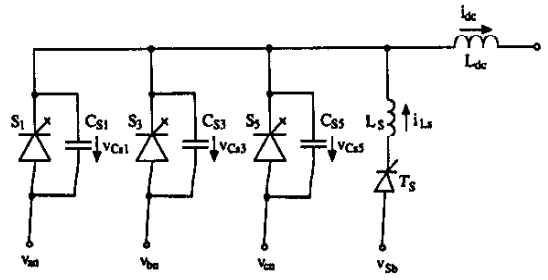


Fig. 1. Generalized representation of the CSC-RS.

The dwell time associated with the build up and reset of the optimal commutation conditions is always minimized if the active commutation process is employed in the commutation between devices associated with the maximum line to line voltage. This situation leads to a newly defined optimal driving voltage, $v'_{Sb,optimal}$, as shown in fig. 2.

Notice that $v'_{Sb,optimal}$ in fig. 2 is basically a zero sequence component with low amplitude in comparison with the amplitude of the line to line AC voltages ($\leq 0.14\ V_{LL,peak}$). This characteristic suggests that sub-optimal commutation conditions with no significant additional voltage stress on the main switches can be obtained by defining v_{Sb} equal to the neutral voltage, or $v_{Sb} = 0$. This definition leads to the basic form of the reduced parts count or *the neutral voltage driven (NVD) realization* of the resonant snubbers in CSC topologies shown in fig. 3.

The equations describing the resonant snubber state variables during the resonant mode in the active commutation process derived for the generalized form of the resonant snubbers in CSCs can be directly applied to this topology:

$$v_{Cs}(t\text{-}t_r) = Z_o\,[i_{dc} - i_{Ls}(t_1)]\,\sin\omega_o(t-t_1) - [v_f^{out} - v_{Sb}]\,\cos\omega_o(t-t_1) + v_f^{out} - v_{Sb} + v_{Cs}(t_1) \qquad (2)$$

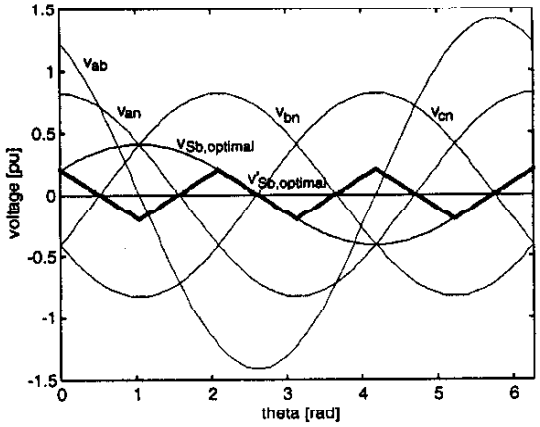


Fig. 2. Optimal snubber driving voltage.

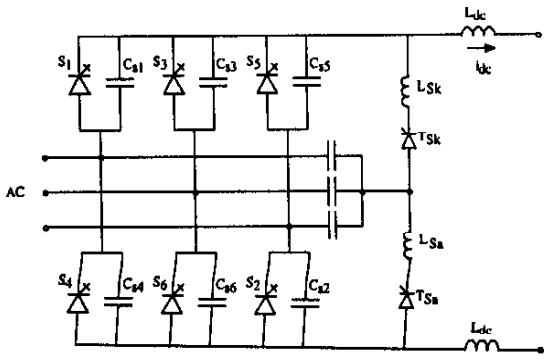


Fig. 3. The neutral voltage driven (NVD) realization of the resonant snubbers.

$$i_{Ls}(t-t_1) = -\frac{1}{Z_o}[v_f^{out} - v_{Sb}]\sin\omega_o(t-t_1) - [i_{dc}-i_{Ls}(t_1)]\cos\omega_o(t-t_1) + i_{dc} \quad (3)$$

where $\omega_o=1/\sqrt{L_sC_{eq}}$, $Z_o=\sqrt{L_s/C_{eq}}$, $C_{eq}=3C_s$ and t_1 is the time instant when the resonant mode in the active commutation process starts (outgoing switch is turned off at $t=t_1$; the snubber switch was turned on at time $t=t_0$, $t_0<t_1$). From (2) and (3), the *necessary condition* to achieve zero voltage turn-on for the incoming switch, following an active commutation sequence, is derived as shown in eq. (4).

$$(v_f^{in})^2 \le Z_o^2[i_{dc}- i_{Ls}(t_1)]^2 + (v_f^{out})^2 \quad (4)$$

From (4) it is seen that if $|v_f^{out}| \ge |v_f^{in}|$, then the zero voltage turn-on is guaranteed for any value of $i_{Ls}(t_1)$, defining a *sufficient condition* to achieve zero voltage turn-on of the incoming switch; otherwise, $i_{Ls}(t_1)$ is seen as a control parameter that can be manipulated to obtain zero voltage turn-on conditions in the entire operating range.

Optimal commutation conditions, as defined for the generalized realization of the resonant snubber, are reached with the reduced parts count realization only if $v_f^{out} = -v_f^{in}$. Sub-optimal conditions are obtained elsewhere. The worst case scenario happens when the difference between $v_{Sb} = 0$ and $v'_{Sb,optimal}$ is maximum, corresponding to the points where either v_f^{out} or v_f^{in} are at their maximum value. Fig. 4 shows phase plane plots for the incoming device for commutation under the conditions: (a) $v_{Sb} > v'_{Sb,optimal}$; (b) $v_{Sb} = v'_{Sb,optimal}$ and (c) $v_{Sb} < v'_{Sb,optimal}$. Trajectories (a) and (c) correspond to $v'_{Sb,optimal}$ at its peak amplitudes. Since $v'_{Sb,optimal}$ satisfies condition (i) in eq.(1), if $|v_f^{out}| > |v_f^{in}|$, $v_{Sb} > v'_{Sb,optimal}$ and a voltage overshoot is observed across the incoming switch. On the other hand, if $|v_f^{out}| < |v_f^{in}|$, $v_{Sb} < v'_{Sb,optimal}$ and the voltage overshoot occurs across the outgoing switch.

The peak voltage across the main switches can be obtained by applying the above conditions into eq. (2) with $v_{Sb}=0$. The peak voltage stress associated with the NVD realization is then given by:

$$v_{Cs,peak} \approx 2\, v_{f,\,peak} = 1.63 \text{ pu} \quad (5)$$

Comparing the peak voltage in (5) with the standard voltage stress (1.42 pu, corresponding to the peak line voltage), it is seen that the additional voltage stress is not significant (about 15%). This extra voltage stress associated with the NVD realization is certainly off-set by the benefits associated with the reduction in the total parts count.

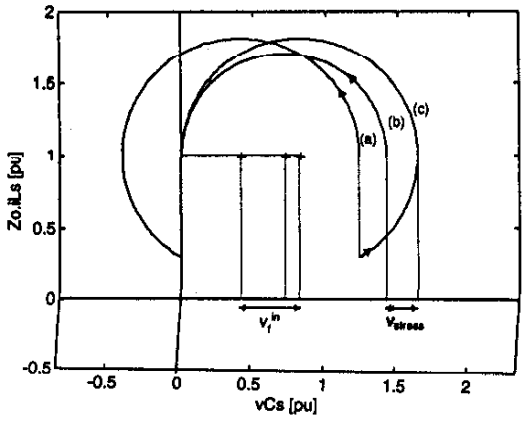
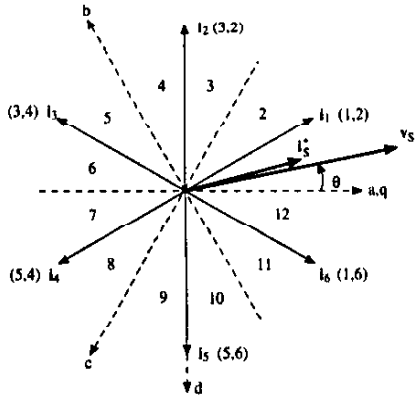


Fig. 4. Phase plane plots.

3. CONTROL AND MODULATION ISSUES

A. Converter control

As was mentioned before, the passive commutation process involves the snubber capacitors only. Zero voltage turn-off and turn-on of the devices is inherently guaranteed. In this sense, the use of the passive commutation process is preferred from the perspective that it involves fewer switchings than the active commutation process and no control is required. In general, all the devices in the group undergoing commutation conduct current during a certain interval of the switching period. This fact implies that by ordering the conduction time of the devices according to their associated phase voltage (from higher to lower), one can reduce the number of active commutations to one per switching period. This switching sequence leads naturally to the desired condition when the active commutation occurs between devices associated with the highest and lowest phase voltages. Fig. 5 below illustrates a near unity power factor condition for the converter operating as a rectifier. The suitable switching sequence in this case is indicated in the same figure, where $\xrightarrow{p}$ and $\xrightarrow{a}$ indicate passive and active commutation processes, respectively. Notice



Common-cathode group: $S_1 \quad S_1 \quad S_1 \quad S_1 \ldots$

Common-anode group: $S_2 \xrightarrow{p} S_6 \xrightarrow{p} S_4 \xrightarrow{a} S_2 \ldots$

Current vector: $i_1 \xrightarrow{p} i_6 \xrightarrow{p} i_0 \xrightarrow{a} i_1 \ldots$

Fig. 5. Converter switching sequence.

that for the situation in fig. 5 there is no commutation in the common-cathode group. This switching pattern where only one of the main switches group commutates (each switch conducts continuously for a $\pi/3$ interval) is a consequence of the modulation based on adjacent vectors and the existence of three null vectors CSC topologies.

The basic issue in terms of converter control is guaranteeing zero voltage turn-on for the incoming device following an active commutation process. According to the analysis presented in the previous section, if the commutation conditions are to be as close as possible to the optimal ones (1), then $i_{Ls}(t_1)$, and consequently t_1, is the correct manipulation parameter. The locus of the values of $i_{Ls}(t_1)$ can be obtained directly from (4). Notice that (4) has real solutions for $i_{Ls}(t_1)$ only if $|v_f^{in}| \geq |v_f^{out}|$ (zero voltage turn-on is always guaranteed otherwise). Under this condition, the time interval $t_1 = t - t_0$ marking the starting point of the resonant mode relative to the beginning of the active commutation process can be computed from (5):

$$t_1 = t - t_0 = L_s \frac{i_{dc}}{|v_f^{out}|} - \frac{1}{Z_o}\sqrt{(v_f^{in})^2 - (v_f^{out})^2} \qquad (5)$$

and the resonant mode is initiated actively by turning off the outgoing switch at $t = t_1 + t_0$. If $|v_f^{in}| < |v_f^{out}|$, then $i_{Ls}(t_1)$ is bounded by the DC bus current amplitude. In this case, commutation conditions closer to the optimal ones are obtained if the outgoing switch is turned off at $t = t_1 + t_0$ such that $i_{Ls}(t_1) \approx i_{dc}$. This situation is also reached by active turn-off of the outgoing switch. Another possibility is to allow zero current turn-off of the outgoing switch. However, the latter alternative should be avoided if significant reverse recovery current is expected, since it would boost the initial energy in the resonant snubber components, increasing the voltage stress across the main switches.

Another factor to be accounted for here is that t_1 corresponds to a dwell time leading to non-linearities in the modulation process. This dwell time becomes particularly important when the CSC with the NVD realization of the resonant snubber is used as an inverter in variable speed drive applications. Since the dwell time increases as the AC voltage goes down, it is important to establish an upper limit on the dwell time to avoid significant distortion of the AC currents. In order to guarantee an upper limit on the dwell time, the value computed for t_1 has to be always compared to the dwell time limit value, $t_{d,max}$. The latter value is assumed if t_1 computed from (5) exceeds the dwell time limit. Notice that this constraint implies that t_1 needs to be computed from eq. (5) even if $|v_f^{in}| < |v_f^{out}|$. In this case, the term associated with the square root is neglected and the t_1 corresponds to the interval for i_{Ls} to ramp up from zero to i_{dc}.

An important practical point regarding the energy boost mode is the fact that the storage time in high power medium voltage devices is of the same magnitude than the snubber inductor current rise time. In this case, the storage time should be included in the computations of t_1.

In the actual implementation of the CSC with resonant snubbers, a turn-off command can be sent to the devices in the main switches at any moment. If passive commutation conditions exist, a turn-on command is sent simultaneously to the incoming switch, provided that there is no reduction in the reverse voltage blocking capability of the power devices. The incoming switch enters conduction as soon as it is forward biased. If active commutation conditions exist, the devices in the incoming switch can only receive a turn-on gate signal if zero voltage switching conditions have been already established. Turn-on commands can be sent along with turn-off commands in this case if a zero voltage detection circuit is added to the gate driver circuits. This circuit passes the turn-on commands to the gate of the power devices in the incoming switch as soon as the specified voltage levels have been reached. Another possibility is to estimate the delay associated with the active commutation process and send the turn-on command at the computed time instant. Tracking the progress of the active commutation sequence by means of feedback signals from the power converter has been proposed for the control of similar converter topologies [17].

B. Modulation of the AC currents

The CSC with the present realization of the resonant snubbers is compatible but not restricted to regular sampled single-edge PWM methods employing the adjacent vectors approach, as seen from the switching sequence in fig.5. Harmonic elimination techniques typically employed with low switching frequency GTO-CSCs [1,8] can also be employed.

The modulation process consists of the selection of the current vectors involved and computation of the respective modulation intervals. Space vector methods were applied to the CSC and analytical expressions for the modulation interval were obtained (6). These expressions can be solved on-line or used to generate standard look up tables (1 pu modulation index and switching period).

$$t_m = T/i_{dc}\,(-i_{qs}^{*}\sin\theta_n - i_{ds}^{*}\cos\theta_n)$$

$$t_n = T/i_{dc}\,(i_{qs}^{*}\sin\theta_m + i_{ds}^{*}\cos\theta_m) \qquad (6)$$

where T is the sampling interval; vectors $\mathbf{i}_m$ and $\mathbf{i}_n$ are adjacent to $\mathbf{i}^*$ and $\theta_m - \theta_n = \pi/3$ rad. The modulation index information in embedded in the amplitude of the components of $\mathbf{i}^*$ in the stationary reference frame.

The switching sequence defined by the control scheme somewhat degrades the performance of the modulation algorithm. Since the current vectors involved in the modulation are switched according to their relative position with respect to the AC voltage vector, a vector sequence inversion is observed in the switching pattern at $\pi/3$ intervals. As a result, low frequency harmonics are present in the AC currents. The resultant harmonic distortion is similar to the one observed in hard-switching VSCs associated with the blanking time.

The modulation characteristics of the CSCs employing the NVD realization of the resonant snubbers are quite similar to the ones associated with the McMurray realization [15], given the same constraints in terms of converter control. Notice, however, the significant reduction in the total parts count achieved with the NVD realization when compared to the former one.

4. SIMULATION RESULTS

Simulation results are presented in this section, obtained from a SABER model of the CSC topology with the NVD realization of the resonant snubbers operating in the rectifier mode. The simulation conditions are:

$V_s = 2300\ V_{rms}$; $|i_s| = 120$ A; $\cos\phi = 1.0$
$i_{dc} = 150$A; $f_{sw} = 1800$ Hz

The snubber components were designed to limit the maximum rate of voltage change across the switches to 500V/μs and the peak current through the snubber inductor to twice the rated DC bus current. The snubber parameters employed in the simulation were:

$$L_S = 47\mu H; \quad C_S = 100\ nF$$

where $L_S = L_{Sk} = L_{Sa}$ and $C_S = C_{S1} = C_{S2} = \ldots = C_{S6}$.

Fig. 6 shows typical waveforms of a CSC topology employing the NVD realization of the resonant snubbers. Each snubber inductor-switch branch is involved in half of the active commutations during one switching cycle. Notice also the reduced voltage stress on the snubber switch (T_{Sk}) compared to the main converter switches (S_1). Fig. 7 shows a plot of the current at the terminals of the CSC (no filtering). The three level PWM pattern is noted. The current waveform shows some spikes with amplitude equal to $i_{dc}/3$. These spikes are associated with the commutation processes. The DC bus (passive commutation) and the snubber inductor current (active commutation) are divided more or less equally between the snubber capacitors in the group undergoing commutation since the AC voltages clamp the voltage difference between any pair of snubber capacitors. The frequency spectrum of the AC currents is also included in fig. 7. Low order harmonics are present (5^{th}, 7^{th}, ...) , associated with the discontinuous (single edge) PWM method employed with this topology. The non-filtered 5^{th} harmonic amplitude is about 5% of the fundamental current amplitude.

Fig. 8 shows a detailed view of the passive commutation process. The incoming device turns on undergoes a zero voltage turn-on. The turn-on dI/dt is limited by the power devices current rise time and/or the leakage inductance in series with the switch. With GTO-type devices, forward biased second breakdown protection is provided by the snubber capacitor (zero voltage turn-on).

Fig. 9 shows the active commutation waveforms for near optimal commutation conditions ($v_{Sb} \approx v'_{Sb,optimal}$) between switches S_1 and S_5 in the common-cathode group. The incoming device is gated on at the zero crossing point Again, the turn-on dI/dt and leakage inductance limited. The corresponding snubber waveforms are shown in fig. 10. It is shown that the snubber inductor-switch branches are decoupled and high dV/dt stresses are not created across the

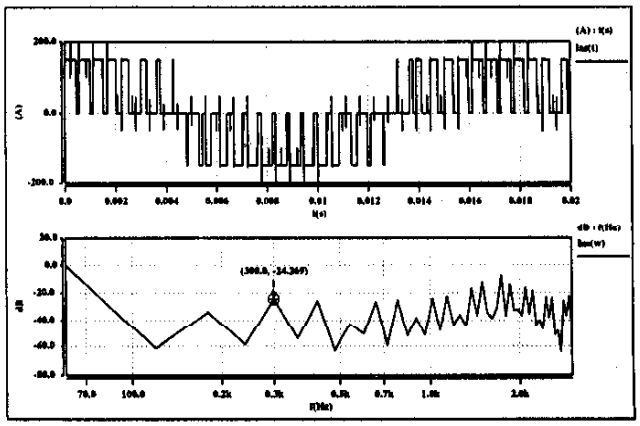


Fig. 7. CSC-NVD input current.

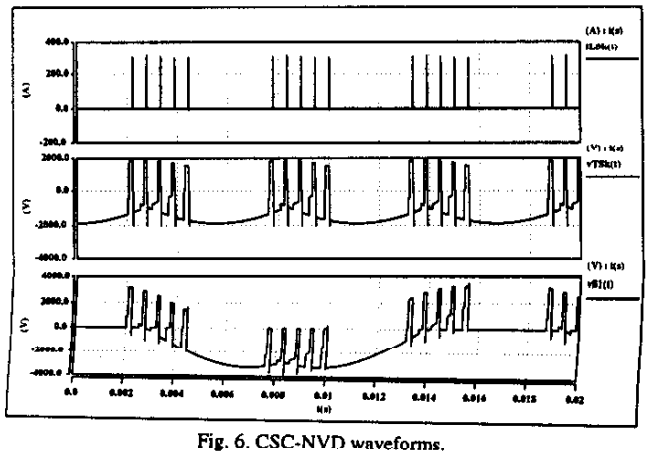


Fig. 6. CSC-NVD waveforms.

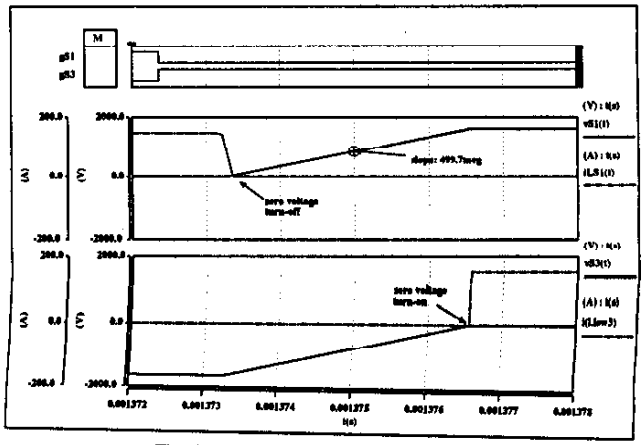


Fig. 8. Passive commutation waveforms.

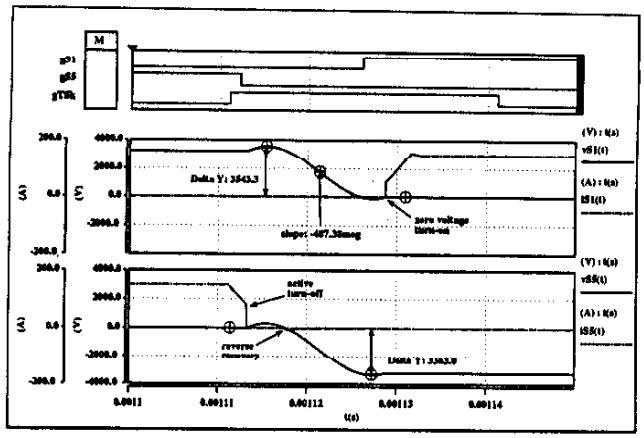


Fig. 9. Active commutation waveforms ($v_{Sb} \approx v'_{Sb,optimal}$).

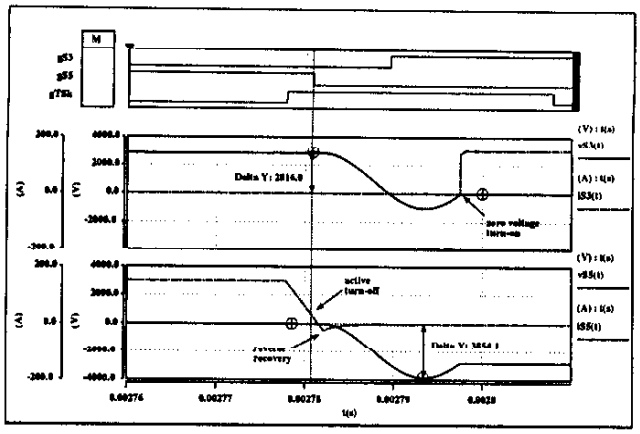


Fig. 11. Active commutation waveforms ($v_{Sb} >> v'_{Sb,optimal}$).

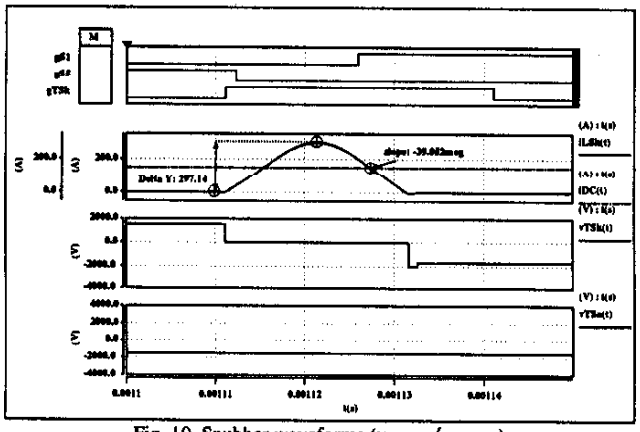


Fig. 10. Snubber waveforms ($v_{Sb} \approx v'_{Sb,optimal}$).

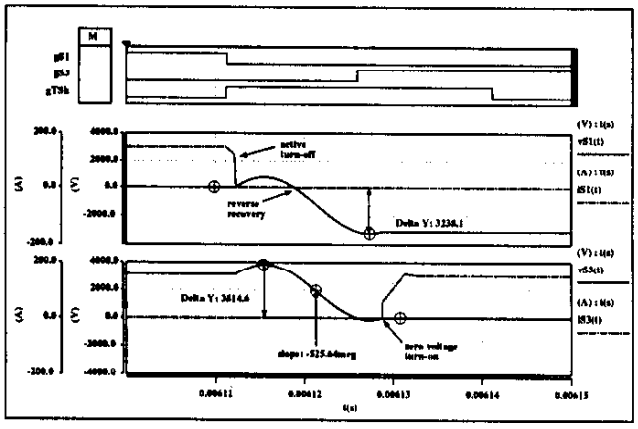


Fig. 12. Active commutation waveforms ($v_{Sb} << v'_{Sb,optimal}$).

complementary snubber branch. In fact, the dV/dt across the snubber switches is also limited by the resonant snubber action, allowing the use of fast thyristor devices in the snubber switches.

Figs. 11 and 12 show active commutation waveforms for the situations where $v_{Sb} >> v'_{Sb,optimal}$ and $v_{Sb} << v'_{Sb,optimal}$, respectively. As pointed out before, the voltage overshoot occurs across the outgoing switch in the situation depicted in fig. 11 and across the incoming switch in the situation illustrated in fig. 12. In both cases, the peak voltage amplitude is in close agreement with the predicted value (1.63 pu).

An interesting phenomena observed in these simulations is the boost effect from the reverse recovery process in the outgoing devices in the active commutation sequence (the outgoing switch always blocks forward voltage after a passive commutation). The reverse recovery current through the power devices in the outgoing switch changes the energy distribution among the snubber components during the resonant mode. The energy in the snubber is boosted since the snubber inductor current increases by an amount equal to i_{rr}.

The voltage and current ratings for all the switches in the converter are summarized in Table I. The RMS current through the snubber switches is quoted at 1800 Hz, since this is a switching frequency dependent rating. Fig. 13 shows a plot of the RMS snubber inductor current versus switching frequency for the NVD realization.

4. CONCLUSIONS

In this paper, a new realization of the resonant snubbers for current stiff converters, employing the neutral voltage as the snubber driving voltage was introduced. An important advantage of this realization over that initially proposed by McMurray (6 snubber switches, 3 inductors) is the significant reduction in the snubber parts count (2 snubber switches, 2 inductors in the NVD realization), while preserving compatibility in terms of modulation and control characteristics. Another advantage is the low voltage and current rating of the snubber switches and effective limitation of the dV/dt across the snubber switches by the normal operation of the resonant snubber. These characteristics are particularly important in practical implementations, since they point out to the possibility of using fast thyristors in the snubber switches.

Improvement in the performance characteristics of CSCs, pushing the switching frequency into the low kHz range, implies necessarily in reviewing the snubber circuits employed in this converters. The absence of a stiff DC bus voltage in-